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DESIGN OF A PRINTER SYNCHRONIZER FOR VERIFYING DATA CONVERSIONS

by

Frederick Holser

APPLIED MATHEMATICS LABORATORY
RESEARCH AND DEVELOPMENT REPORT

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ABSTRACT

This report summarizes the design and development of a digital synchronizer and page printer that has been integrated into the Computer Data Format Translator system to provide a means of printing out and thus verifying the validity of data conversions performed by this system.

ADMINISTRATIVE INFORMATION

Sponsored by Bureau of Ships under Project Number SR 003-09-01 Task 0005.

INTRODUCTION

The synchronizer and printer described in this report have been integrated into the complex of equipment comprising the Computer Data Format Translator system (CDFT) manufactured by the Electronic Engineering Company (EECO) of California. Briefly, the CDFT is a large scale, multi-purpose, data translator (or converter) with analog-to-digital and digital-to-digital conversion capabilities. A detailed summary of the characteristics and capabilities of this system is available in References 1 and 2.[1] Since its installation at the Applied Mathematics Laboratory in 1960, this unique system has had an ever-increasing work load. This is especially true in the area of analog to digital conversion work done in conjunction with instrumentation and sea trial test data reduction.

With the steady growth of the work load, and the increased need for higher accuracy and reliability of data conversions, a need became manifest for a printout facility to check and analyze the performance of these conversions "on-line." A printing "system" comprised of a

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[1] References are listed on page 23.

synchronizer and an Anelex line printer* was designed and developed under Project 1-860-938-01. A block diagram of the CDFT and the interconnections to the synchronizer are shown in Figure 1.

The basic printer mechanism can print up to 70 digits to a line at a maximum rate of 600 lines per minute.

FABRICATION TECHNIQUES AND LAYOUT

The synchronizer was constructed in a standard 19 in. rack cabinet using plug-in circuit "modules" (see Figure 2). This cabinet contains all of the logic for implementing the storage, code recognition, control, and communication functions between the printer and translator system. Included in this cabinet are the power supplies for the synchronizer and the master control panel for switching and time-sequencing the primary power for the entire printing system. Controls for operating and testing the system are located on the front panel of the synchronizer cabinet. Cooling is accomplished by using the chilled air available within the translator plenum floor system. The air enters the bottom of the cabinet, passes over the components, and is exhausted at the top of the cabinet by a blower.

The plug-in modules or "cards" used in this project (see Figure 3) are the tube-and-diode type manufactured by EECO of California and are nearly identical to those used in the CDFT system. These particular cards were selected because an abundant supply was already available. They offer direct electrical compatibility to those used in the CDFT. With the exception of 12 special circuits required to interface the printer and synchronizer electronics, all of the cards (132 in total) in the system are of standard EECO design and are interchangeable with those of the CDFT. Five of the special circuits are level changers, custom designed to maintain compatibility between the low level signals generated at the printer timing disk (6v) and the higher level (20v) of the synchronizer logic (see Figure 4). Within the synchronizer, a binary "one" is represented by a -20-v level and a binary zero is represented by a 0-v level.

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*This commercially manufactured equipment is described in Reference 3.

The seven remaining special circuits are thyratron drivers; see Figure 5. These drivers were designed to provide the proper signal fuel necessary to threshold bias the thyratron hammer drivers located in the Anelex pedestal. The printer and its companion unit, the "pedestal," are commercial models of equipment manufactured by the Anelex Corporation (see Figures 6 and 7).[3] The printer is mounted on a pedestal which houses the hammer drivers and other electronics associated with the electro-mechanical assemblies of the printer.

THEORY OF OPERATION

A. BASIC PRINCIPLES

Printer

An analysis of the synchronizer design must necessarily be preceded by a discussion of the essential characteristics of the printer. The printer operates on an impact principle, i.e., printing is accomplished by a hammer actuator striking the paper onto a revolving print roll through an inked ribbon. The printing symbols are engraved upon the periphery of this roll in bands; each band contains a complete set of symbols. There are 70 such bands, one for each printing position across the paper. The basic timing for the print operation is established by a timing rotor (or pulse generator) which revolves with the print roll. This rotor provides "character" pulse that occur at each digit (printing symbol) position around the print roll and an "index" pulse that occurs once per revolution. The index pulse provides the timing for the input load cycle as well as for the print cycle.

Synchronizer

Figure 8 is a simplified block diagram which shows the essential control logic of the synchronizer.

The input data from the CDFT are loaded into storage registers composed of 6-bit flip-flop operating as binary counters. There are seven of these registers, each with a capacity for storing one 6-bit digit. The data are read in (6 bits at a time) in a parallel fashion, such that it "pre-sets" each register to the complemented binary value represented

by the incoming symbol code. After the data are read in, the control logic of the synchronizer allows character pulses to enter serially and advance the binary count of each register. As each register reaches a full condition, i.e., all flip-flops are equal to "one's," it emits a pulse to activate its respective print hammer.

It requires seven transfers of data from the CDFT to fill these registers, after which a group of seven characters is printed. The loading process is accomplished during the time interval of the index pulse which is 1.25 msec. As mentioned previously, the binary data taken from the CDFT are interpreted in their complementary form. For an example, a binary one would enter the synchronizer register as 111110. In this manner, the number of pulses required to fill the counter is equal to the numeric value of the printing symbol. Thus, as in the case of the binary one, a single character pulse will advance the register to a full condition and print the number 1, which is engraved in the first printing position on the print roll.

A print operation is initiated by a select pulse (level change) from the CDFT. The Select pulse interrogates the availability gate (No. 49) to determine if the synchronizer is in a receptive status, i.e., if all lockouts inactive. The lockouts (or inhibits) are active whenever the synchronizer is engaged in code recognition (preparatory to printing) or the printer is actually printing, or the paper is feeding. If upon selection by the CDFT, all lockouts are inactive, the synchronizer will respond by sending a control signal (designated unload sync) back to the CDFT. Within the CDFT, this signal is used to "gate out" each digit of data from the CDFT memory.

Concurrently, with each group of data transferred from the CDFT, a Write Sync pulse is sent back to the synchronizer. Within the synchronizer, the write sync pulses are used to advance the storage register loading counter and to generate additional unload sync pulses. It will be recalled that upon selection, the synchronizer generated the first unload sync pulse sent to the CDFT. It was this first unload pulse that gated out the first group of data (with an accompanying write sync pulse). Thereafter, the write sync pulses are used to generate each succeeding unload sync pulse and to advance the loading counter. This process continues until

the loading counter reaches the count of 7, at which time the storage registers are full and the loading sequence is terminated. When this occurs, the print demand (PD) Flip-Flop 58 is set which phases a lockout on the availability gate (49) to prevent the transfer of additional data (preventing the generation of additional unload sync pulses) until the contents of the storage registers are printed out.

Since the storage register can attain a full condition asynchronously with respect to the timing of the print roll, the setting of PD flip-flop alone cannot establish the true start of a print cycle. A means of "synchronizing" the start of the print cycle with the index period of the print roll must be provided. This is accomplished by the print control (PC) Flip-Flop 52 in the following manner. The PC Flip-Flop is "reset" by the leading edge of the index pulse; it is subsequently set by the trailing edge of this same pulse if the PD Flip-Flop is set. This action insures that after the storage registers are full, the very next pulse (trailing edge time) can trigger the start of a print cycle. When the PC Flip-Flop is "set," it gates character pulses in from the timing disk to advance the binary value in the storage registers. As coincidence occurs at the register readout gates, pulses are emitted that energize the hammer drivers.

B. DETAILS OF LOGICAL FUNCTION

For the sake of clarity, certain details were omitted in the preceding simplified explanation of the basic operation. These details will now be discussed.

Since the storage capacity of the buffer unit is only seven digits, it is necessary to switch the output of this unit into ten logical paths in order to print a full line of 70 digits. This is accomplished (as shown in Figure 9) by using the shield grids of the print hammer thyratron drivers as gates, and arranging these into a 7 by 10 matrix. A 10-stage linear counter (designated group counter) is used to select the appropriate group. For each step of this counter, a group of seven digits are printed; the total number of digits to a line will be determined by the format selected. When the group counter reaches the predetermined value, a paper feed action is initiated and a lockout is placed upon the availability gate until 8 msec after the end of the paper feed action.

Once the printer is "selected," it will continue to operate until the "Select" signal is cleared by the CDFT at the end of a print operation. Whenever the data to be printed are not formated in a multiple of seven digits, the unfilled portion of the storage registers (remaining after the last transfer of data from the CDFT) is automatically loaded with fill digits. The > symbol was selected for this purpose. This operation is initiated by detecting the logical condition of a cleared select line occuring at a time when the loading counter is not equal to seven. The controlling logic for this operation is comprised of Inverted Circuit 20, the loading counter, Flip-Flop 17, and Gates 188, 12 and 13.

The operation is as follows (see Figures 10 and 11). Whenever the memory is empty or the print operation is to be terminated, the CDFT control circuits clear (to ground) the input "Select" signal. This swing to ground will set FF-17 via the output of Inverter 20. The M output of FF-17 enables G-12 and allows index pulses to gate through G-12 via "One-shot" 68, through G-13 and trigger Blocking Oscillator 14. The output of BO-14 will provide the signal to step the loading counter each index pulse time and provide the input buffer delay strobe to gate input information in from the bus. The M output of FF-17 also enables G-188, allowing a signal to enable Gates G-104 through G-110 via "Cathode Follower 189. This is a "jam-set" signal for bits "2^2" for the entire buffer register. All other input lines will be at ground level and will gate in all zeros for the remaining bit positions, resulting in the complemented bit format for the ">" fill symbol. The H output of Flip-Flop 17 will inhibit G-15 and block sending out "Unload Sync" signals to the CDFT control circuits. This "fill" sequence will continue until the loading counter is stepped to seven and initiates a print cycle as already described. At the end of the print cycles, a clear pulse will reset FF-17, effecting a paper feed section via FF-42, G-47, and Paper Feed FF-51. This paper feed section after each "fill" operation offers clear recognition of the memory area or the tape block size used in printing.

The paper-feed action is initiated either by the end of a "fill" print cycles or by satisfying the group counter selection via FF-42, G-47, and Paper Feed FF-51. This paper-feed action is controlled by a paper loop and a brush-sensing device housed on the paper-feed mechanism. As the

brush senser senses holes in the paper loop, Paper Feed FF-51 is reset via Level Changer 70 and the paper-feed action is terminated. Proper hole programming of the paper loop allows the desired format of paper spacing for any print operation. A "Paper Homing" switch was provided on the control panel to allow the paper to be "homed" in an initial condition prior to a printing run.

APPLICATION AND OPERATION

GENERAL INFORMATION

The printer system has numerous applications within the CDFT system in both the broad areas of operation and maintenance. In the case of operation, a variety of conversion modes are possible using the printer but in general these will fall into two basic categories:

1. Operations where it is desired to read a sample of analog data from tape, perform a digital conversion, and print out the results of this conversion.
2. Operations where it is desired to print from digital data previously recorded on magnetic tape.

The latter application is useful in verifying the results from a conversion run. It is this application, in particular, where a significant savings in time can be realized since it eliminates the delays inherent in off-line printer processing of an output tape. It should be pointed out that in its present configuration, the printing equipment cannot provide a continuous real-time printout during a tape-to-tape conversion.

In the area of maintenance, the printer serves as an aid in diagnosing and isolating system malfunctions and in evaluating overall system performance. Its value in this area will grow as maintenance techniques utilizing the printer are developed.

OPERATING CONTROLS

The operating controls are shown in Figure 12. The equipment is initially prepared for operation by energizing all power supplies. This is done by turning on "Main AC," "Printer AC," "Logic DC," and "Printer DC" in that order. After the expiration of an internal time delay, the

"DC On" indicator lights up. The system may now be manually cleared by operating the "master clear" switch. The desired format, i.e., the number of digits to be printed to a line, may be selected by a 10-position switch located on the front panel. Through the use of this switch, printing formats may be selected (in multiples of 7) ranging from 7 to 70 digits. The synchronizer is "set up" for a particular operating mode by inserting the appropriate plug board "patches" in the CDFT complex. The following modes have been developed using the patches indicated:

1. IBM BCD to Printer
   a. Use program patch "D."
   b. Use tape patch marked "IBM BCD-Printer."
   c. Use UFC patch marked "IBM BCD-Printer."
   d. Use character patch marked "IBM BCD-Printer."
2. Uniservo (UNIVAC) to Printer
   a. Use program patch "D."
   b. Use tape patch marked "Uniservo-Printer."
   c. Use UFC patch marked "Uniservo-Printer."
   d. Use character patch marked "Uniservo-Printer."

MAINTENANCE FACILITIES

For purposes of maintenance and testing, the system may be readily switched to an on-line testing mode by the control switches provided and located on the front panel of the synchronizer cabinet. To facilitate the ease of maintenance, all of the basic control and information signals are brought out to connectors or terminal strips on the back-board side of the cabinet. When in the "test" position, the "Test Operate" switch will provide a psuedo "Select" signal, allow any bit configuration to be jammed on the information bus by the "Code-Selector" switch, and will connect in a pair of phantastrones (PH-1 and PH-2) that will generate the psuedo "Unload sync" pulse with the proper delay to simulate the memory duty cycle and "Write sync" signal. Through the use of this test mode of operation, all of the printing characters and symbols can be tested for all print position completely off-line.

ACKNOWLEDGMENTS

The author wishes to acknowledge the excellent cooperation and assistance afforded him by many members of the Applied Mathematics Laboratory, in particular Mr. H. Lee Hancock, Jr. and Mr. T. W. Beswick. The assistance of Mr. Jack Fidiam of the Electronic Engineering Company is also acknowledged.

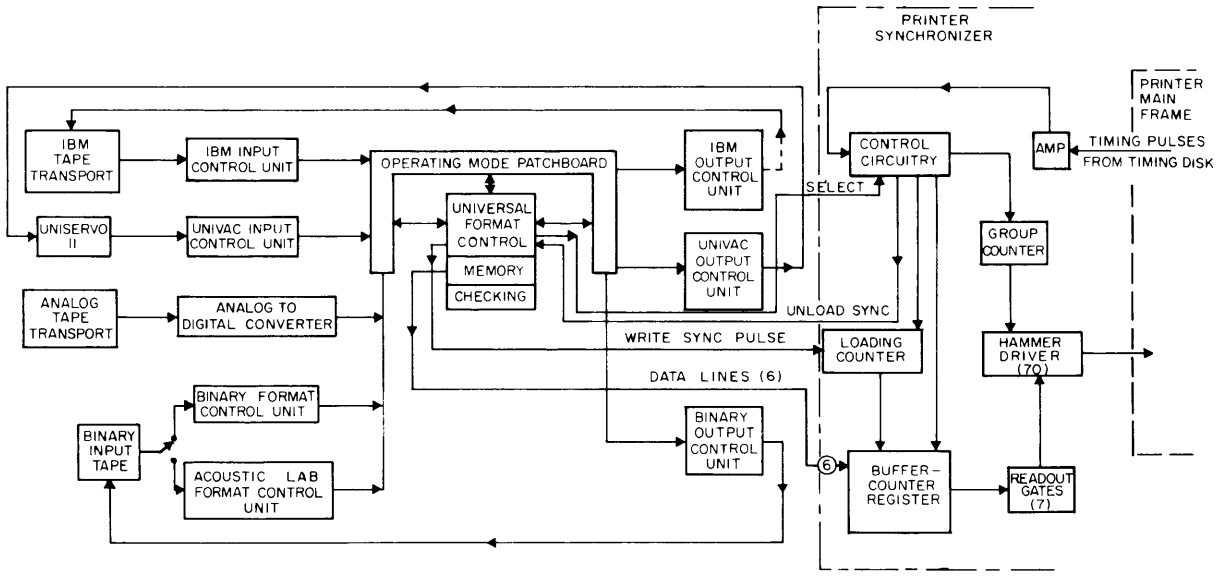


Figure 1 - Computer Data Format Translator and Synchronizer Interconnections

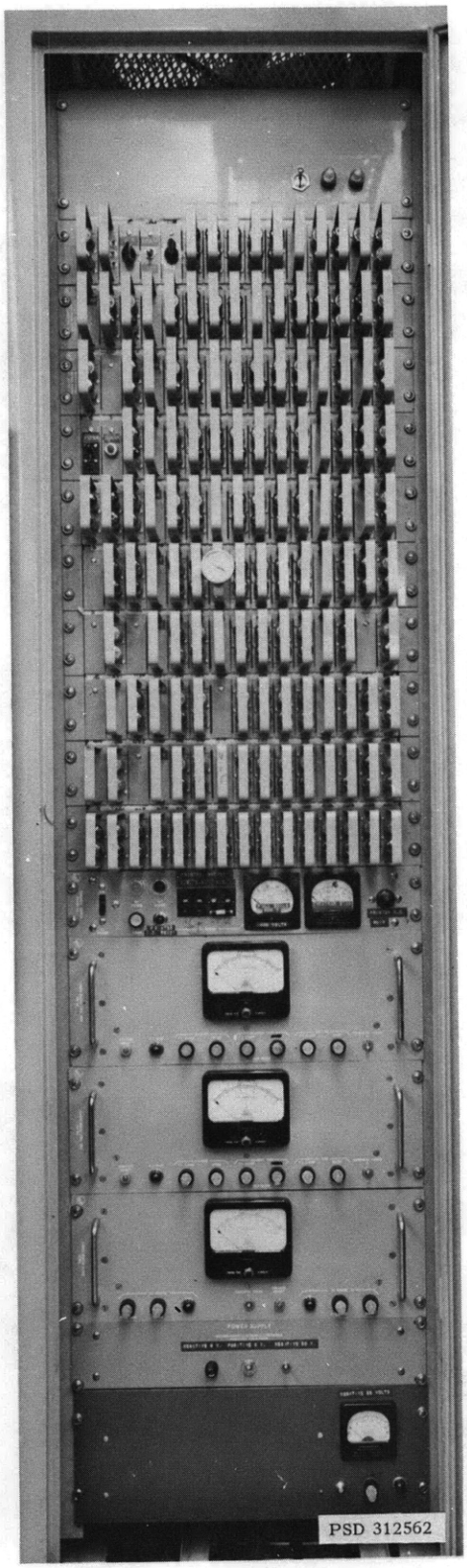


Figure 2 - Synchronizer Cabinet

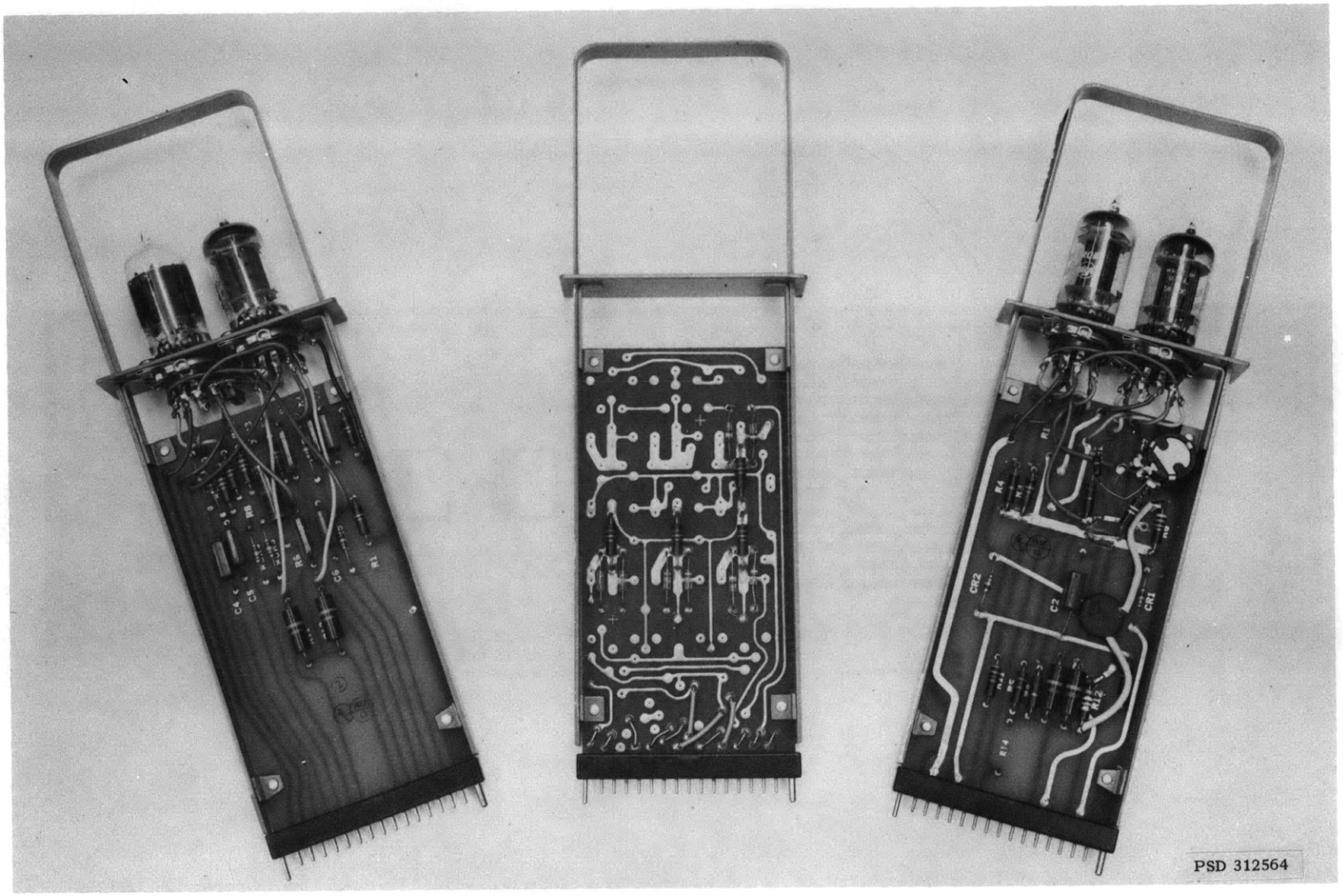


Figure 3 - ECCO Card Modules

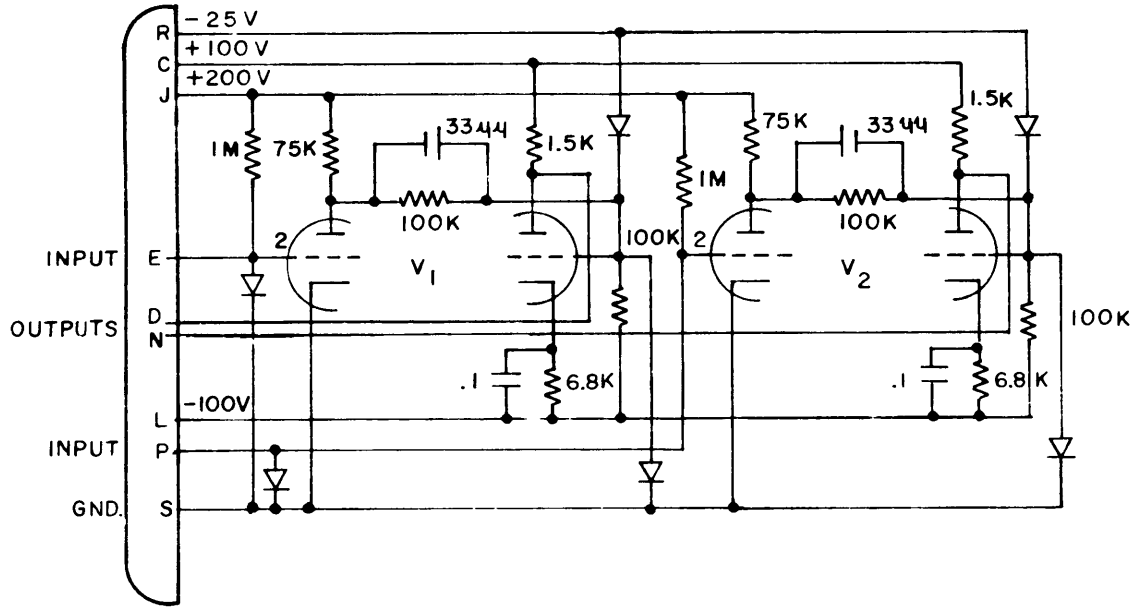


Figure 4 - Level Changer for Printer Synchronizer

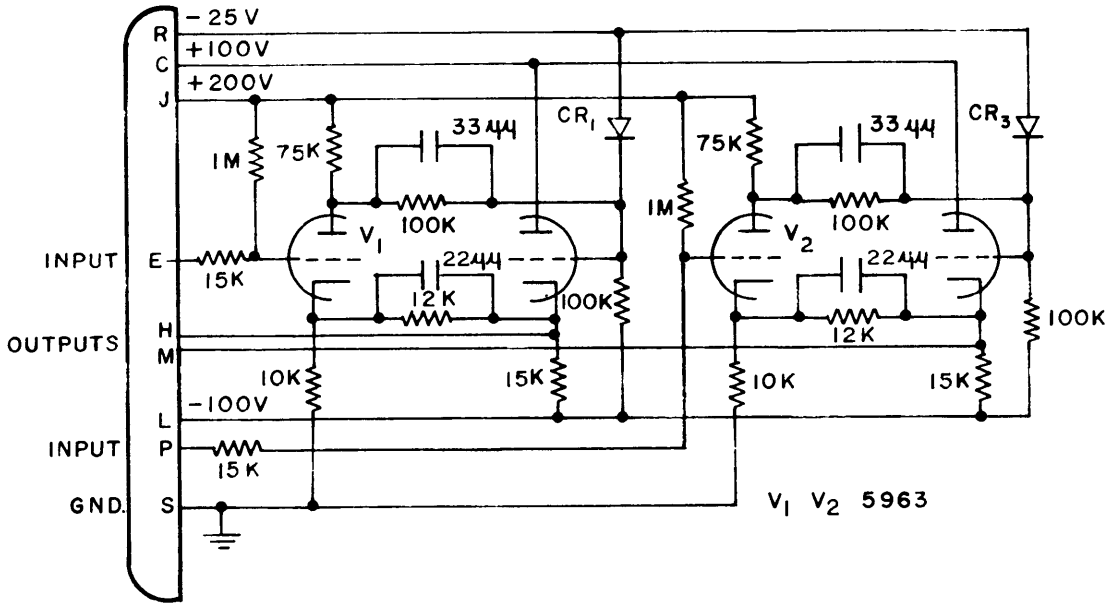


Figure 5 - Thyratron Driver for Printer Synchronizer

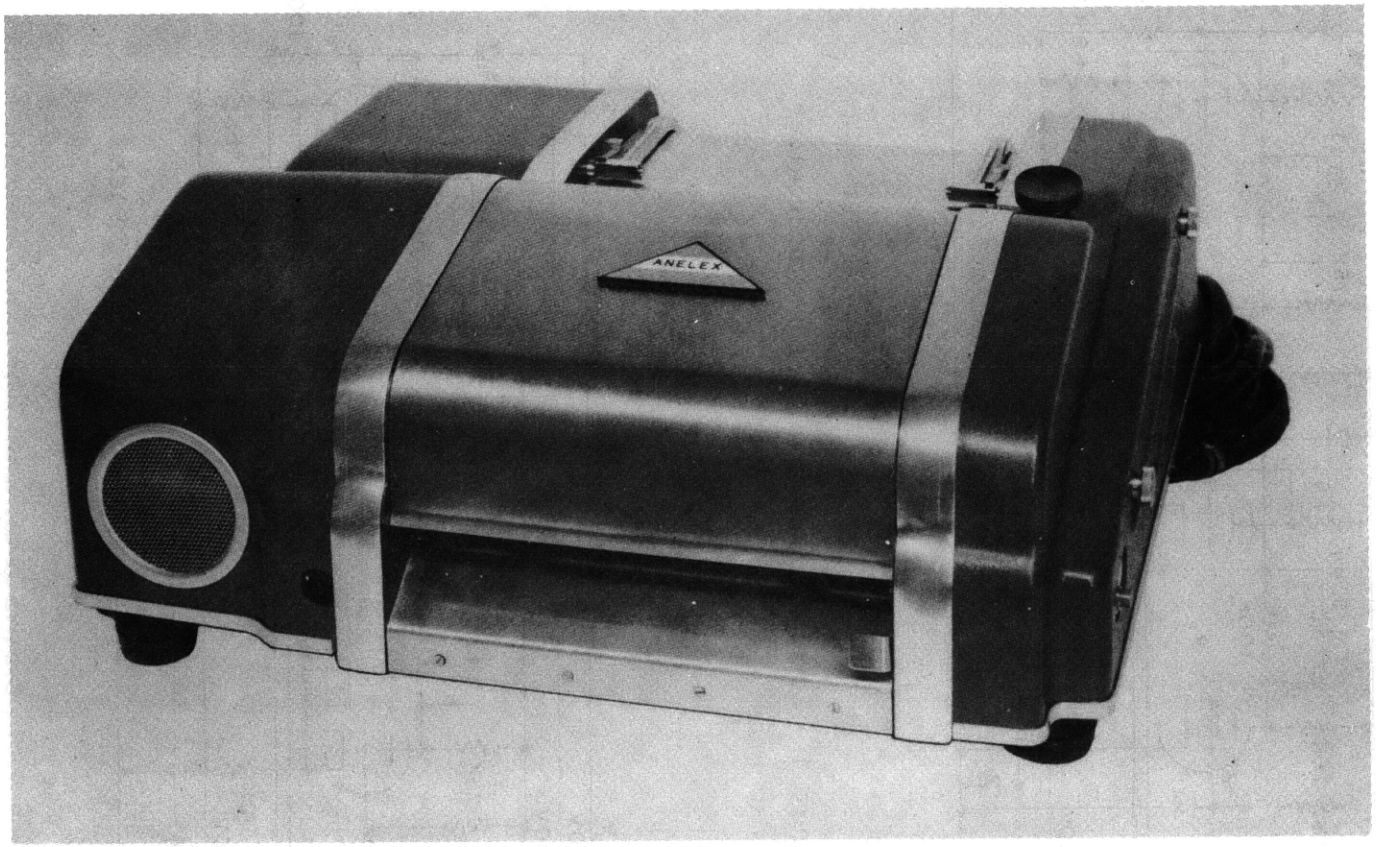
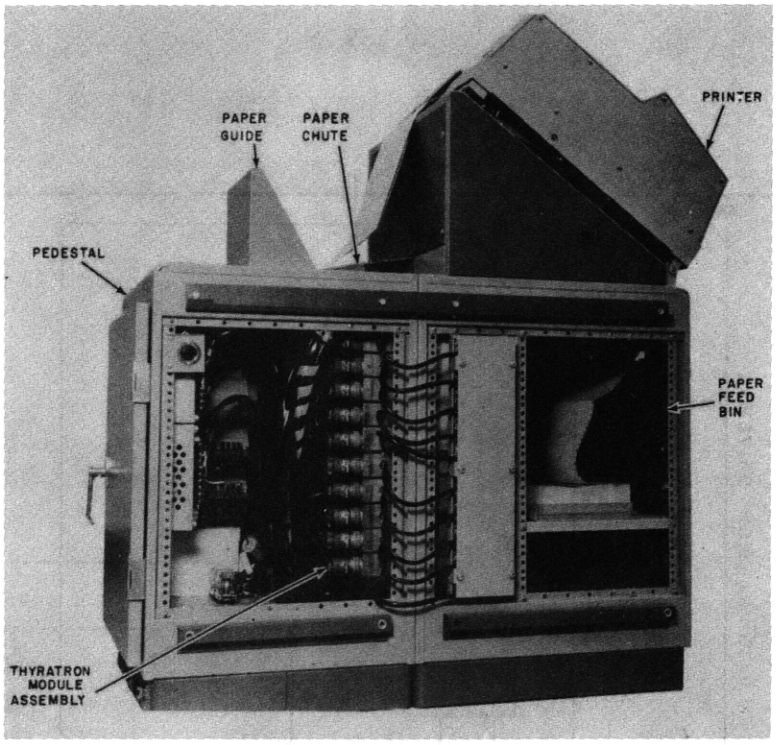


Figure 6 - Anelex Printer



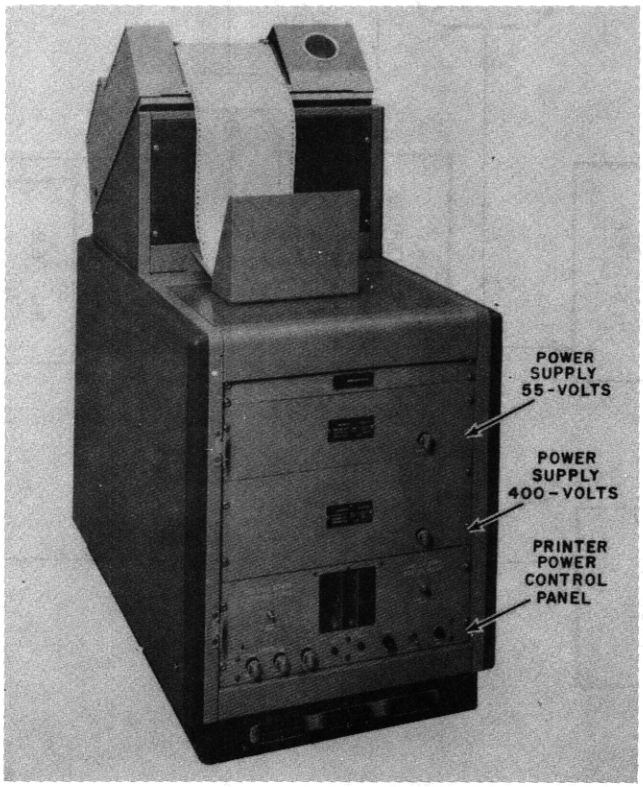


Figure 7 - Anelex Pedestal

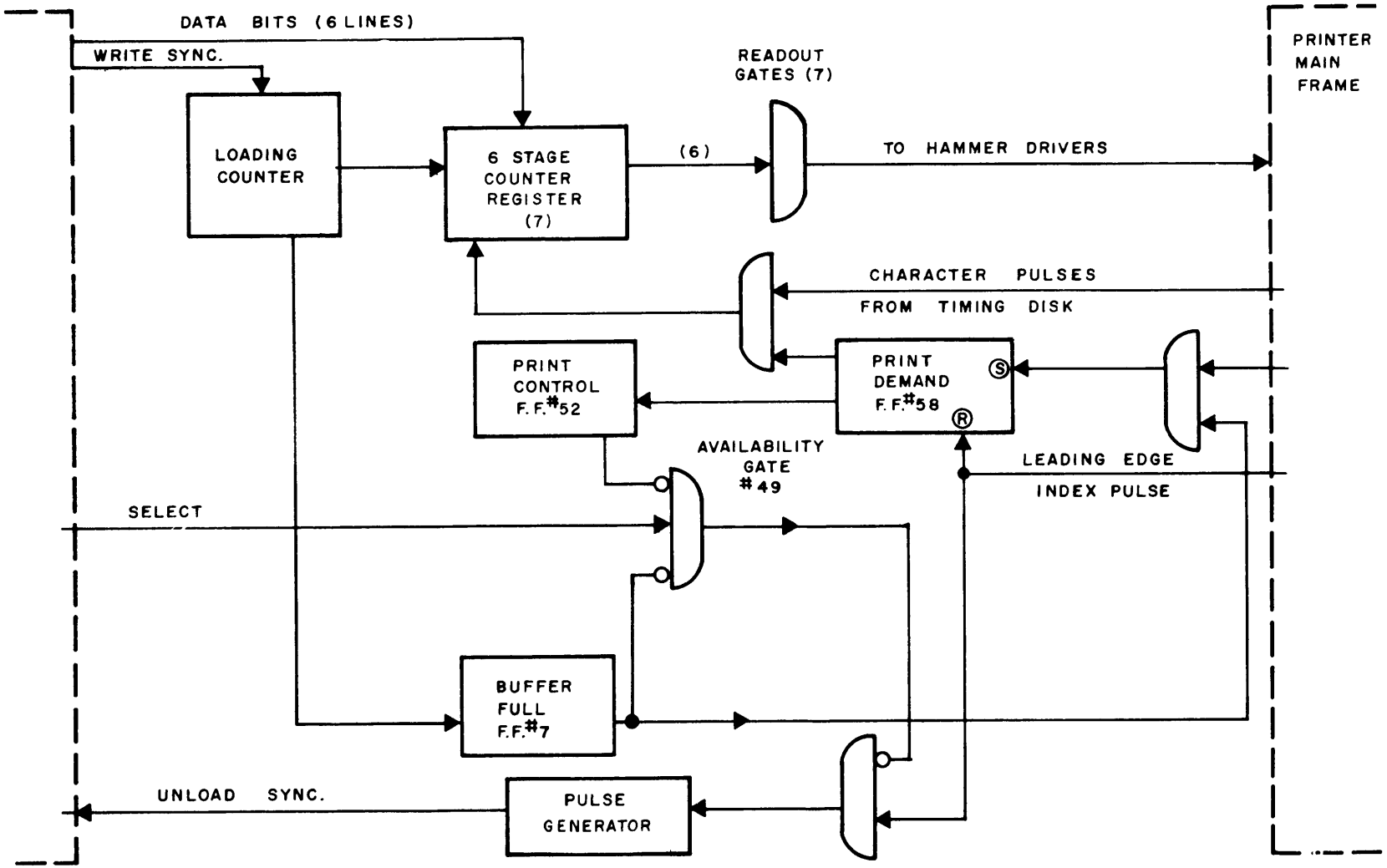


Figure 8 - Essential Control Logic of the Synchronizer

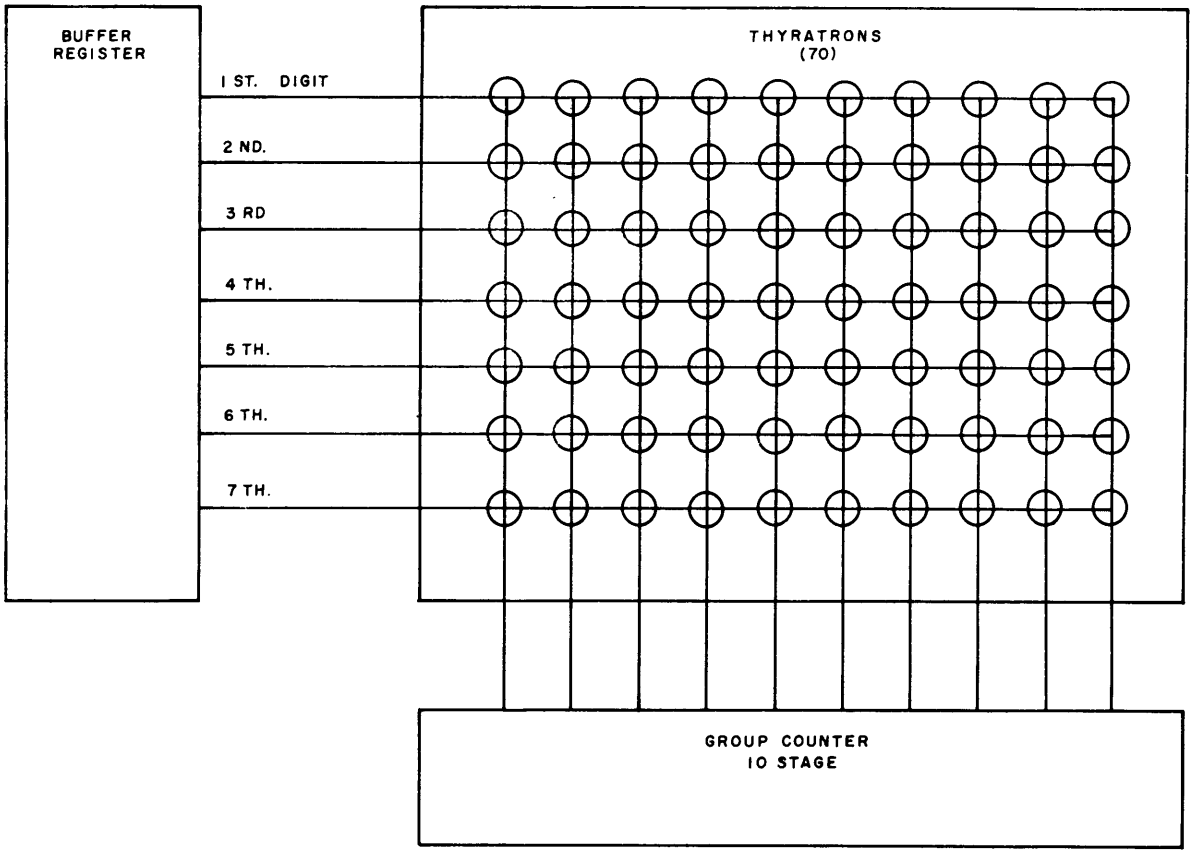


Figure 9 - Thyratron Matrix

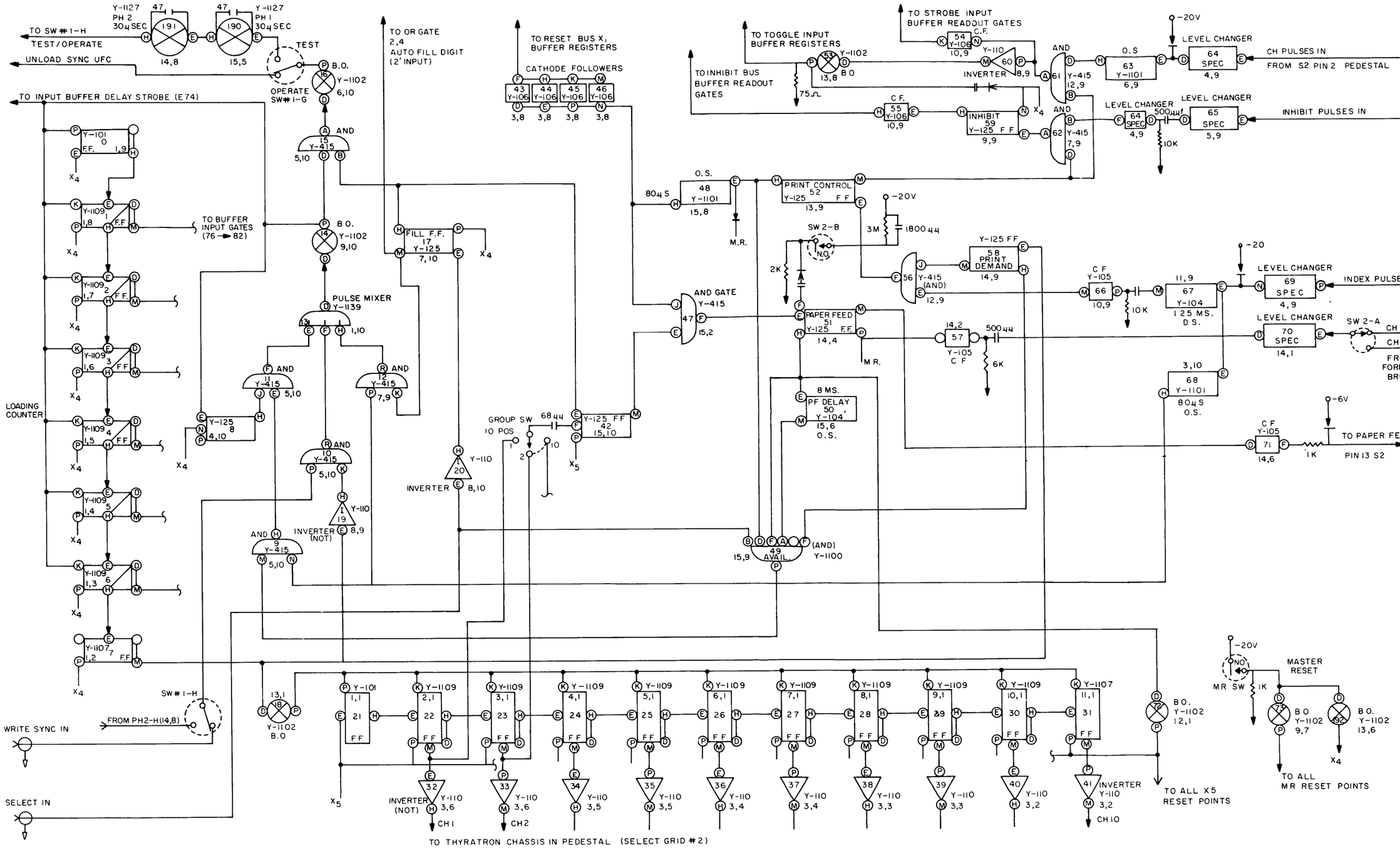


Figure 10 - Detail Control Logic Print

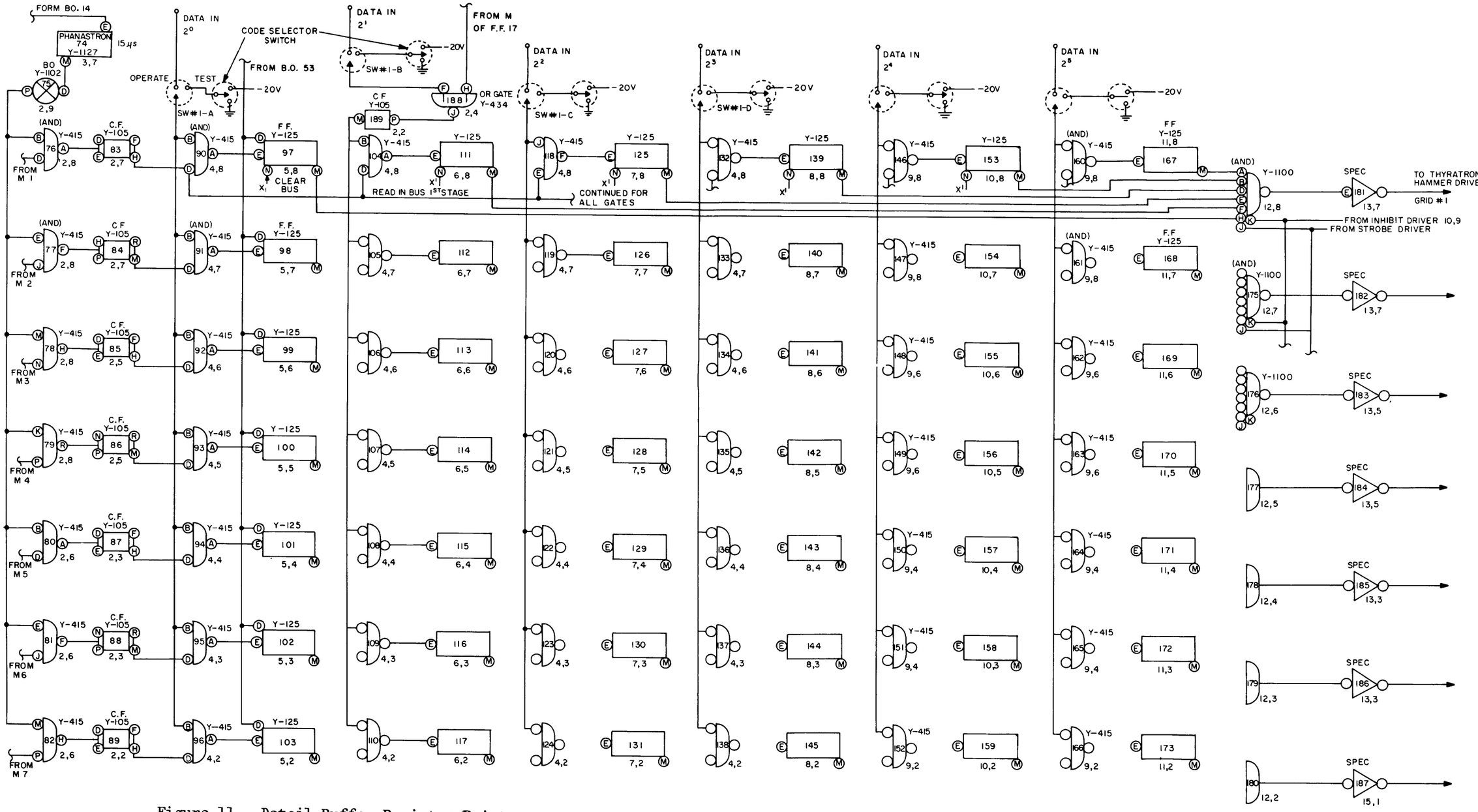


Figure 11 - Detail Buffer Register Print

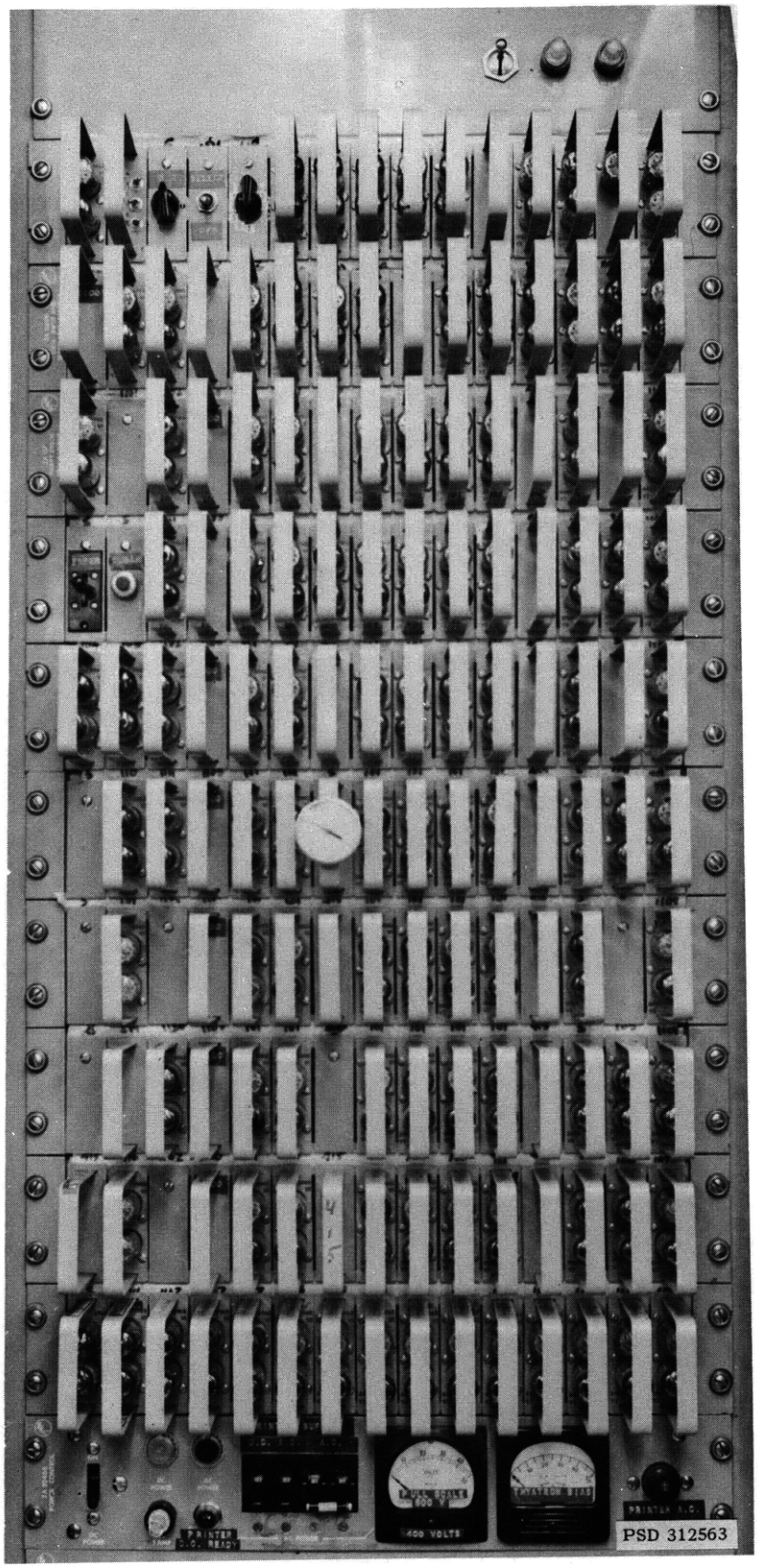


Figure 12 - Operating Control Panel

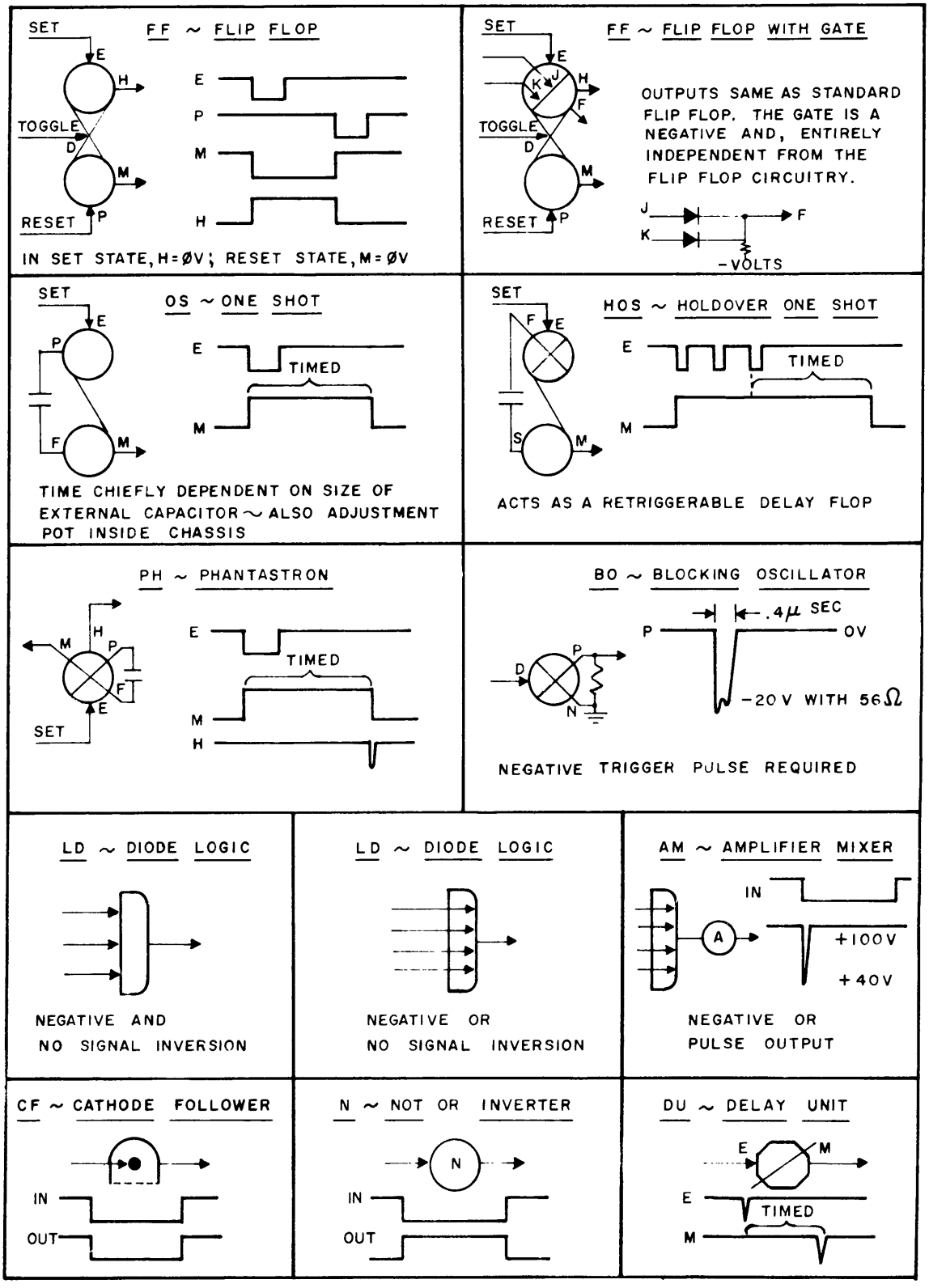


Figure 13 - CDFT Basic Circuits

Figure 14 - Card Location Guide

Logical Entity Number	Location by x, y Coordinates	Card Type	Function
0	1, 9	Y-101	FF
1	1, 8	Y-1109	
2	1, 7		
3	1, 6		
4	1, 5		
5	1, 4		
6	1, 3		
7	1, 2	Y-1107	
8	4, 10	Y-125	
9	5, 10	Y-415	And Gate
10	5, 10		
11	5, 10		
12	7, 9		
13	1, 10	Y-1139	Pulse Mixer (or gate)
14	9, 10	Y-1102	Blocking Oscillator
15	5, 10	Y-415	And Gate
16	6, 10	Y-1102	Blocking Oscillator
17	7, 10	Y-125	Fill FF
18	13, 1	Y-1102	Blocking Oscillator
19	8, 9	Y-110	Inverter (not)
20	8, 10		
21	1, 1	Y-101	FF
22	2, 1	Y-1109	
23	3, 1		
24	4, 1		
25	5, 1		
26	6, 1		
27	7, 1		
28	8, 1		
29	9, 1		
30	10, 1		
31	11, 1	Y-1107	
32	3, 6	Y-110	Inverter (not)
33	3, 6		
34	3, 5		
35	3, 5		
36	3, 4		
37	3, 4		
38	3, 3		
39	3, 3		
40	3, 2		
41	3, 2		
42	15, 10	Y-125	FF
43	3, 8	Y-106	Cathode Follower
44	3, 8		
45	3, 8		
46	3, 8		
47	15, 2	Y-415	And Gate
48	15, 8	Y-1101	One Shot
49	15, 9	Y-1100	And Gate
50	15, 6	Y-104	One Shot
51	14, 4	Y-125	Paper Feed FF
52	13, 9	Y-125	Print Control FF
53	13, 8	Y-1102	Blocking Oscillator
54	10, 9	Y-106	Cathode Follower
55	10, 9		
56	12, 9	Y-415	And Gate
57	14, 2	Y-105	Cathode Follower
58	14, 9	Y-125	Print Demand FF
59	9, 9	Y-125	Inhibit FF
60	8, 9	Y-110	Inverter (not)
61	12, 9	Y-415	And Gate
62	7, 9		
63	6, 9	Y-1101	One Shot
64	4, 9	Special	Level Changer
65	5, 9		
66	10, 9	Y-105	Cathode Follower
67	11, 9	Y-104	One Shot
68	3, 10	Y-1101	One Shot
69	4, 9	Special	Level Changer
70	14, 1		
71	14, 6	Y-105	Cathode Follower
72	12, 1	Y-1102	Blocking Oscillator
73	9, 7		
74	3, 7	Y-1127	Phanastron Delay
75	2, 9	Y-1102	Blocking Oscillator
76	2, 8	Y-415	And Gate
77	2, 8		
78	2, 8		
79	2, 8		
80	2, 6		
81	2, 6		
82	2, 6		
83	2, 7	Y-105	Cathode Follower
84	2, 7		
85	2, 5		
86	2, 5		
87	2, 3		
88	2, 3		
89	2, 2		
90	4, 8	Y-415	And Gate
91	4, 7		
92	4, 6		
93	4, 5		
94	4, 4		

Logical Entity Number	Location by x, y Coordinates	Card Type	Function
96	4, 2	Y-415	And Gate
97	5, 8	Y-125	FF
98	5, 7		
99	5, 6		
100	5, 5		
101	5, 4		
102	5, 3		
103	5, 2		
104	4, 8	Y-415	And Gates
105	4, 7		
106	4, 6		
107	4, 5		
108	4, 4		
109	4, 3		
110	4, 2		
111	6, 8	Y-125	FF
112	6, 7		
113	6, 6		
114	6, 5		
115	6, 4		
116	6, 3		
117	6, 2		
118	4, 8	Y-415	And Gate
119	4, 7		
120	4, 6		
121	4, 5		
122	4, 4		
123	4, 3		
124	4, 2		
125	7, 8	Y-125	FF
126	7, 7		
127	7, 6		
128	7, 5		
129	7, 4		
130	7, 3		
131	7, 2		
132	4, 8	Y-415	And Gates
133	4, 7		
134	4, 6		
135	4, 5		
136	4, 4		
137	4, 3		
138	4, 2		
139	8, 8	Y-125	FF
140	8, 7		
141	8, 6		
142	8, 5		
143	8, 4		
144	8, 3		
145	8, 2		
146	9, 8	Y-415	And Gate
147	9, 8		
148	9, 6		
149	9, 6		
150	9, 4		
151	9, 4		
152	9, 2		
153	10, 8	Y-125	FF
154	10, 7		
155	10, 6		
156	10, 5		
157	10, 4		
158	10, 3		
159	10, 2		
160	9, 8	Y-415	And Gates
161	9, 8		
162	9, 6		
163	9, 6		
164	9, 4		
165	9, 4		
166	9, 2		
167	11, 8	Y-125	FF
168	11, 7		
169	11, 6		
170	11, 5		
171	11, 4		
172	11, 3		
173	11, 2		
174	12, 8	Y-1100	And Gate
175	12, 7		
176	12, 6		
177	12, 5		
178	12, 4		
179	12, 3		
180	12, 2		
181	13, 7	Special	Thyratron Driver
182	13, 7		
183	13, 5		
184	13, 5		
185	13, 3		
186	13, 3		
187	15, 1		
188	2, 4	Y-434	Or Gate
189	2, 2	Y-105	Cathode Follower
190	15, 5	Y-1127	Phanastron
191	14, 8		

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