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SUBJECT: MEMORY-PLANE MARGINS: DCL-2-720 CORES VS. S-1 CORES

To: David R. Brown, Staff Group 63

From: J. L. Mitchell

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Approved: W. N. Papian

Abstract: Test margins taken on two 64x64 planes indicate that DCL-2-720 cores are superior to S-1 cores.

The object of these tests was to compare two 64x64 planes; one containing DCL-2-720 cores, the other a standard MTC plane containing General Ceramics S-1 cores. The planes were tested in Memory Test Setup VI where they were subjected to a number of different information patterns, and relevant margins were recorded. The graphs at the end of this report show plots of sense-amplifier bias voltage vs. strobe time for three different patterns, and sense-amplifier bias voltage vs. X and Y currents for one pattern. In addition, the output of the sense winding was observed when the plane contained the "worst" pattern. The sense amplifier used for these tests is a linear amplifier with a gain of approximately 140. All tests were made with no post-write disturb pulse.

Graphs I, II, and III show the sense-amplifier bias voltage vs. strobe time for three different values of driving currents, 350 ma, 400 ma, and 450 ma when the planes contain all ONEs and all ZEROs. Graphs IV, V, and VI show sense-amplifier bias voltage vs. strobe time for three different values of driving current, 350 ma, 400 ma, and 440 ma, when the plane contained the complemented checkerboard pattern with ONEs in the corner. It should be noted that when the driving currents were increased to 445 ma, the DCL plane would not hold the complemented checkerboard; the DCL cores became "disturb sensitive" at this point. The S-1 cores do not become disturb sensitive until the driving currents are over 475 ma.

Graphs A-61151 and A-61152 show a plot of sense-amplifier bias voltage vs. X and Y driving currents for three different values of Inhibit current. During these tests, the strobe time was held constant.

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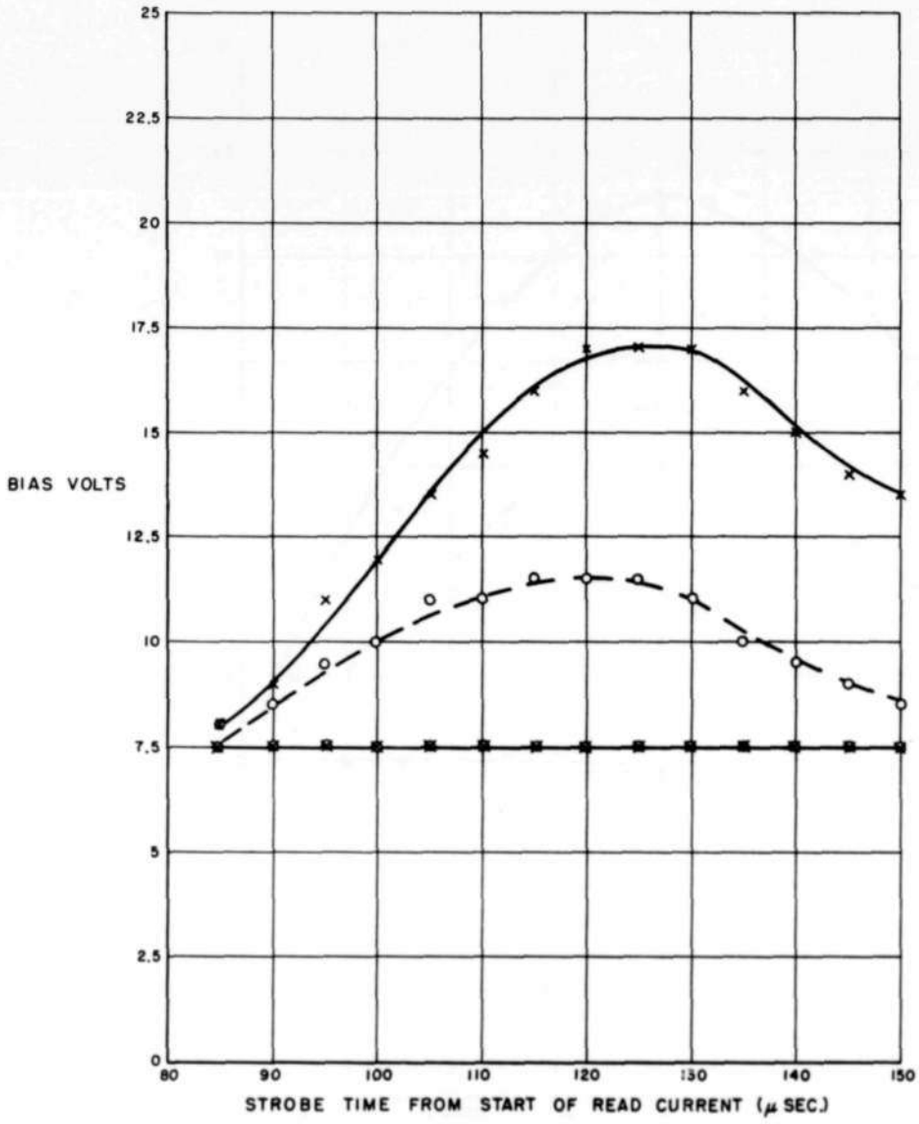
The sense-amplifier output was observed when the cores on the selected row and column contained the checkerboard pattern where the half-selected ONEs were Write-disturbed and the half-selected ZEROs were Read-disturbed. The polarity of "delta" (the difference voltage between the half-selected outputs) was such that it reduced the magnitude of the desired signal when the selected core contained a ONE, and increased the size of a ZERO signal; this ONE-ZERO ratio is the "worst" signal-to-noise situation that we know how to generate at this time. The observation showed that while the ZEROs were about equal, the ONESs from the DCL plane were about 50% larger than those from the S-1 plane.

The test results show that the DCL-2-720 core has a significantly better signal-to-noise ratio than the General Ceramics S-1 core.

Signed: J. L. Mitchell
J. L. Mitchell

JLM/dg

Attachments:
Drawing B-61702
Drawing B-61703
Drawing B-61704
Drawing B-61705
Drawing B-61706
Drawing B-61707
Drawing A-61151-1
Drawing A-61152-1

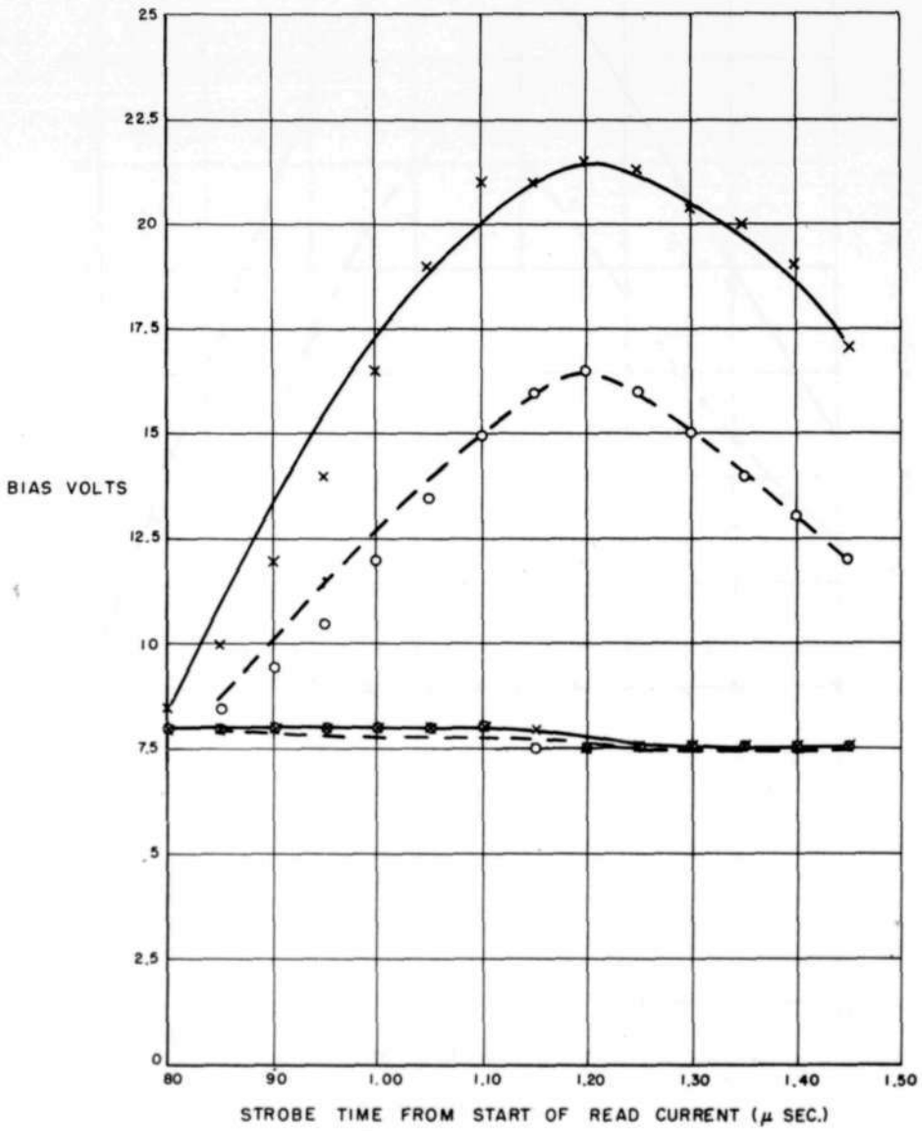


PLANE C-26 (DCL-2-720) ————
PLANE C-7 (MTC) — — — —
PATTERN: ONES & ZEROS

X,Y, AND INHIBIT CURRENTS = 350ma
NO POST WRITE DISTURB
TEMP. 70° F

B-61702

BIAS VOLTS vs. STROBE TIME (GRAPH I)

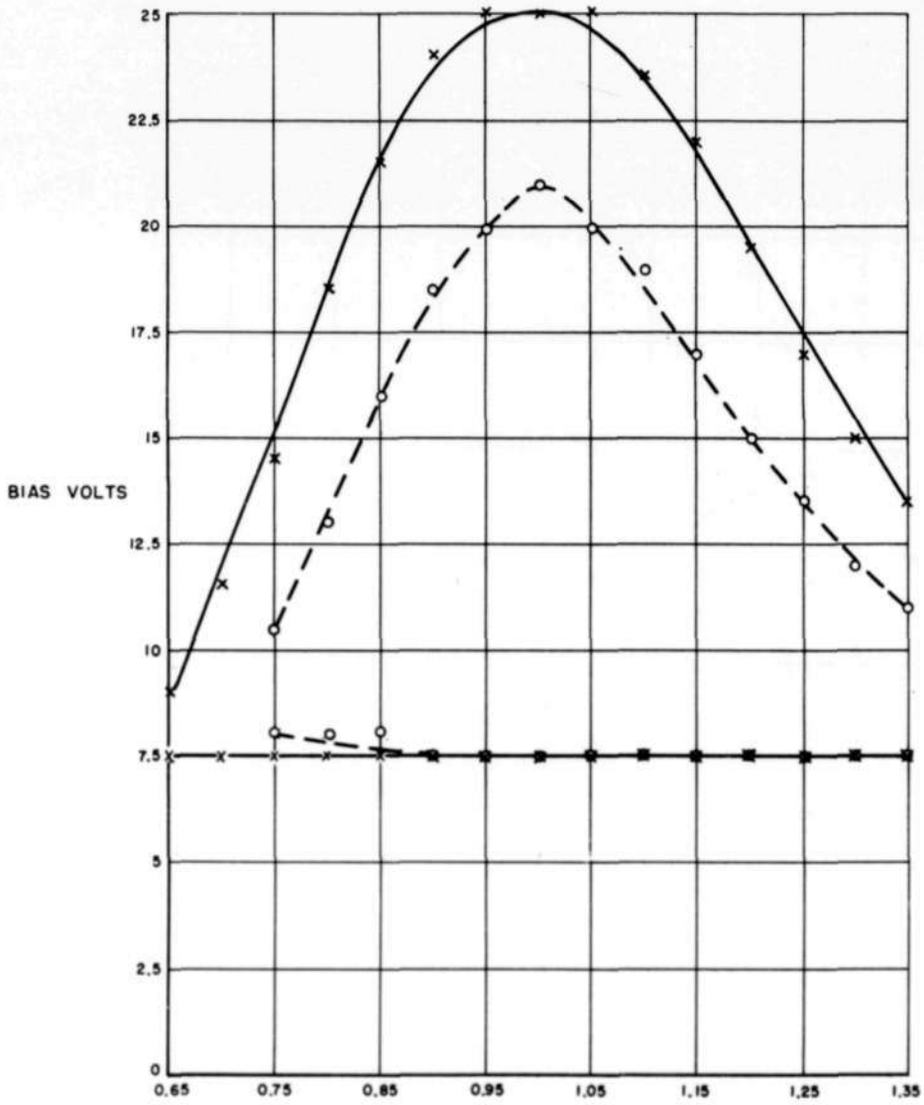


PLANE C-26 (DCL-2-720) ————
PLANE C-7 (MTC) — — — —
PATTERN: ONES & ZEROS

X, Y, AND INHIBIT CURRENTS = 400ma
NO POST WRITE DISTURB
TEMP. VARIATION: 70°F, 74°F

B-61703

BIAS VOLTS vs. STROBE TIME (GRAPH II)

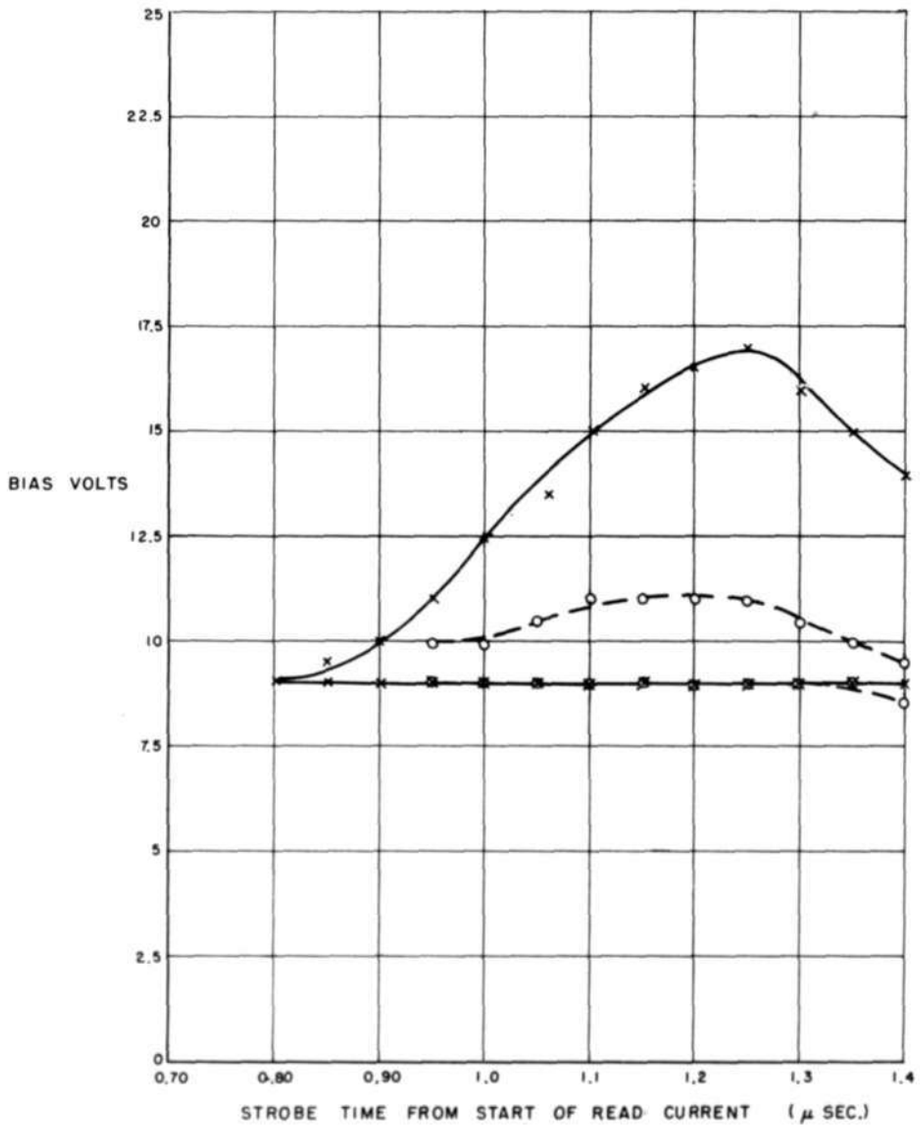


PLANE C-26 (DCL-2-720) ————
PLANE C-7 (MTC) — — — —
PATTERN: ONES & ZEROS

X, Y, AND INHIBIT CURRENTS = 450ma
NO POST WRITE DISTURB
TEMP. 70° F

8-61704

BIAS VOLTS vs. STROBE TIME (GRAPH III)

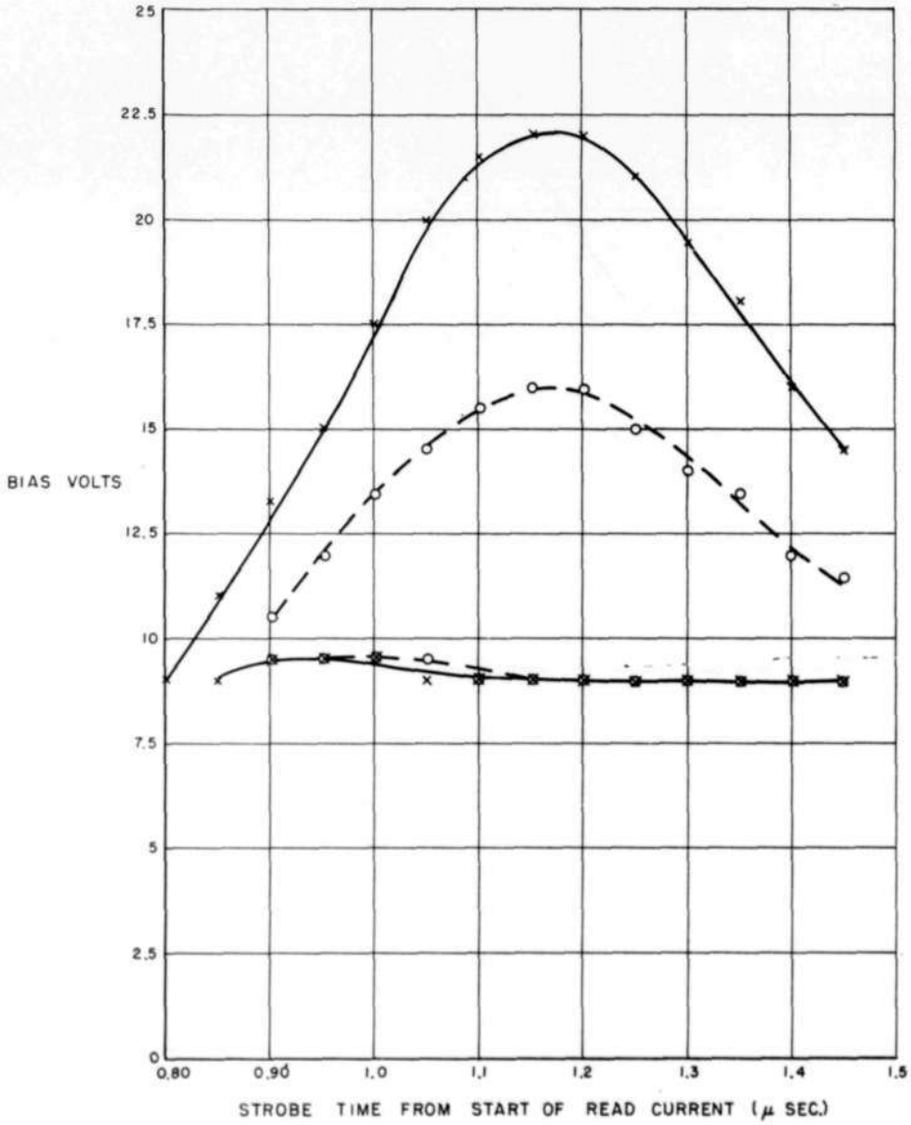


PLANE C-26 (DCL - 2 - 720) ——————
PLANE C-7 (MTC) — — — —
PATTERN: COMPLEMENTED CHECKERBOARD
"ONES" IN CORNER

X, Y, AND INHIBIT CURRENTS = 350 ma
NO POST WRITE DISTURB
TEMP. 70° F

B-61705

BIAS VOLTS vs. STROBE TIME (GRAPH IV)

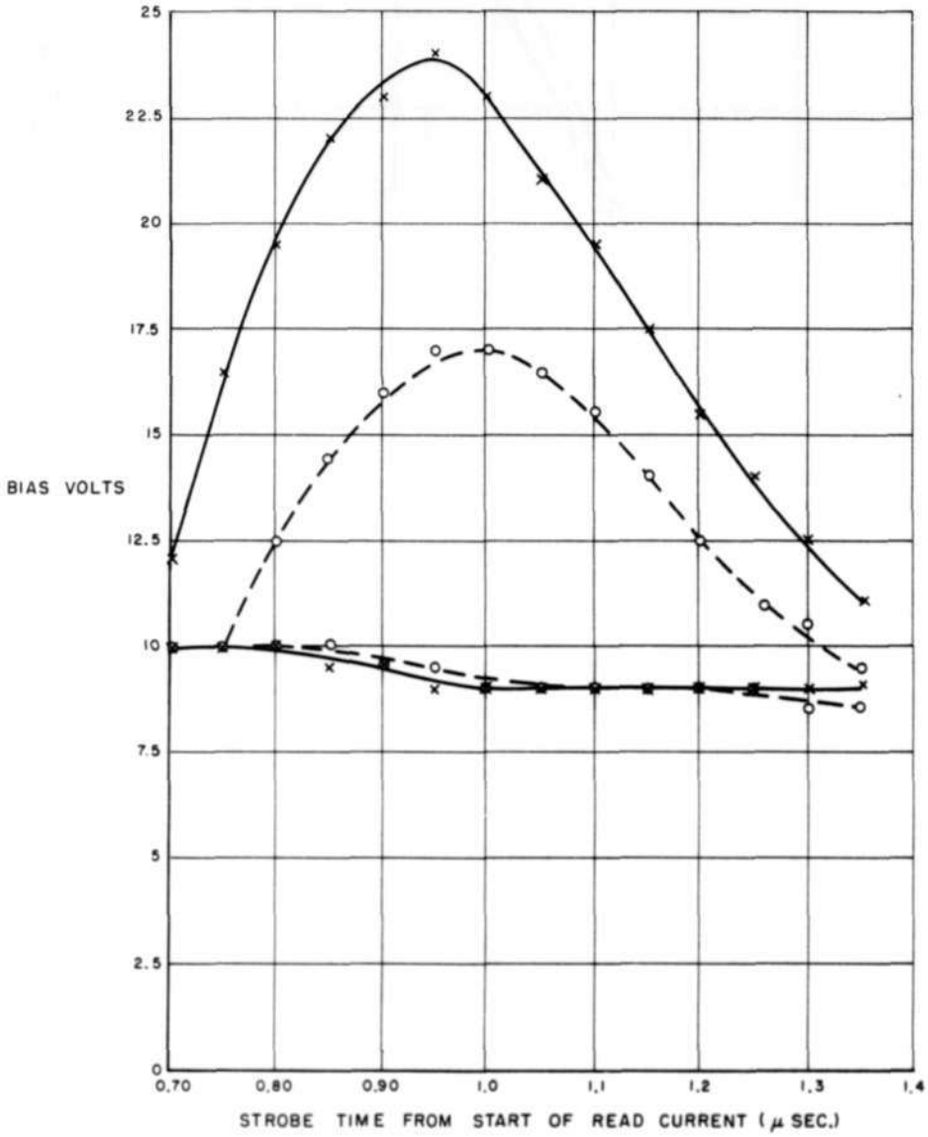


PLANE C-26 (DCL-2-720) ————
PLANE C-7 (MTC) — — — —
PATTERN: COMPLEMENTED CHECKERBOARD
"ONES" IN CORNER

X, Y, AND INHIBIT CURRENTS = 400ma
NO POST WRITE DISTURB
TEMP. 70°F

B-61706

BIAS VOLTS vs. STROBE TIME (GRAPH V)



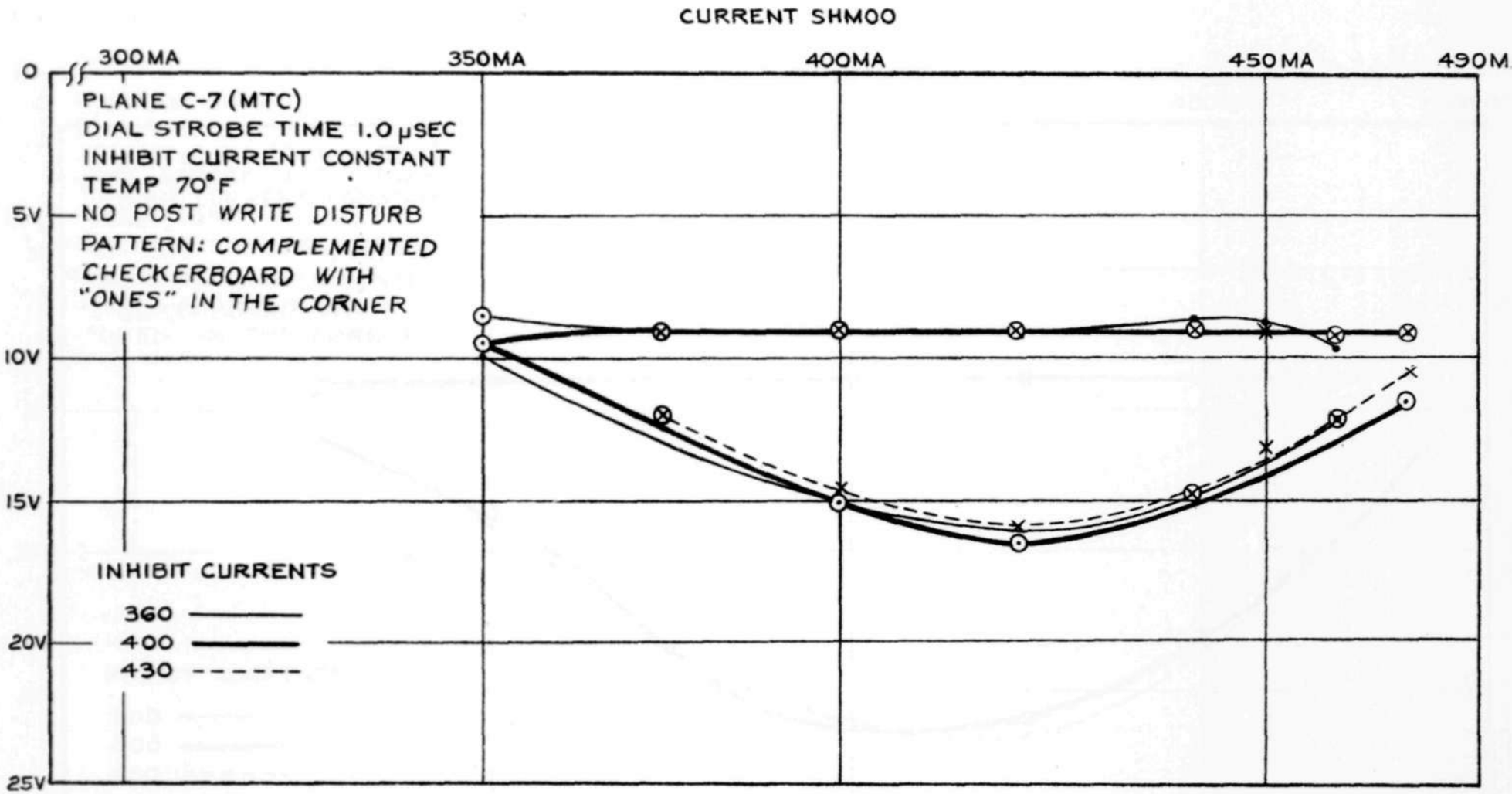
PLANE C-26 (DCL - 2 - 720) ————
PLANE C-7 (MTC) — — — —
PATTERN: COMPLEMENTED CHECKERBOARD
"ONES" IN CORNER

X, Y, AND INHIBIT CURRENTS = 440 ma
NO POST WRITE DISTURB
TEMP. 70°F

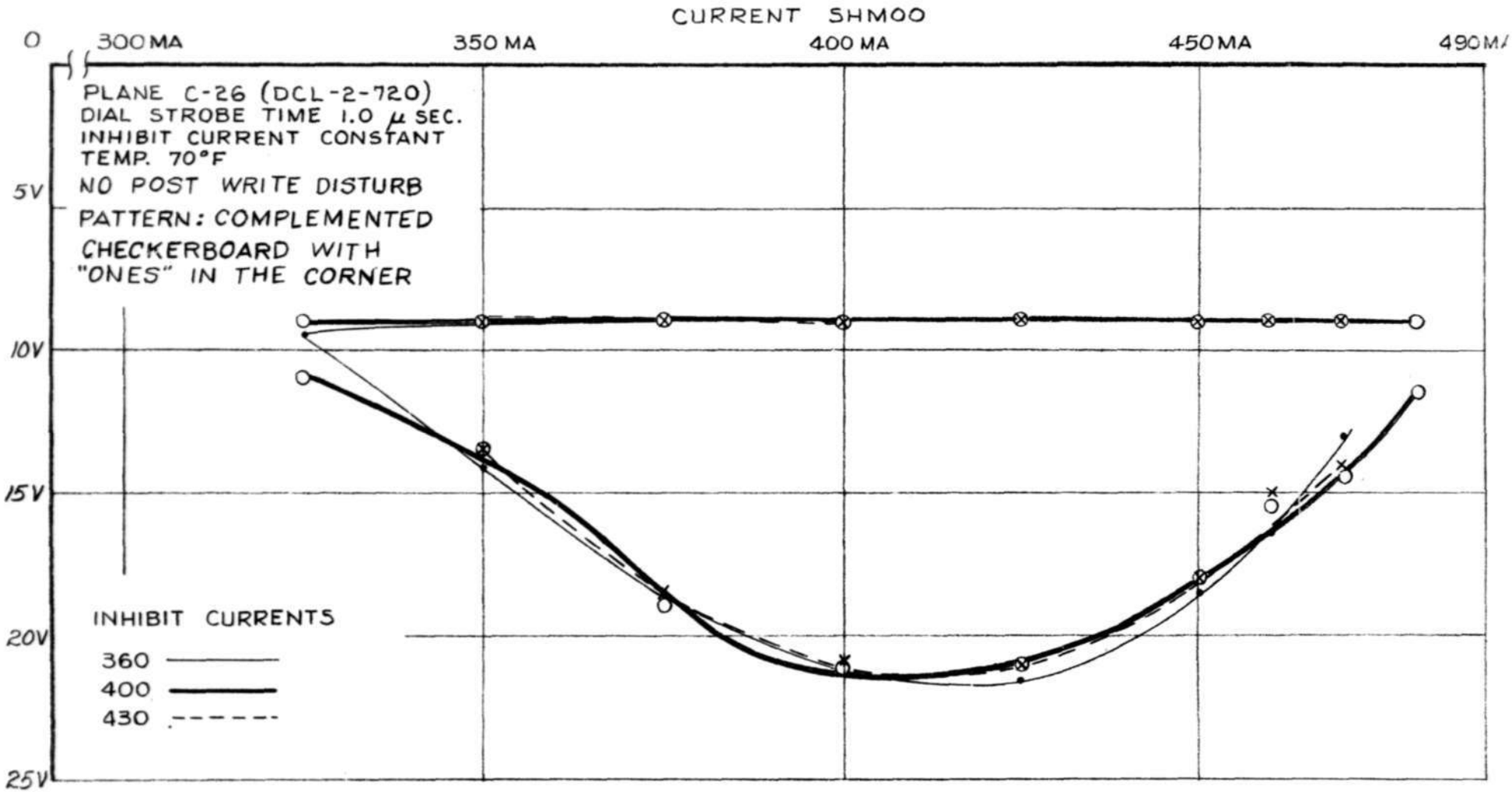
8-61707

BIAS VOLTS vs, STROBE TIME (GRAPH VI)

A-61151-1



BIAS VOLTS vs DRIVING CURRENTS
PLANE C-7 (MTC)



BIAS VOLTS vs. DRIVING CURRENTS
PLANE C-26 (DCL-2-720)