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 Massachusetts Institute of Technology
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SUBJECT: SPECIFICATIONS FOR THE CENTRAL COMPUTER SYSTEM FOR THE AN/FSQ-7

To: Jay W. Forrester

From: P. R. Bagley

Date: 28 January 1955

Approved: S. H. Dodd/mc
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Abstract: A series of documents is being prepared, giving the current status of specifications for the AN/FSQ-7. These documents, of which this is one, list the AN/FSQ-7 specifications as recommended by Lincoln Laboratory as a basis for definitizing the first production contract. In addition to the specifications as now known, these documents call attention to any presently anticipated changes which will be required and indicate the urgency of these changes.

This memorandum lists the IBM specification documents and Lincoln Laboratory M-notes which describe under the following sections, the AN/FSQ-7 Central Computer System:

<u>Index:</u>	<u>Section</u>	<u>Subject</u>
	0.0	Introduction
	1.0	Memory Element
	2.0	Arithmetic Element
	3.0	Program Element
	4.0	Instruction Control Element
	5.0	Selection and Input Output Control Element
	6.0	Test Memory
	7.0	Magnetic Tape Units, Adapter and Power
	8.0	Instruction Code
	9.0	Card Machines
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0.0 INTRODUCTION

Each of the remaining sections of this report, indicated by whole numbers such as 1.0, 2.0, 3.0, etc., deal with major areas of the AN/FSQ-7. Each section is organized in the same manner. The subsections of this introduction are organized in this standard form and explain the

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organization of and the reasons for the contents of similar subsections of the remaining sections.

The expression "concurrence" is used to signify that specifications have received written acceptance of technical design by the Lincoln Laboratory Division 6 Systems Office and the IBM Project High Duplex Planning Group. Some documents listed have not received concurrence but will be studied and concurred on as soon as possible. This formal technical review may occasionally reveal necessary design changes.

"Release" indicates that a Technical Information Release (TIR) has been distributed to indicate Lincoln approval with attached qualification, if any, and recommended action to be taken. A document may be released, with the degree of agreement explained, even if it has not received concurrence.

0.1 Specifications

The specifications listed under this subsection describe the AN/FSQ-7 as recommended by Lincoln Laboratory as a basis for the preparation of the initial production contract so that the production program can proceed on the schedule established by the Air Force.

0.2 Presently Anticipated "Class A" Changes

A "Class A" change is defined as one which must be made before the equipment will be suitable for its air defense function. If such a change is now foreseen in these specifications of the preceding subsection but is not well enough defined to be now included in the specifications, it will be discussed in ().2 subsection.

0.3 Presently Anticipated "Class BR" Changes

Changes discussed in this subsection are considered ultimately necessary in all machines. The AN/FSQ-7 can be used for air defense work without them, but they should be introduced as soon as possible without adversely affecting delivery schedules.

0.4 Presently Anticipated "Class B" Changes

"Class B" changes are desirable changes to facilitate the air defense function of the AN/FSQ-7. They should be incorporated in the production program as soon as possible without adversely affecting delivery schedules, but Lincoln currently feels that they need not be retrofitted into all previous machines.

0.5 Comments

This subsection includes additional information concerning the specifications.

1.0 MEMORY ELEMENT

1.1 Specifications

IBM document IM-97 (IBM file number D-14), Memory Element for the AN/FSQ-7 Production System, dated 12 July 1954 with corrections dated 20 July 1954 is a complete specification. Concurrence was reached in a letter (IBM file number D-14) dated 22 July 1954 on IM-97 with corrections. Release of the specifications was held up pending reconsideration of the memory cycle time. Lincoln felt that the memory cycle time must be shortened to 6 microseconds. At Project High Coordination Meeting No. 3, on 22 December 1954, (see meeting minutes) it was agreed that 6.5 μ sec would be acceptable for the first production machine, and that 6.0 μ sec would be the design objective; IBM will make a proposal for phasing any changes necessary to achieve a 6.0 μ sec memory cycle into production and introducing them on a retrofit basis.

1.2 Presently Anticipated "Class A" Changes

None

1.3 Presently Anticipated "Class BR" Changes

Any computers shipped with memory cycle times greater than 6.0 microseconds shall be retrofitted to operate at 6.0 microseconds.

1.4 Presently Anticipated "Class B" Changes

None

1.5 Comments

Division 6 document M-2904, Proposed Changes in FSQ-7 Memory, dated 13 July 1954, recommending changes in circuitry and mechanical design, was discussed at the concurrence meeting on 23 July 1954. These changes were not to be a part of the specification, but the IBM personnel present (Astrahan, Edwards, D. C. Ross, and Wittenberg) agreed that they would be considered as time permitted. A review of these recommendations will be initiated by June 1955 by the Lincoln Division 6 Systems Office in order to incorporate prototype experience.

Refer to Section 2.0 for related material on the parity checking circuits.

2.0 ARITHMETIC ELEMENT

2.1 Specifications

The Arithmetic Element specifications are contained in IBM file D-6 in IBM document IM-95, Specifications of the Arithmetic Element for the AN/FSQ-7 Production System, dated 29 June 1954, amended and concurred

on by a concurrence letter (IBM file D-6) dated 20 July 1954. These documents were released by TIR 1-35, dated 20 October 1954.

2.2 Presently Anticipated "Class A" Changes

None

2.3 Presently Anticipated "Class BR" Changes

IBM document, Parity Circuits of the XD-1, by Kurkjian and MacDonald, dated 20 September 1954 proposes, for the prototype machines, changes in the parity circuits to avoid alteration of erroneous parity bits. The changes are covered in detail in IBM document, XD-1 Parity Count and Parity Check Controls, by Kurkjian and MacDonald dated 21 September 1954. If not incorporated initially, these changes should be made as soon as present delivery schedules permit.

2.4 Presently Anticipated "Class B" Changes

None

2.5 Comments

IBM document D-22 referring to the mechanical clock originally specified for the Arithmetic Element has been eliminated by concurrence letter D-22-1 dated 22 December 1954 and rescinded by TIR 1-55 dated 22 December 1954.

Refer to Section 6.0 for related material concerning moving Test Memory Plugboard from the Arithmetic Frame to the Maintenance Console.

The changes in the parity circuits (see Section 2.3 above) proposed by Kurkjian and MacDonald do not, however, rectify all the existing deficiencies. The parity circuits do not "fail safe" (the absence of a pulse indicates an even parity), a parity error, a parity error cannot be programmed, and under some conditions of "cyclic program control" parity generation does not work at all and so wrong parities are stored (when the computer is stopped between TP 2 and 3 of a break in or an OT B cycle). Maintenance might be hampered until these conditions are corrected, and some consideration should be given to them. No documented studies or solutions of these problems have yet been made. The IBM System Planning Group should undertake an investigation of these items.

3.0 PROGRAM ELEMENT

3.1 Specifications

The specifications are covered in IBM document IM-94, Program Element for AN/FSQ-7 Production System, dated 28 June 1954 (IBM file

number D-5) as amended and concurred on by a letter Program Element, Duplex Central dated 13 July 1954 (IBM file number D-5). These documents were released by TIR 1-37, dated 4 October 1954.

An additional document, Proposal for Change in "Control Clear" for AN/FSQ-7 Production System, dated 4 November 1954 (IBM file number D-42) received concurrence in a letter dated 4 January 1955 (IBM file number D-42).

Verbal agreement exists between D. C. Ross, M. M. Astrahan, and B. E. Morriss that four Index Registers will be provided in the Program Element; hence the specifications need to be revised accordingly. IBM plans to issue a concurrence letter by 7 February 1955 covering this revision.

3.2 Presently Anticipated "Class A" Changes

None

3.3 Presently Anticipated "Class BR" Changes

None

3.4 Presently Anticipated "Class B" Changes

None

3.5 Comments

IBM document, Use of Compare Circuits for "Arithmetic Compare," dated 22 September 1954 (IBM file number D-41) has been offered by IBM for concurrence. Lincoln feels that the proposed changes are desirable but not necessary, and that the decision to make them be left to IBM, with the reservation that if the change is made in the prototypes, it should be made in the production machine.

4.0 INSTRUCTION CONTROL ELEMENT

4.1 Specifications

The principle specifications are contained in IBM document TR-15, Instruction Control Frame, dated 17 February 1954, as amended by Concurrence on Instruction Control Frame, Production System, dated 12 October 1954 (IBM file number D-15) and by three items entitled Automatic Branch on Alarms, dated 9 August 1954, 11 August 1954, and 31 August 1954 (IBM file number D-21). These specifications also received concurrence in documents cited above and were released by TIR 1-44, dated 17 November 1954.

An additional document, Proposal for Automatic "Branch to Zero" under Switch Control, by R. M. Douglas, dated 12 November 1954

(IBM file number D-45) received concurrence in a letter dated 4 January 1955 (IBM file number D-45).

4.2 Presently Anticipated "Class A" Changes

None

4.3 Presently Anticipated "Class BR" Changes

None

4.4 Presently Anticipated "Class B" Changes

None

4.5 Comments

A proposal to revise cyclic program control to correctly interpret the instruction HLT was made by R. M. Douglas in an IBM document, Cyclic Program Control, dated 1 September 1954. Lincoln has no strong convictions regarding this proposed change, excepting that if it is included in the prototypes it should be also be in the production machines.

5.0 SELECTION AND INPUT-OUTPUT CONTROL

5.1 Specifications

The specifications for Selection and Input-Output Control are covered in the following documents:

- a. IBM document TR-24, Selection and Input-Output Control Specifications, dated 4 May 1954, as amended by two items dated 19 July 1954 and 31 Aug. 1954, is covered by a concurrence letter dated 31 Aug. 1954 (the preceding documents bear IBM file number D-19) and was released by TIR 1-36 dated 4 November 1954.
- b. IBM document, Proposal to Operation I-0 Interlock for the AN/FSQ-7 Production System, dated 26 October 1954 (IBM file number D-37) received concurrence in a letter (IBM file number D-37), dated 5 November 1954.
- c. IBM document, Marginal Checking of Intercommunication Sense and Operate Circuits, Production Machine, dated 5 November 1954 is covered by a concurrence letter dated 4 January 1955 (both documents bear IBM file number D-43).

5.2 Presently Anticipated "Class A" Changes

None

5.3 Presently Anticipated "Class BR" Changes

None

5.4 Presently Anticipated "Class B" Changes

None

5.5 Comments

Refer to Section 2.5 above for a discussion on parity circuits which may affect Selection and In-Out Control.

6.0 TEST MEMORY

6.1 Specifications

The specifications for Test Memory are briefly covered in two IBM documents, IM-95 (see citation in Section 2.1) and Specifications for the Duplex Maintenance Console of an AN/FSQ-7 Production System (IBM File number D-32) discussed in Section 2.1 of Lincoln Memorandum, 6M-3300. IBM document IM-79, Proposal for Test Memory, dated 17 March 1954 is satisfactory as a more detailed specification. IM-79 has not been concurred upon.

6.2 Presently Anticipated "Class A" Changes

None

6.3 Presently Anticipated "Class BR" Changes

None

6.4 Presently Anticipated "Class B" Changes

According to concurrence letter, Arithmetic Frames, Duplex Central, dated 20 July 1954, (IBM file number D-6) IBM will give consideration to locating the Test Memory plugboard on the maintenance console when the development schedule permits. If this change is not included in the first production machine, Lincoln considers that it is satisfactory to make the change a "Class B" change.

6.5 Comments

None

7.0 MAGNETIC TAPE UNITS

7.1 Specifications

IBM document, Magnetic Tape Proposal for AN/FSQ-7 Production

System, dated 2 July 1954, was amended and concurred on by a letter dated 8 July 1954 (both documents bearing IBM file number D-4).

An IBM document, dated 15 December 1954 (IBM file number D-4-1), requests concurrence on a change in the method of switching of tape select lines at the tape drive units. Lincoln agrees that the proposed change is adequate but recommends that consideration be given to the addition of an indicator light on the maintenance console. It indicates if any tape units are connected to other than normal selection lines (see Section 7.3).

7.2 Presently Anticipated "Class A" Changes

None

7.3 Presently Anticipated "Class BR" Changes

Lincoln feels strongly that a light should be provided on the maintenance console to indicate when any tape unit is not connected to its preassigned (or "normal") address. If this feature is not included in all machines before delivery, it should be retrofitted.

7.4 Presently Anticipated "Class B" Changes

None

7.5 Comments

A proposed redesign of the circuits of the tape equipment to use AN/FSQ-7 basic circuits, eliminate the need for a separate power supply, and incorporate the magnetic tape units in the marginal system was submitted for concurrence. IBM requested that these changes not be incorporated in initial machines. The redesign proposal was rejected with the understanding that it would be reconsidered after the tape units for XD-1 had been completed.

8.0 INSTRUCTION CODE

8.1 Specifications

The instruction codes for the duplex are contained in IBM document PM-8-5, Programmers Reference Manual: Instructions, as amended by two items dated 19 July 1954 and 31 July 1954. These documents are covered by a concurrence letter D-16 dated 31 Aug. 1954 (all the documents cited bearing IBM file number D-16). TIR 1-34 dated 20 October 1954 releases these documents.

IBM document, Perselbsn Codes, dated 1 December 1954, (IBM file number D-16-1) delineates corrections to codes made necessary by other changes in the machine which are already concurred upon; hence, concurrence on this document is a necessary formality.

8.2 Presently Anticipated "Class A" Changes

None

8.3 Presently Anticipated "Class BR" Changes

After substantial programming experience has been achieved on the prototype, it is expected that the instruction code will be subjected to a thorough review and that proposals for changes will be considered at that time.

8.4 Presently Anticipated "Class B" Changes

None

8.5 Comments

None

9.0 MAINTENANCE AREA CARD MACHINES

9.1 Specifications

IBM document, Card Reader, Printer, and Punch Specification for AN/FSQ-7 Production System, dated 6 July 1954 (IBM file number D-12) represents the specifications for the three card machines to be located in the maintenance area; namely, the 713 Card Reader, the 718 Printer, and the 723 Card Punch. Concurrence on this document is given in a letter dated 20 July 1954 (IBM file number D-12) and release by TIR 1-38, dated 4 November 1954.

9.2 Presently Anticipated "Class A" Changes

None

9.3 Presently Anticipated "Class BR" Changes

None

9.4 Presently Anticipated "Class B" Changes

None

9.5 Comments

None

SIGNED:

Philip R. Bagley
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PRB:FJE

Attachment: Reference List

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

Memorandum 6M-3291

REFERENCE LIST

IBM DOCUMENTS

IBM File No.	Document	Lincoln Laboratory Div. 6 Document Room No.
D-14	<u>IM-97, Memory Element for AN/FSQ-7 Production System</u> dated 12 July 1954.	6DR-10
D-14	Corrections to IM-97, dated 20 July 1954.	6DR-11
D-14	Concurrence on IM-97 letter dated 22 July 1954.	6DR-12
	Minutes of Project High Coordination Meeting No. 3 of 22 Dec. 1954.	6DR-13
D-6	<u>IM-95, Specifications of the Arithmetic Element for the AN/FSQ-7 Production System</u> dated 29 June 1954.	6DR-14
D-6	Concurrence letter on IM-95 dated 20 July 1954.	6DR-15
	<u>Parity Circuits of the XD-1, by Kurkjian and MacDonald</u> dated 20 Sept. 1954.	6DR-16
D-22	<u>XD-1 Parity Count and Parity Check Con- trols, by Kurkjian and MacDonald</u> dated 21 September 1954.	6DR-17
D-22	Document referring to Mechanical Clock originally specified for the Arithmetic Element.	6DR-18
D-22-1	Concurrence letter dated 22 December 1954 rescinding requirement for the Mechanical Clock in the Arithmetic Element	6DR-19
D-5	<u>IM-94 Program Element for AN/FSQ-7 Production System</u> dated 28 June 1954.	6DR-20

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IBM File No.	Document	Lincoln Laboratory Div. 6 Document Room No.
D-5	<u>Concurrence letter Program Element, Duplex Central dated 13 July 1954.</u>	6DR-21
D-42	<u>Proposal for Change in 'Control Clear' For AN/FSQ-7 Production System dated 4 November 1954.</u>	6DR-22
D-41	<u>Use of Compare Circuits for "Arithmetic Compare" dated 22 September 1954.</u>	6DR-24
D-42	Concurrence letter dated 4 January 1955.	6DR-23
D-15	<u>TR-15 Instruction Control Frame dated 17 February 1954.</u>	6DR-25
D-15	<u>Concurrence on Instruction Control Frame, Production System, dated 12 October 1954.</u>	6DR-26
D-21	<u>Automatic Branch on Alarms, dated 9 August 1954.</u>	6DR-27
D-21	<u>Automatic Branch on Alarms, dated 11 August 1954.</u>	6DR-28
D-21	<u>Automatic Branch on Alarms, dated 31 August 1954.</u>	6DR-29
D-45	<u>Proposal for Automatic "Branch to Zero" Under Switch Control, by R.M. Douglas, dated 12 Nov. 1954.</u>	6DR-30
D-45	Concurrence letter dated 4 January 1955.	6DR-31
	<u>Cyclic Program Control dated 1 September 1954 by R.M. Douglas.</u>	6DR-32
D-19	<u>TR-24 Selection and Input-Output Control Specifications dated 4 May 1954.</u>	6DR-33
D-19	Amendments to TR-24 dated 19 July 1954.	6DR-34

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IBM File No.	Document	Lincoln Laboratory Div. 6 Document Room No.
D-19	<u>Amendments to TR-24 dated 31 Aug. 1954.</u>	6DR-35
D-37	<u>Proposal to Operate I-O Interlock for the AN/FSQ-7 Production System dated 26 Oct. 1954.</u>	6DR-36
D-37	Concurrence letter dated 5 Nov. 1954.	6DR-37
D-43	<u>Marginal Checking of Intercomm. Sense and Operate Circuits, Production Machine, dated 5 Nov. 1954.</u>	6DR-38
D-43	Concurrence letter dated 4 January 1955.	6DR-39
D-32	<u>Specifications for the Duplex Maintenance Console of an AN/FSQ-7 Production System.</u>	6DR-40
	<u>IM-79 Proposal for Test Memory dated 17 March 1954.</u>	6DR-41
D-6	<u>Concurrence letter Arithmetic Frames, Duplex Central dated 20 July 1954.</u>	6DR-42
D-4	<u>Magnetic Tape Proposal for AN/FSQ-7 Production System dated 2 July 1954.</u>	6DR-43
D-4	Concurrence letter dated 8 July 1954.	6DR-44
D-4-1	IBM document dated 15 December 1954.	6DR-45
D-16	<u>PM-8-5 Programmers Reference Manual: Instructions.</u>	6DR-46
D-16	Amendments to PM-8-5 dated 19 July 1954.	6DR-47
D-16	Amendments to PM-8-5 dated 31 July 1954.	6DR-48
D-16	Concurrence letter dated 31 Aug. 1954.	6DR-49
D-16-1	<u>PERSELBSN Codes dated 1 December 1954.</u>	6DR-50
D-12	<u>Card Recider, Printer, and Punch Specification for AN/FSQ-7 Production System dated 6 July 1954.</u>	6DR-51

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Memorandum 6M-3291

IBM File No.

Document

Lincoln Laboratory
Div. 6 Document
Room No.

D-12

Concurrence Letter dated 20 July 1954.

6DR-52

LINCOLN LABORATORY DOCUMENTS

Document

M- Number or
Div. 6 D.R. No.

Proposed Changed in FSQ-7 Memory
dated 13 July 1954.

M - 2904