APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



Sydney Bradspies

April 6, 1954

## MASTER'S THESIS PROPOSAL

**TITLE:** A Magnetic-Core Memory With External Selection

### BRIEF STATEMENT OF THE PROBLEM

The purpose of this thesis investigation is to design, build, and evaluate the operation of a magnetic-core memory in which selection is external to the actual memory cores.

### HISTORY OF THE PROBLEM:

For several years the Digital Computer Laboratory at MIT has worked on the problems of storing binary information in a three-dimensional magnetic-core memory.[1,2] In the course of these studies, it was found that the major requirement for the cores to be used is that they have rectangular hysteresis loops (Fig. 1).

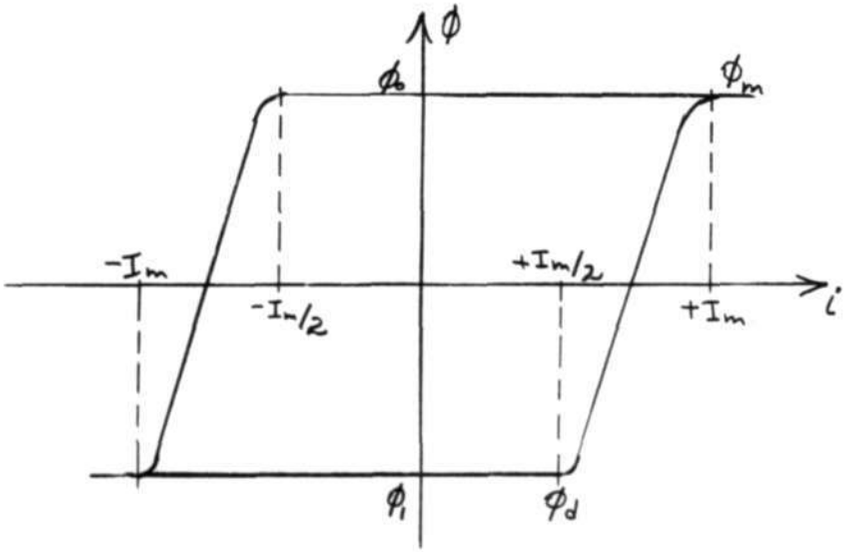


Fig. 1 A typical hysteresis loop for a magnetic-memory core

When there is no current driving a core, with such a hysteresis loop, it is in equilibrium at point $\phi_1$ or at point $\phi_0$, depending upon its previous history. By convention, the flux position $\phi_0$ is called ZERO, and $\phi_1$ is called ONE.

---

[1, 2] Superscripts refer to similarly numbered items in the Bibliography.

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



A simple 9-core (3 x 3) portion of a large memory plane (Fig. 2) clarifies operation of the coincident-current magnetic memory.

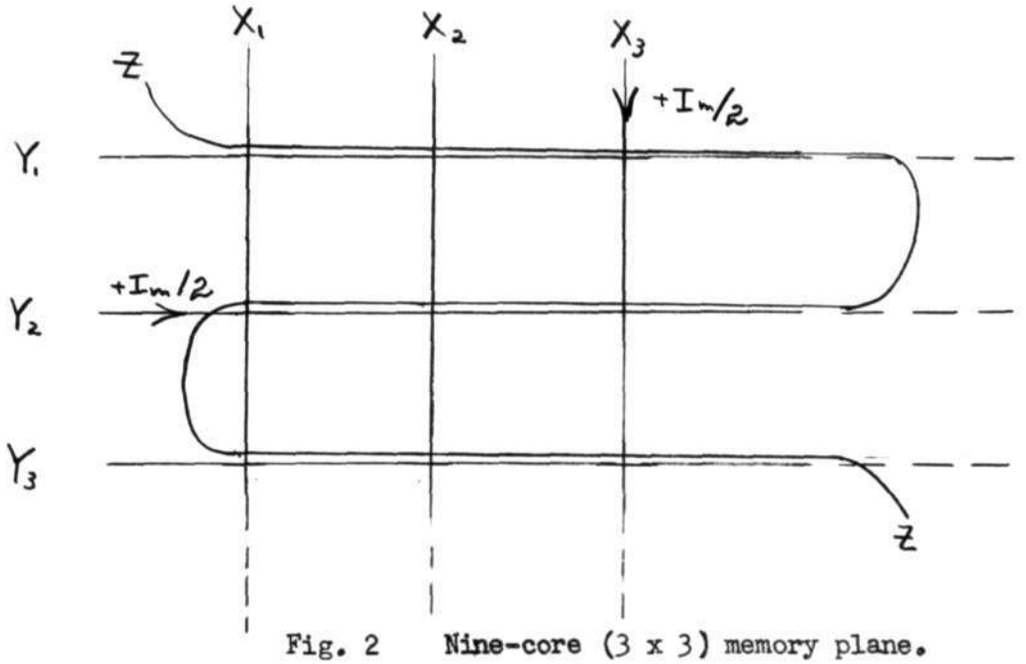


Fig. 2 Nine-core (3 x 3) memory plane.

At the intersection of each X and Y line there is a magnetic core. Both a Z (inhibiting winding used for writing ZEROS) winding and a sensing winding (used for reading out of the memory, and not shown so as to prevent confusion in the diagram) are threaded through each core.

The "read" operation passes $+I_m/2$ through the selected X and Y co-ordinates, exciting the selected core by $+I_m$. If the core holds a ONE, its flux state is reversed, and a large voltage is induced in the sensing winding. If, on the other hand, the core holds a ZERO, there is a relatively small change of flux in the core, and little voltage is induced, provided that the ratio $\phi_0/\phi_m \cong 1$ (Fig. 1). The read operation is destructive; that is, when reading has been accomplished, the core holds a ZERO, regardless of its original contents.

A number of cores lie on either the selected X co-ordinate or the selected Y co-ordinate. These cores are excited by $+I_m/2$ (that is, they are half selected). At the time of the read operation the information held by these cores is of no interest; furthermore the information that they hold should not be destroyed. For these reasons, the half selected-cores should not even be partially switched. As a consequence (referring to Fig. 1), the ratio $\phi_d/\phi_1$ has to be close to unity.

These, then, are the requirements for a core in a coincident-current magnetic memory -- the ratios $\phi_0/\phi_m$ and $\phi_d/\phi_1$ must each be

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



close to unity. By symmetry $\phi_0 = -\phi_1$. Therefore these conditions may be combined and restated: $|\phi_d/\phi_m|$ must be close to unity if the memory is to operate with a minimum of output signal from half-selected cores and from the selected core (if it holds a ZERO) and with a certainty that information is not being destroyed. The ratio $|\phi_d/\phi_m|$ is called the squareness ratio,[3] and it is in general somewhat less than unity.

"Writing" is accomplished in one of the following manners:

To write a ONE, pass currents of $-I_m/2$ down the chosen X and Y co-ordinates.

To write a ZERO, pass currents of $-I_m/2$ down the chosen X and Y co-ordinates, and a current of $+I_m/2$ through the Z (inhibiting) winding.

Block diagrams of the write operations may be found in the literature.[4,5]

The core performs two functions in the coincident-current magnetic memory just described: primarily it stores information, but its rectangular hysteresis loop also provides the nonlinearity which discriminates between $I_m$ and $I_m/2$, needed for selection. Because the core must be used for selection, it must have a rectangular hysteresis loop with $|\phi_d/\phi_m| \cong 1$, and the magnitudes of the switching currents are severely limited because $I_m/2$ must not even partially select a core.

For a given switched core, the change of flux is independent of the switching time, $\tau$, and the voltage induced in the sensing winding is inversely proportional to $\tau$. Thus, shortening $\tau$ increases the output voltage and also increases the speed of the memory. It has been shown[3] that $\tau$ is inversely proportional to the exciting current. The exciting current in the present memory is limited, however, by coincident-current restrictions, significantly limiting the operating speed of the memory.

PROPOSED SCHEME:

A system that did not use the memory cores for selection would avoid the restrictions on exciting current (which could be made very large, thereby reducing $\tau$ significantly) and it would reduce rectangularity requirements on the hysteresis loop of the cores. Such a system has been proposed by J. Raffel.[6]

In this memory system, switch cores A and B (Fig. 3) are used for selection. Memory core M is used solely for retention of information. This system requires 3 cores for each bit of information as compared to 1 core in the present memory. However, the rectangularity requirements placed on these cores are far more lenient than the requirements on the present cores.

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



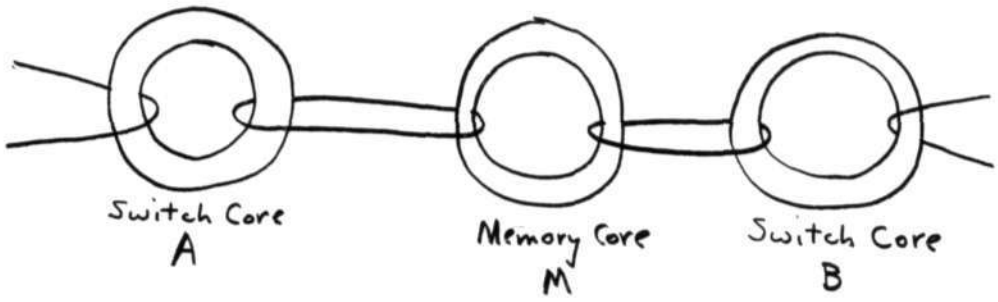


Fig. 3 Wiring necessary for one bit of information.

It is only necessary that switch cores A and B have nonlinear $\phi$-i curves (Fig. 4) and that memory core M have some remanence (Fig. 5).

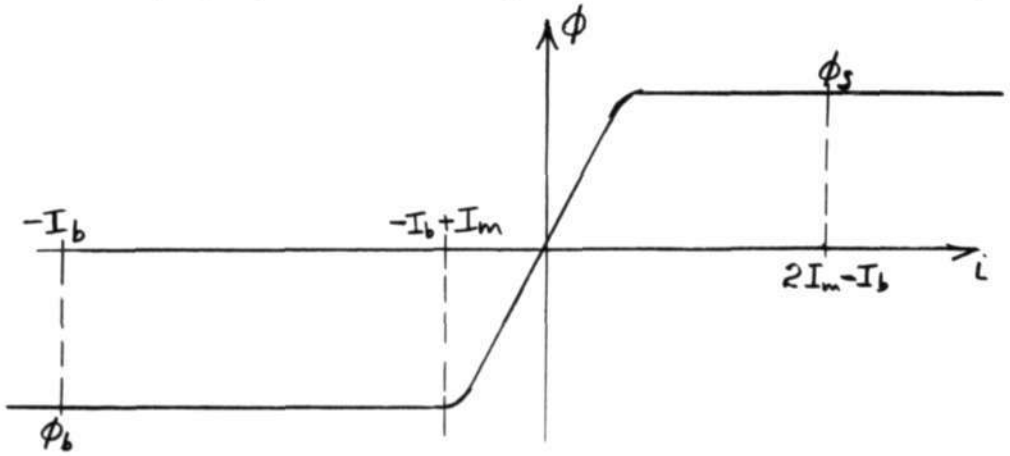


Fig. 4 Switch-core characteristics.

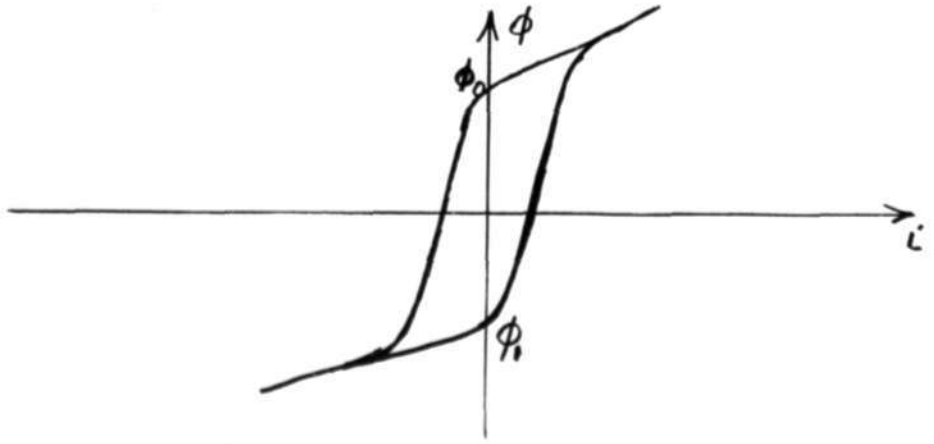


Fig. 5 Memory-core characteristics.

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



Let us now consider the operation of a 9-core (3 x 3) memory plane (Fig. 6), flanked by two 9-core switch planes.

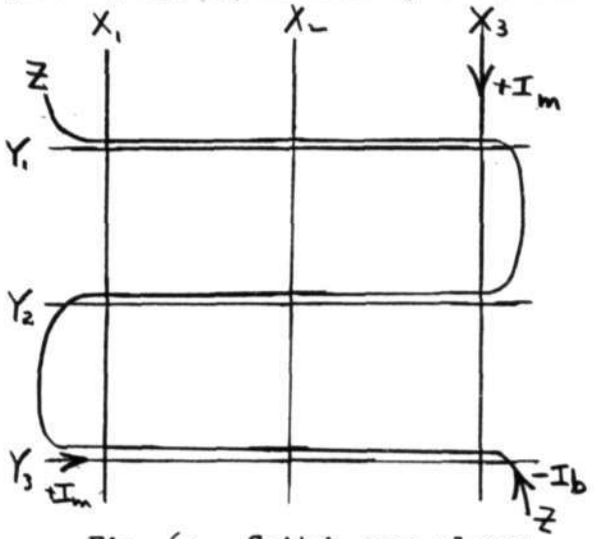


Fig. 6a. Switch-core planes (Plane A or B). Top view.

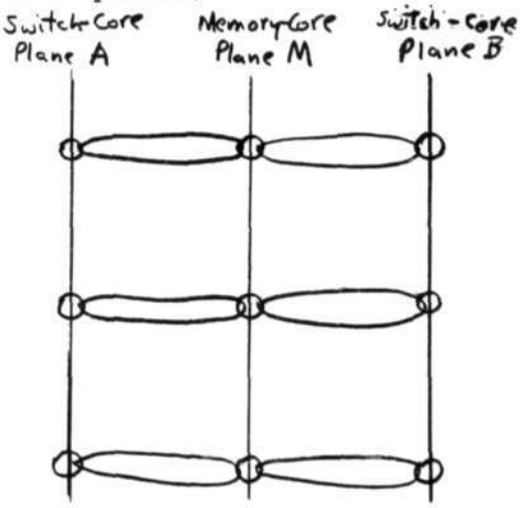


Fig. 6b. Side view of 9-bit memory

Switch-plane A is for the read operation, and switch-plane B for writing. The Z-winding (Fig. 6a) carries bias currents, $-I_b$ in plane A (Fig. 4) and $+I_b$ in plane B.

The read operation sends currents $+I_m$ along the selected X and Y co-ordinates. The selected switch core in the A plane is switched from $\phi_b$ to $\phi_s$ (Fig. 4). When the excitation of lines X and Y is stopped, switch core A reverts to $\phi_b$. The output of switch core A (Fig. 7) is coupled to the memory core M, and so the information is read out and destroyed. At the completion of the read cycle, the selected memory core holds a ONE.

If ONE is to be written in core M, switch core B is left unexcited following a reading.

If ZERO is to be written, $-I_m$ is passed along the selected X and Y co-ordinates in switch-core plane B (the Z-winding of plane B carries a bias current of $+I_b$). The output of switch core B (Fig. 8) leaves memory core M in the ZERO state.

Certain advantages may be expected from this system, in comparison to the present coincident-current-memory system:

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



Fig. 7 Read output of switch core A.

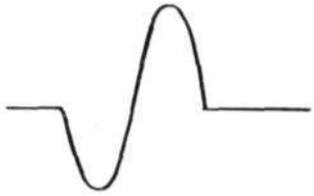

Fig. 8 Write-ZERO output of switch core B.

1. Faster switching (by an amount not yet determined) becaused the switch cores can be excited by very large currents. The only restriction is that $-I_b + I_m$ (Fig. 4) must not pass the knee of the Ø-i curve. Thus the larger $I_b$ is, the harder the core may be driven and the more rapidly it will switch.

2. Larger output ONEs because the voltage output is inversely proportional to the switching time.

3. The hysteresis-loop requirements on the various cores are relaxed as is evidenced by comparing Figs. 4 and 5 to Fig. 1.

There are, however, some disadvantages immediately obvious in the proposed system:

1. The coupling necessary between the cores of planes A, B, and M is such that difficulties in construction may be expected.

2. For a word n digits in length, at least 2n + 1 cores are required (1 A core, n B cores and n M cores). The present system requires only n cores.

## PROPOSED PROCEDURE

### 1. Determine the Magnetic Properties of Cores

Metallic and ferrite cores with various types of hysteresis loops will be tested. The operating characteristics of these cores will be determined and compared to ascertain how poor the cores may be and still be satisfactory for the proposed memory. The relative sizes of the switch and memory cores will be ascertained. Limits on core uniformity must also be determined.

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



2. Determine the Operation of the Memory

Investigations will be made into the requirements to be placed on the loop of wire coupling the memory core to the switch core. Operating characteristics will be found for various resistance values of this loop. Also to be determined is the number of times this loop should be wrapped around both the switch and memory cores.

Signal-to-noise ratios are extremely important and will be established for various schemes of wiring and for different cores.

3. Operation of Experimental Model

The switching logic for a simple 3-dimensional memory will be designed. The memory will be built and tested. Its operating characteristics -- switching time, outputs and core requirements -- will be compared to those of the present magnetic core memory.

EQUIPMENT NEEDS

The magnetic cores and the equipment necessary for testing the cores are available at the MIT Digital Computer Laboratory.

ESTIMATED DIVISION OF TIME:

| | | |
|---|---|---|
| 1. | Preparation of Proposal | 50 hours |
| 2. | Further study of Literature | 30 hours |
| 3. | Experimental Work and Analysis | 200 hours |
| 4. | Correlation of Results and Formulation of Conclusions | 50 hours |
| 5. | Preparation of Thesis Report | 70 hours |
| 6. | Total | 400 hours |

SIGNATURE AND DATE

Signed: Sydney Bradspies
Sydney Bradspies

Date: April 7, 1954

SUPERVISION AGREEMENT

I consider this material adequate for a Master's Thesis and agree to supervise and evaluate the thesis.

Approved: William K. Linvill
William K. Linvill
Associate Professor of
Electrical Engineering

SB:cs

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.



## BIBLIOGRAPHY

1. J.W. Forrester, "Digital Information Storage in Three Dimensions Using Magnetic Cores," R-187 (May 16, 1950), MIT Digital Computer Laboratory Report.

2. W.N. Papian, "A Coincident Current Memory Unit," R-192 (September 8, 1950), MIT Digital Computer Laboratory Report.

3. J.B. Goodenough, N. Menyuk, "Nucleation of Domains of Reverse Magnetization and Switching Characteristics of Magnetic Materials," E-532 (March 9, 1953) MIT Digital Computer Laboratory Engineering Note.

4. K.H. Olsen, "A Magnetic-Matrix Switch and Its Incorporation into a Coincident-Current Memory," R-211 (June 6, 1952), MIT Digital Computer Laboratory Report.

5. B. Widrowitz, "The 16 x 16 Metallic-Core Memory Array, Model I," R-216 (September 25, 1952), MIT Digital Computer Laboratory Report.

6. J. Raffel, "Core Memory Using External Bit Selection," M-2736 (March 18, 1954), MIT Digital Computer Laboratory Memorandum.