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SWITCH FOR REGISTER SELECTION
IN A MAGNETIC-CORE MEMORY

J. I. Raffel

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FOREWORD

The practicability of the magnetic core as the basic storage element in a high-speed digital computer has been established with the installation and successful operation of the banks of core storage in the WWI computer. It has long been realized that the basic functions of a memory system, storage and switching, can be performed in many different ways using cores. Some techniques for performing these functions, especially selection, are explored and analyzed in this paper.

The author is grateful to Mr. D. R. Brown for undertaking the supervision of this thesis; to Mr. W. N. Papiian for many helpful suggestions; to Mr. Jay W. Forrester; and to the Staff of Division 6, Lincoln Laboratory, without whose aid this thesis work would have been impossible.

Because it presents information of general interest, this thesis report, which has had only very limited distribution, is being issued as a Division 6 R-series report.

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SWITCH FOR REGISTER SELECTION IN A MAGNETIC-CORE MEMORY

ABSTRACT

A summary of the requirements of different systems which are realizable using memory cores and switch cores is presented. A number of different systems are analyzed to show how operating characteristics are affected by various designs.

An analysis is given of the switch core or saturable transformer as a circuit element. An equivalent circuit is derived which is valid under pulsed conditions. An experimental method for obtaining pulsed hysteresis loops simply is explained. Universal curves are presented which are useful in switch design.

A 256 register, 16 place memory, driven register-wise from a 256 position core switch is described and operating results are given. This system was operated dynamically and successfully stored all patterns of information which were tested. The system employs some innovations not believed to have been tried in previous memories such as a single non-cancelling winding for both sensing and inhibiting.

A theoretical analysis and some experimental results are given for a proposed system which would employ external register drive but which would require two memory cores per bit.

A memory system is proposed in which the memory and switching functions are completely divorced, each being performed in separate cores. This system would theoretically reduce requirements on core characteristics to a minimum.

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CHAPTER 1

INTRODUCTION

1.0 Electronic Computers

The prime function of a general-purpose high-speed digital computer is to perform many simple arithmetic operations in a short period of time. In computational applications, such as the solution of problems in the physical sciences by numerical analysis, speed is clearly desirable. In so-called real-time applications, the machine is required to process information continuously at a rate which permits its insertion in a feedback loop in which conditions change rapidly; here speed is essential.

Until recently the limiting element in computers has been the internal storage or memory. Flip-flops and gates which operate at 1 megacycle have been available for some time but until the advent of newer, faster, memory systems it has not been possible to take full advantage of these.

1.1 Memory Systems

The memory of a large-scale digital computer is generally a unit capable of storing thousands to millions of numbers in registers each of some 10 to 100 binary digits long. High-speed memories should have random access; that is, it should be possible to read out of the registers in any order. It should also be parallel; that is, all digits of a number (or "word" as it is called) enter and leave the memory simultaneously along separate channels rather than sequentially along a

single channel. It is desirable to be able to select the proper register efficiently and quickly from among the thousands or possibly millions of registers and to read out the information it holds and then write in any desired information.

A survey of the attempts to produce a suitable storage¹ element reveals a wide variety of components which have been partially successful. The most important of these is the electrostatic-storage tube. As the demand for faster, more efficient, and more reliable machines increased, however, the search for a new storage element was intensified.

1.2 The Magnetic Memory Core

In 1949 Jay W. Forrester² suggested the use of a magnetic toroid as the memory element in a computer. The system he proposed then has since been designed, developed, and constructed at the M.I.T. Digital Computer Laboratory and has supplanted the previous banks of electrostatic storage in the Whirlwind I computer. This system uses the square hysteresis loop of certain magnetic materials to partially perform the selection process and to store information, necessary operations in a computer memory. The dependence of such a memory on the proper square-loop characteristic of the core has greatly accelerated research in the field of materials for this type of work. William N. Papien in 1950³ carried on much of the initial work in testing materials and found that metallic-ribbon cores were available with sufficient rectangularity to make usable memory materials. Since that time powdered-ferrite cores have been developed which switch faster, are cheaper to fabricate, and are less sensitive to physical contact.

1) Numbered references refer to correspondingly numbered references in the bibliography.

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The coincident-current-memory system operates in the following manner. Consider an array of cores arranged in planes and oriented with respect to three orthogonal axes as shown in Fig. 1-1. Each core in the array lies at the intersection of a unique set of X, Y, and Z co-ordinates, an actual wire runs through the cores for each co-ordinate. The memory-core hysteresis loop is sketched in Fig. 1-2.

The lower flux state by definition, will constitute a ONE and the upper a ZERO. To read out, enough positive current must be applied to switch the core from the lower to the upper state. If the core was already in the upper or ZERO state, there is very little flux output. Reading a ONE, therefore, produces a large voltage, while reading a ZERO gives a small output. These outputs are sketched in Fig. 1-3.

The memory cycle consists in reading the information contained in a register and then writing into the same register (not necessarily the same information). It is important at this point to recognize two important facts:

1. The read-out destroys the information held in the core, i.e., all cores in the register are put in the ZERO state.
2. The read-out does not require any selection among the digits. The entire register receives the read-out excitation, whereas in writing some cores in the register will be switched to the ONE state and others will be left in the ZERO state they were in because of reading - depending, of course, on the information to be stored in the register.

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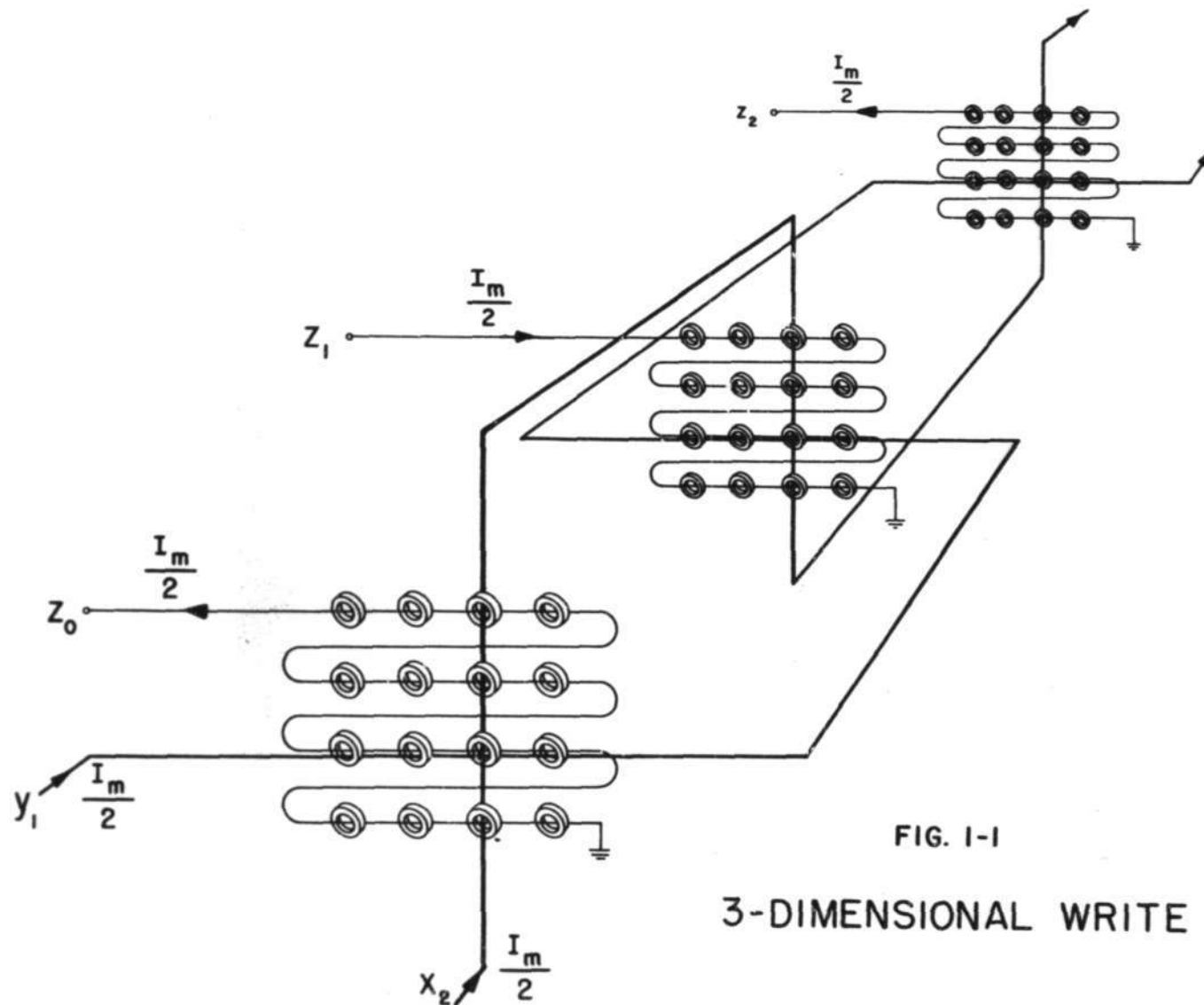
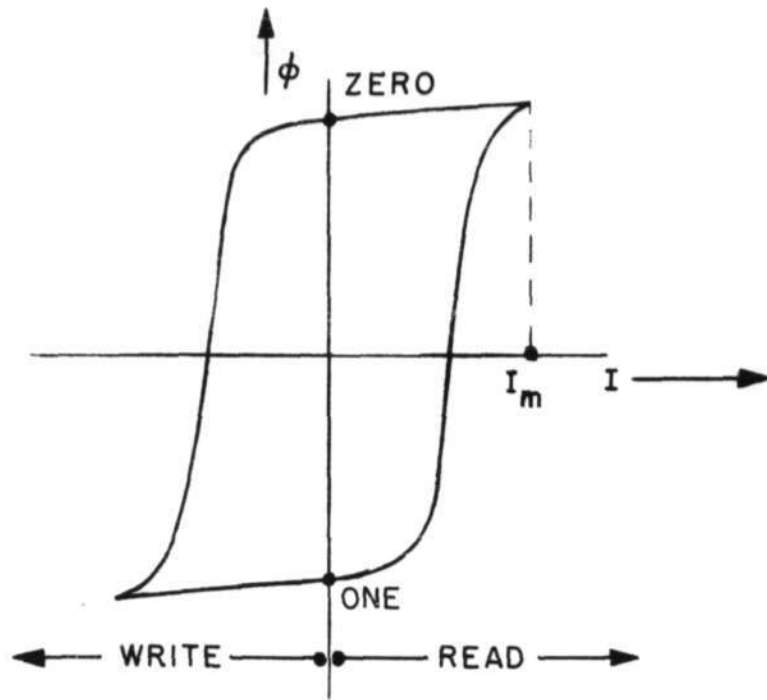
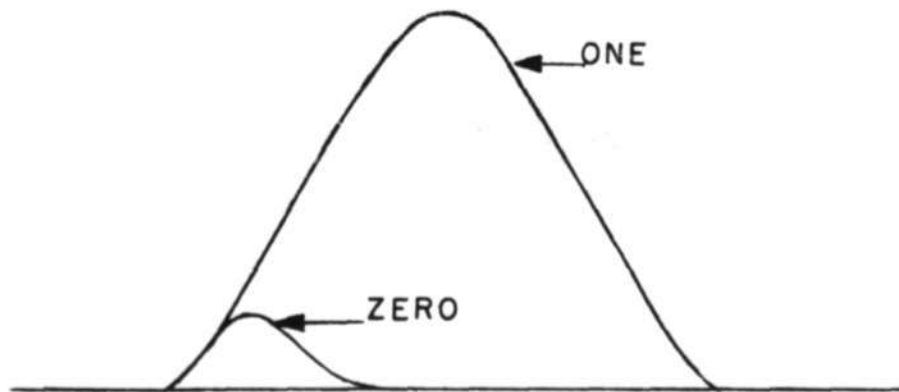


FIG. 1-1
3-DIMENSIONAL WRITE



MEMORY CORE HYSTERESIS LOOP

FIG. 1-2



SKETCH OF ZERO AND ONE OUTPUTS

FROM A MEMORY CORE

FIG. 1-3

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Two functions need explaining:

1. How a register can be selected to read;
2. How an arbitrary pattern of ONES and ZEROS can be written in a register.

Both of these of course must be accomplished without changing the information held by the other cores in the array.

If the current necessary to switch a core is defined as I_m and the core material is such that $I_m/2$ will not switch the core, then by applying $+I_m/2$ to an X line and $+I_m/2$ to any Y line, it is possible to select the register at the intersection of these two co-ordinates without destroying the information held in other registers. In order to write in this register $-I_m/2$ is applied on the X and $-I_m/2$ on the Y line. The appropriate Z-windings are used to inhibit with $+I_m/2$ on those planes in which ZEROS are to be written. This selection process depends entirely on the ability of the core to switch at an excitation of I_m and to remain unchanged when subjected to an excitation of $I_m/2$. At this point it is convenient to define the noise in this system as that part of the sense-winding output during read-out which is not contributed by the selected core. The noise would be made up of capacitive and inductive coupling from driving lines as well as the outputs due to half-selected cores which are subjected to $I_m/2$ excitation.

1.3 Memory Evaluation

The system described above is only one of a very large number which uses the magnetic core as its basic element. Part of the aim of this thesis is to organize the sporadic series of inspirational schemes

for magnetic-core memories into a general system of selection principles and to attempt to characterize the memory system in terms of significant key properties which will help in evaluating the many different possible schemes.

These properties are:

1. Reliability, which is most easily estimated by tube count and margins;
2. Size (number of registers x number of places = number of bits);
3. Access time; the minimum time between successive read-outs.
4. Cost, which is mainly measured by core specifications, wiring complexity, and tube count.

1.4 Outline

The general problem of selection in a core memory will be considered in the next Chapter, and a system using a core switch for direct register drive will be outlined. Chapter 3 will be concerned with saturable transformer design for such core switches.

Chapter 4 will describe the design and experimental work on a system consisting of a 256-position core switch driving a 16-place memory register-wise. Results, conclusions, and suggestions for future work will be contained in Chapter 5.

The appendices contain descriptions of two suggested systems which have some unusual features.

CHAPTER 2

SELECTION SYSTEMS FOR CORE MEMORIES

2.0 The Switching Problem

For a memory with 2^N registers, the switching problem for reading is to select one register determined by the information held in N flip-flops. Selection consists of applying full switching current to the cores in the appropriate register without destroying information held in other registers. For writing it must be possible to put any combination of ONES and ZEROS in the different places of the selected register.

To perform these selection or switching functions assume only the following sources of nonlinearity to be available:

1. Memory cores with square hysteresis loops;
2. Diode matrices;
3. Saturable transformers (or switch cores).

The over-all switching system is the result of cascading these 3 elements, each of which is capable of being used as an "and" gate, into a combination capable of controlling 2^N outputs from the N input-pairs available at the address flip-flops.

2.1 Memory Cores

Memory-core materials now available are either sintered ferrite or metallic ribbon. In general, the metallic cores switch more slowly than most ferrites at coincident-current excitations and have lower coercive forces. Experiments show that the product of switching time and net magnetic field intensity is a constant for a given material.⁴

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This constant S_w is smaller for metals than for ferrites and does not vary greatly for different ferrite mixtures now available. (Net field is the applied field less the coercive force of the material.)

If ρ is defined as the ratio of the smallest excitation which will switch a core to the largest which will not, then core materials presently at hand have characteristics in the range from $\rho = 1.5$ to 3. It is important to realize that successful selection as defined above is not necessarily sufficient in itself to assure a working memory array. For this, the output of a ONE must be distinguishable from that of a ZERO in the presence of noise on the sense winding during the read process. Much work has been done to analyze the different types of noise produced by partially selected cores⁵ and the effect of sense-winding geometry on the noise problem.⁶

R. Everett has developed the general principles of selection within an array of memory cores.⁷ Consider an array of cores each lying at the intersection of S co-ordinate wires and specify that selection will be made by the linear addition of S independent selections, one in each co-ordinate. The selection ratio R is defined as the absolute value of the ratio between the excitation received by the selected core and the largest total excitation received by any unselected core. It is possible to show that the maximum selection ratio, R_M , obtainable for a system having S dimensions is given by:

$$R_M = \frac{S + 1}{S - 1} \quad (1)$$

For a system to have $R = R_M$ it is necessary and sufficient that the following conditions be fulfilled:

1. The difference between the selecting and unselecting excitations in any dimension is $2/(S+1)$ of full switching current.
2. The absolute value of neither selecting nor unselecting excitations can exceed $2/(S+1)$ of full switching current.
3. The sum of all selecting excitations is equal to full switching current.

For successful selection it is necessary, of course, that R be greater than ρ . The number of cores, C , in an array having a coincidence of S dimensions, the s^{th} of which has σ_s elements, (that is drive wires) is given by the product of the number of elements in each dimension,

$$C = \prod_{s=1}^S \sigma_s \quad (2)$$

2.2 Switch Cores

The use of saturable transformers as switching elements has been described extensively in the literature.^{8,9,10} For the present the core can be considered as having characteristics similar to those of a memory core. There is one fundamental difference, however, between their modes of operation. A switch core is not required to store information beyond the limits of a single cycle. That is, after a core has been switched and before another selection can be made, the core is always reset to its original starting point on the hysteresis loop. The selection problem within the switch is, therefore, much less severe than in the memory core, since unlimited amounts of bias current can be applied to

nonselected cores without any danger of destroying information. Ideally, therefore, the ρ of the switch core approaches unity, and the number of dimensions of selection can be as large as desired.

In the systems to be considered, the core switch, where used, will provide the current pulses on the co-ordinate wires of the memory. The elements of a given dimension will be controlled by a switch having as many outputs as there are elements.

Concern here is only with modes of operation in which both polarities of output are used to drive the memory cores, the first during read and the second during write. This eliminates the need for a diode for decoupling the load when the core is switching back and eliminates the need for separate write drivers. This also precludes the possibility of switching back the switch core at some time outside the read-write cycle. This method has certain advantages but is too costly in time to be considered here. As in the case of the memory core, consider a switch core lying at the intersection of M co-ordinate wires. If the net excitation received by the selected switch core is defined as unity, then the requirements on the excitations for selecting and unselecting are:

1. The difference between selecting and unselecting excitations in any nontrivial dimension is greater than or equal to unity. (A nontrivial dimension is one having more than a single element. A trivial dimension has a single element and would correspond to a wire linking all the cores in the switch which, therefore, is always selected

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since it was specified that one selection was made in each dimension. In referring to a switch as having a specific number of dimensions, nontrivial dimensions will henceforth be tacitly assumed unless otherwise stated.)

2. The sum of all the selecting excitations is equal to unity.

If condition 1 above is satisfied with an equal sign, the system is most efficient with respect to bias currents. That is, the greatest net excitation on any nonselected core is zero, the maximum allowable for an ideal core.

Two systems satisfying the requirements for successful selection are shown below in tabular form.

		<u>Dimensions</u>					
		S_1	S_2	S_3	- - - -	S_M	
<u>Excitations</u>	Selected	1	0	0	0	0	0
	Unselected	0	-1	-1	-1	-1	-1

		<u>Dimensions</u>					
		S_1	S_2	S_3	- - - -	S_M	
<u>Excitations</u>	Selected	1	1	1	1	1	$-(M-2)$
	Unselected	0	0	0	0	0	$-(M-2)$

The first scheme has the advantage of not using a trivial dimension. The second has the advantage of exciting only one driver at a time in each dimension, whereas the first requires all but one driver in each

dimension to be excited simultaneously. To switch the core back in either scheme 1 or 2 it is only necessary to unselect one dimension completely and change the address in any other dimension, thus giving a net excitation of -1 for writing.

In general, the following relationships are found to hold for core switches of this type.

For a σ position switch having M dimensions the mth containing μ_m elements:

$$\sigma = \prod_{m=1}^M \mu_m \quad (3)$$

That is, the number of switch outputs equals the product of the number of elements per dimension.

$$T = \sum_{m=1}^M \mu_m \quad (4)$$

The number of vacuum-tube drivers, T, required to excite the switch is given (equation (4)) by the sum of the number of elements in each dimension.

The number of wires per core (excluding secondary) is equal to the number of dimensions M. The number of switch cores a driver excites in a dimension is equal to the product of the number of elements in the other dimensions. From formulas (3) and (4) it can be shown that the tube count is minimized for a symmetrical system (i.e., one in which all the dimensions have the same number of elements). It can also be shown that after a point increasing the number of dimensions in a switch buys little in the way of reducing vacuum tube-count. As an example, consider

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the graph of tube count vs. M , the number of dimensions for a 256-position switch, as shown in Fig. 2-1. The net reduction in tube count in going from 2 to 8 dimensions is a factor of 2. The costs in added number of wires per core and in added number of cores driven per tube are to be weighted against this saving in drivers. A full binary switch, that is, one with 2 elements per dimension is probably never justifiable because of the great wiring complexity and the large number of cores driven per dimension. Any quaternary switch (4 elements per dimension) yields the same tube count (because $2+2 = 2 \times 2$) but requires half the windings per core needed in the binary, and each tube drives one-half as many cores.

2.3 Diode Matrix

The diode matrix shown schematically in Fig. 4-7 is capable of providing 2^F outputs from F flip-flops. In general, the flip-flops cannot drive the matrix directly, 2 buffers being needed per flip-flop or a total of $2F$ drivers for a matrix with 2^F outputs. The number of diodes required if the matrix is of the rectangular¹¹ kind is $F \times 2^F$. Depending on the circuit details, buffers may also be necessary between the matrix and the driver tubes.

2.4 General System

The method of cascading the three nonlinear elements discussed above into a complete memory-switching system is shown in Fig. 2-2.

The Greek letter in each box indicates the size of (number of outputs from) the switch it represents; the subscripts indicate the switching path with which it is associated.

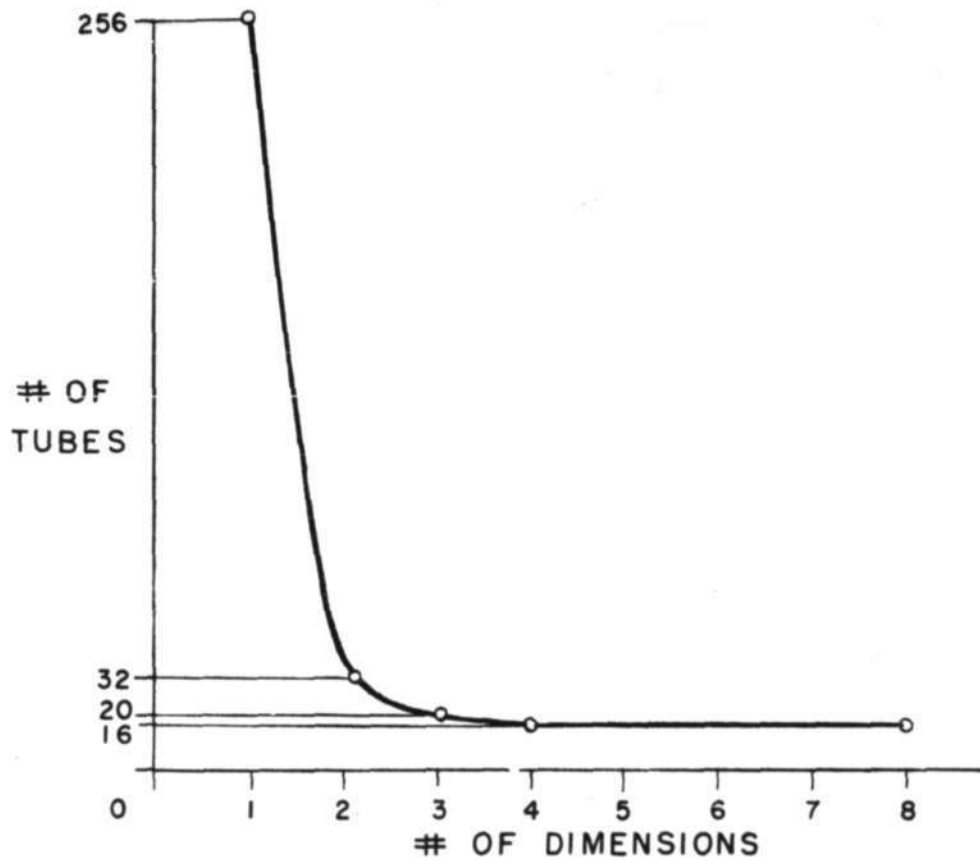
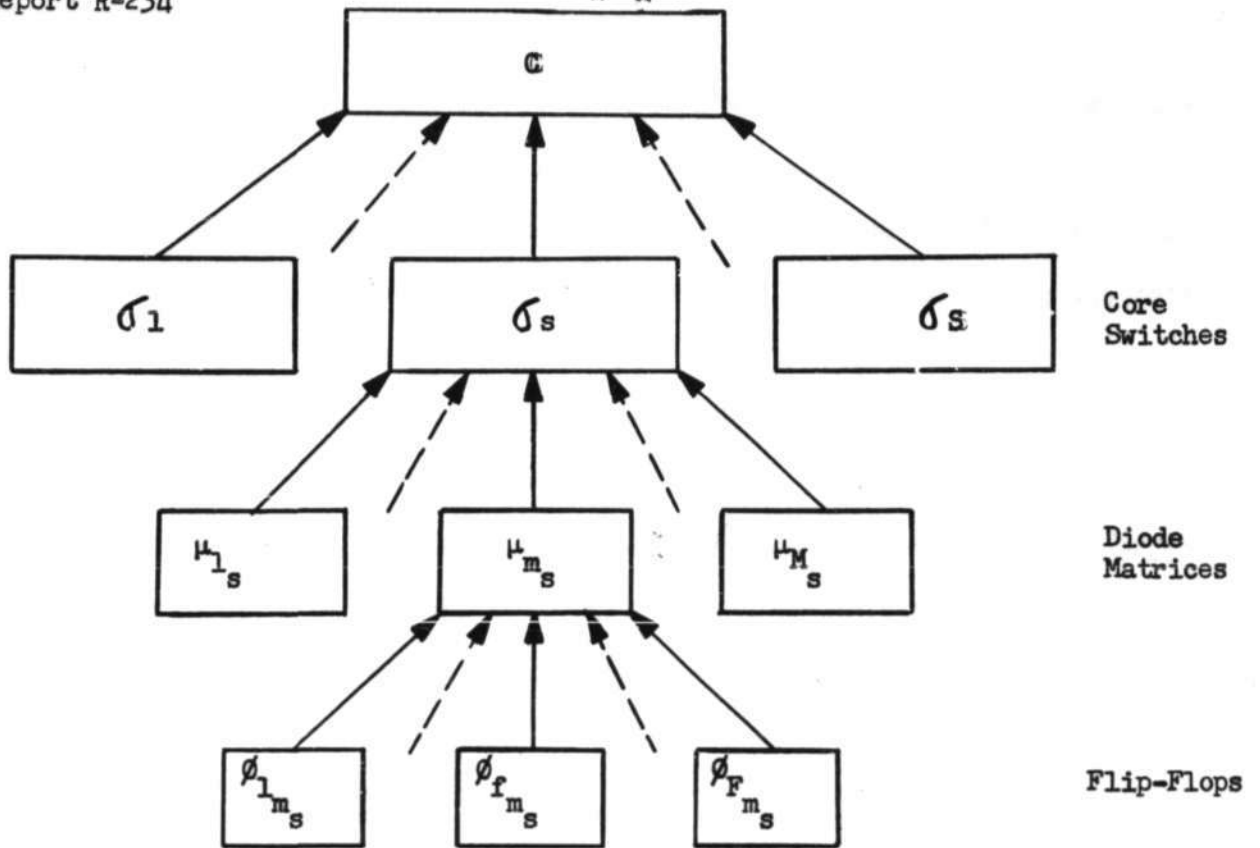


FIG. 2-1
TUBE COUNT vs. NUMBER OF DIMENSIONS
FOR A 256 POSITION CORE SWITCH

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C is the number of cores in memory.

s refers to the s^{th} switch and the dimension in the memory which it drives.

σ_s is the size of the s^{th} switch.

m_s refers to the m^{th} diode matrix driving the s^{th} core switch and the dimension in core switch which it selects.

μ_{m_s} is the size of m^{th} matrix in s^{th} switch.

f_{m_s} refers to f^{th} flip-flop driving m^{th} matrix driving s^{th} core switch.

$\phi_{f_{m_s}}$ is the size of flip-flop (always 2).

T is the number of vacuum-tube drivers.

D is the number of diodes in matrices.

GENERAL MEMORY SWITCHING SYSTEM

Fig. 2-2.

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An S-dimensional memory is driven by S independent core switches, each of which is excited in a number of dimensions by vacuum tubes which are in turn controlled by diode matrices which are selected by flip-flops.

The equations describing the over-all system and giving the total tube, diode, and switch-core count appear in Appendix 3.

In attempting to make a comparative evaluation between systems the following points should be kept in mind:

1. As S increases the number of wires in the memory increases, the ρ required increases, the number of inputs decreases, the number of memory cores to be driven per selecting line increases, and the number of memory-core noise outputs increases.

2. As M increases the number of windings per switch core increases, the number of cores per driver increases, and the number of noise-current outputs increases. The number of cores which are more highly saturated increases, and the number of different possible bias levels increases.

3. A dimension driven directly from vacuum tubes rather than from a core switch has the advantage of supplying high impedance and well-shaped pulses. The disadvantage is that separate drivers are required for reading and writing whereas the switch requires no write drivers, and 2 wires will be required per dimension unless a pulse transformer is used.

4. The actual number of cathodes per flip-flop associated with driving a diode matrix increases greatly with the size of the matrix if fast rise times are required. For a matrix with 4 or 8 outputs, for

instance, the cathode count per flip-flop is considerably lower than for a 64-position matrix. It is difficult to make a quantitative generalization, however, since much depends on the rise times required and on the tubes available.

2.5 Systems now under Investigation

With the general principles of selection established, it is interesting to consider specific systems. At the present time core-memory work at Lincoln Laboratory's Division 6 is proceeding on a number of systems. Since all of these are symmetrical, i.e., all switches of a kind are of the same size it is useful to introduce a shorthand notation to replace the complex symbols used above to describe the most general case. All that is required to define the system (assuming symmetry) is to specify 2 numbers, one giving the number of dimensions in the core memory and the other, the number of dimensions in the core switches M . Thus, a 2 - 3 memory is a 2-dimensional memory with 3-dimensional core switches driving each dimension. (An M of 1 means no core switch is used.)

This notation is used to describe the read process which is essentially one of register selection (it being tacitly understood that the write requires an additional dimension for place selection, which will be obtained directly from vacuum tubes). In discussing memory-core requirements for a particular system it should be emphasized, therefore, that the ρ required is determined by the R corresponding to the write rather than the read.

A consideration of these systems makes it clear that it is possible to trade one quality for another by design manipulation. The 2 - 1 system first attempted at M.I.T. uses the maximum number of vacuum tubes except for the 1 - 1 (which uses a prohibitive number). It has the minimum in wiring complexity, no core switches and only 2 drive wires per memory core for read (3 for write). A ρ of 2 is required.

The 2 - 6 system being attempted¹² is aimed at reducing the tube count and eliminating the need for the diode matrices (i.e., $F = 2$). The core requirements are unchanged, and the wiring complexity of the switch is an added cost.

The 4 - 1 system being considered¹³ is aimed at reducing the tube count drastically but places an extremely heavy burden on the memory cores which require a ρ of 1.5 and requires at least twice as many wires in the memory. The number of noise output is also increase considerably.

2.6 A Proposed System

It is interesting at this point to consider the possibility of designing a system in which ideally, at least, there would be no restriction on the ρ of the memory core. That is, one in which the selection is performed completely external to the memory itself. This does not fit readily into any of the categories previously mentioned because it requires a one-dimensional write, and the previous systems have all assumed a write with one dimension greater than the read. A possible realization of such a system is described in detail in Appendix 1 and an experimental investigation has been undertaken to determine its feasibility.¹⁴

2.7 System to be Designed

The experience gained with the Whirlwind I storage (which is of type 2-1) has led naturally to an attempt¹⁵ to overcome some of the more serious limitations inherent in the system. One of these was the rigid specifications on cores. A ρ of 2 was required and the number of noise outputs was such that cores had to be tested for half-select noise.

An ideal one-dimensional read system could allow a ρ of as much as 3 and would eliminate noise entirely during the read.

In considering the possibility of such a system the following facts should be noted.

First, it is obvious that a memory of any nontrivial size probably cannot be driven register-wise directly from vacuum tubes because of the prohibitive number required. A core switch having as many outputs as registers of storage could, however, do the job economically. Each core in the switch must be capable of driving a single register of cores. If the switch is not ideal there will be spurious outputs on the sense winding introduced by the noise outputs from the switch. The number, size, and characteristic of these will be determined by the design of the switch.

There are no limits to the amplitude of the read pulse so long as it is sufficient to switch the memory core. This means that faster, larger, readout signals are possible. The write pulse, however, is limited to the restrictions of 2-dimensional coincident-current operation. This operation can be obtained in 2 ways. The first method has a digit-plane driver which produces a half-amplitude pulse in the write direction,

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while the register line receives a half-amplitude write pulse from the core switch. The 2 together are sufficient to write a ONE but neither acting alone can switch a core. The second method has the register line supplied with a full-amplitude pulse and uses the digit-plane driver to inhibit when ZEROs are to be written. This latter method has the advantage of requiring a full-amplitude write pulse from the switch. Since the switch is constrained to put out equal-area pulses on read and on write, the write will require less time than if a half-amplitude pulse were used. The system described in the next Chapter, therefore, uses the digit-plane inhibit for writing.

The potential advantages of a one-dimensional read system over the 2-dimensional are:

1. Elimination of noise outputs;
2. Faster, larger, readout signals;
3. Increase of P to 3;
4. Simpler memory-plane construction.

The possible disadvantages are:

1. The added wiring complexity and expense of the switch;
2. Loss of current-pulse uniformity and output impedance in going from vacuum tube to switch drive.

The feasibility of the entire system depends heavily on the design of the core switch required to drive the registers. This design requires a thorough understanding of the operation of the saturable transformer when used as a switching element.

CHAPTER 3

THE SWITCH CORE AS A CIRCUIT ELEMENT

3.0 Ideal Switch Core

The ideal saturable transformer or switch core has 2 possible impedance levels, zero and infinity. As a shunt element it is capable of transmitting to the output terminals all or none of the energy applied to the input terminals depending on the state that it is in. The hysteresis loop for such an element is shown in Fig. 3-1. A detailed discussion of the use of the switch core as a logical element in the selection system of a magnetic-core memory is included in Chapter 2.

To design a working switch, however, it becomes necessary to consider the characteristics of existing rather than ideal elements. Fig. 3-2 shows the hysteresis loops for a metal and for a ferrite core. In particular, the transformer is often called upon to deliver current pulses of a specific shape, amplitude, and impedance level into various loads when selected (i.e., in the high impedance state). In addition, there is some upper limit to the noise output which can be tolerated when the core is in the low-impedance, or nonselected, state. In order to design for these conditions it is necessary to have a thorough understanding of the electrical characteristics of the core being use.

3.1 General Equivalent Circuit

At the outset it is possible to simplify the problem of the loaded core somewhat before going into the details of core characteristics. Consider the circuit of Fig. 3-3. It is always possible to reduce this to the equivalent circuit¹⁶ shown in Fig. 3-4 where l_1 and l_2 are primary and secondary leakage inductances and r_1 and r_2 are primary and secondary

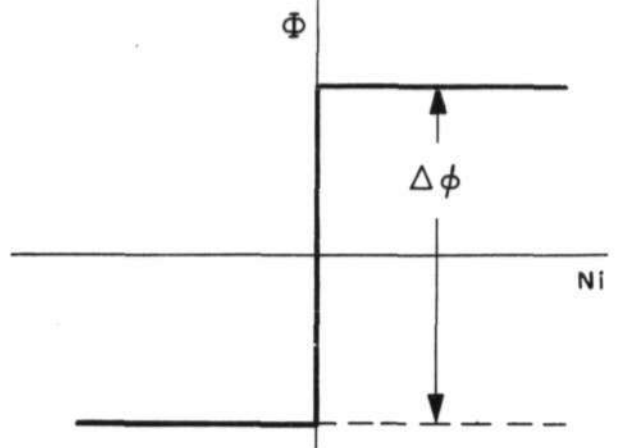
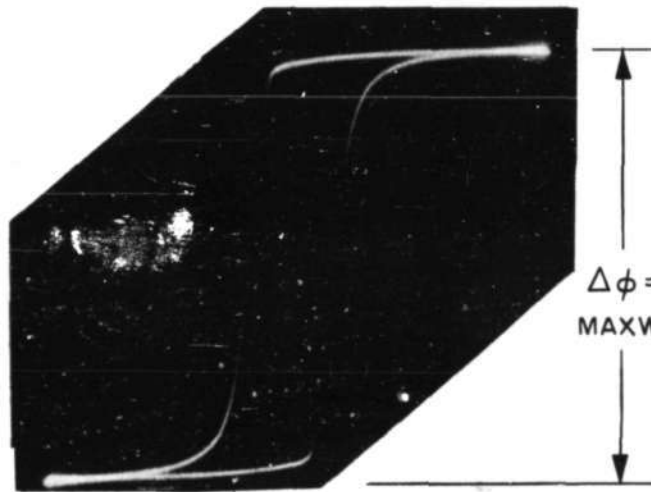
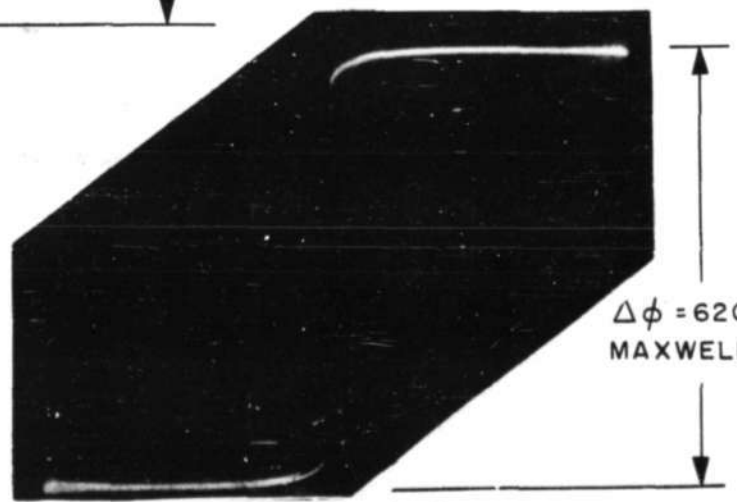


FIG. 3-1
HYSTERESIS LOOP OF IDEAL SWITCH CORE



10 AMP TURN PEAK DRIVE
MF 1312
F-262



10 AMP TURN PEAK DRIVE
MO-PERM 4-79
140 WRAP 1/4" 1/4 MIL

FIG. 3-2
HYSTERESIS LOOP OF A METAL AND OF A FERRITE CORE

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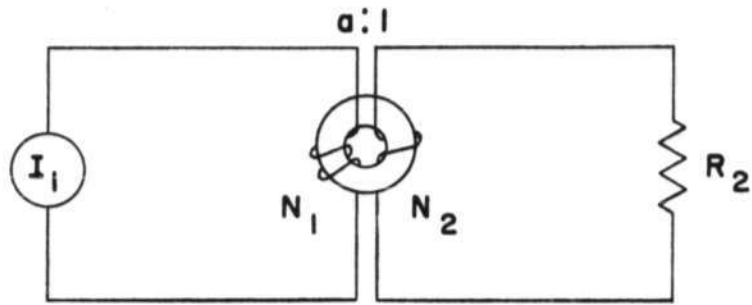


FIG. 3-3
SWITCH CORE WITH LOADED SECONDARY

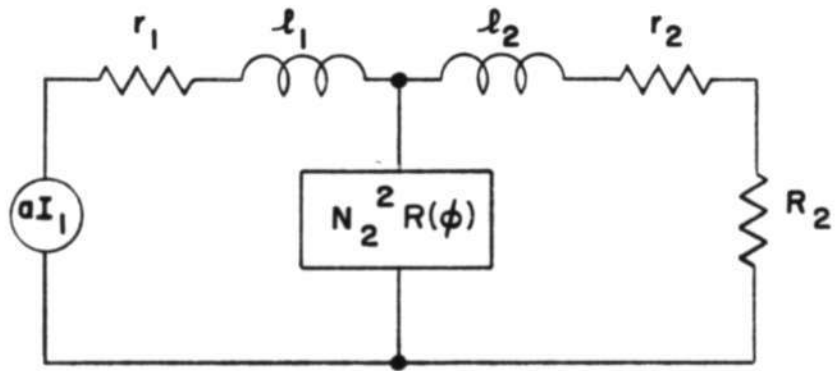


FIG. 3-4
GENERAL EQUIVALENT CIRCUIT
FOR SWITCH CORE WITH LOADED SECONDARY

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winding resistances. All of these are reflected to the secondary winding. This circuit is valid regardless of the specific character of the "black box" labelled $R(\phi)$ and implies no restrictions on it. In arriving at this circuit the following facts are noted:

1. The leakage flux will be proportional to the current producing it because, in general, much of the leakage-flux path is in air and the series reluctance of this portion of the path is large compared to the reluctance of the path within the core. Representation of the leakage components as linear inductances is, therefore, valid.

2. The flux in the core is the mutual flux. This assumes that fringing is negligible.

The problem of the loaded core is thus essentially reduced to that of determining the exact nature of $R(\phi)$. The significance of $R(\phi)$ as used to denote the "black box" of the equivalent circuit is that it represents the $v-i$ characteristic at the input to a single turn linking the core. Most generally it may be thought of as an operator which when multiplied by the current i gives the voltage v induced across the winding at any instant. Since this actually represents the voltage per turn vs. ampere-turn characteristic of the core, multiplying by N^2 specifies the $v-i$ characteristic for N turns.

It is important to realize that the loops of Fig. 3-2 do not present a true picture of the operation of the core in the $\phi-I$ plane under pulsed conditions. If they did, of course, the time response of the core to any excitation could be readily predicted from it. In this region,

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relaxation effects⁴ dominate the behavior of the core; that is, there is a delay between the sudden application of the magnetic field and the buildup of flux in the core. In addition, eddy-current loss cannot be neglected here. The tacit assumption of time independence which is made in discussing low-frequency loops is no longer justified here.

3.2 Current-Source Tests

If a square-loop material is excited with steps of current which exceed the full switching current of the material, the voltage responses of the core will have the general shapes shown in Fig. 3-5. If the voltage and time scales are normalized so that v/V -peak is plotted vs. t/T , the outputs tend to fall directly on one another. Further, if V -peak is plotted vs. I , the value of the exciting-current step, the relationship is linear with an intercept roughly equal to I_c . This plot is sketched in Fig. 3-6. H. K. Rising¹⁷ used the above data to arrive at an equivalent circuit for a metallic core which consisted of a current source in parallel with a resistance which was a function of the flux in the core alone. It is important to realize that this analysis is only valid for core excitations which exceed full switching current, I_m , or, in other words, for switching times which are less than T_m , the switching time corresponding to an excitation of I_m .

There are many applications where it is necessary to determine the $R(\phi)$ for slower switching times. This is particularly true when the core has a loaded secondary. Steps of constant current cannot be used in an open-circuit test for this region, because they would not succeed in fully switching the core. In the limit, of course, as the switching

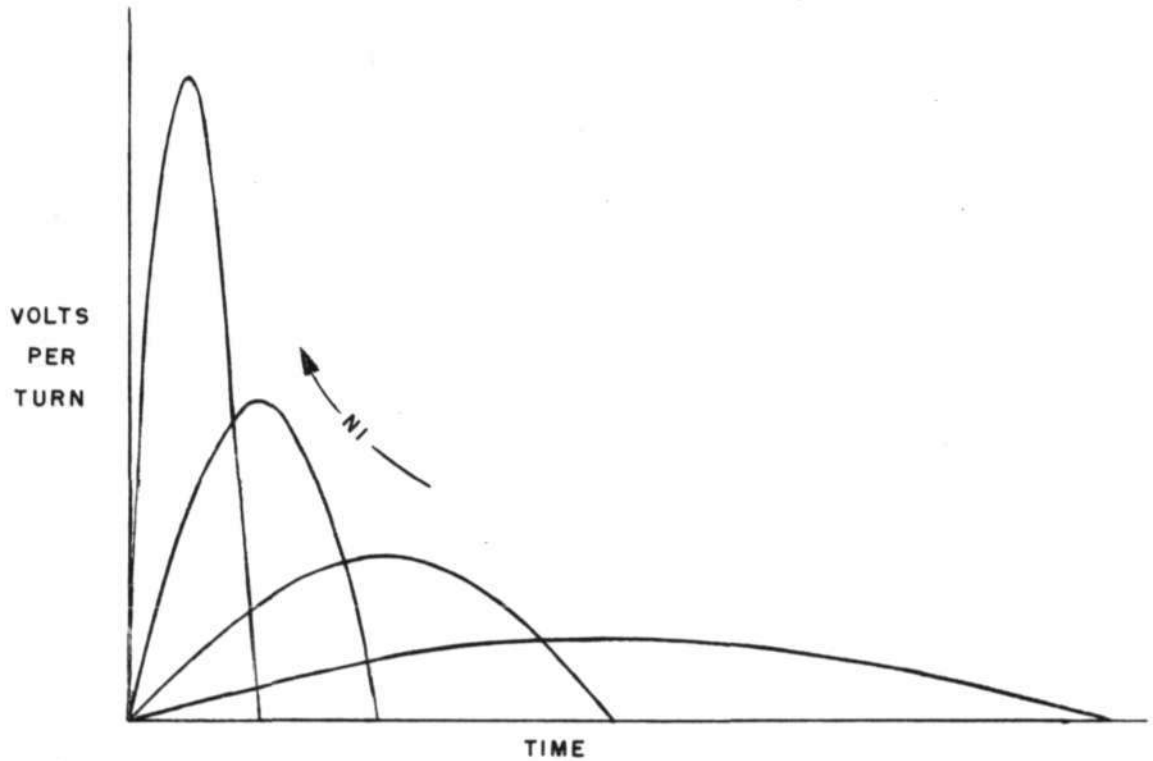


FIG. 3-5 SKETCH OF VOLTAGE RESPONSES OF CORES TO STEPS OF CURRENTS

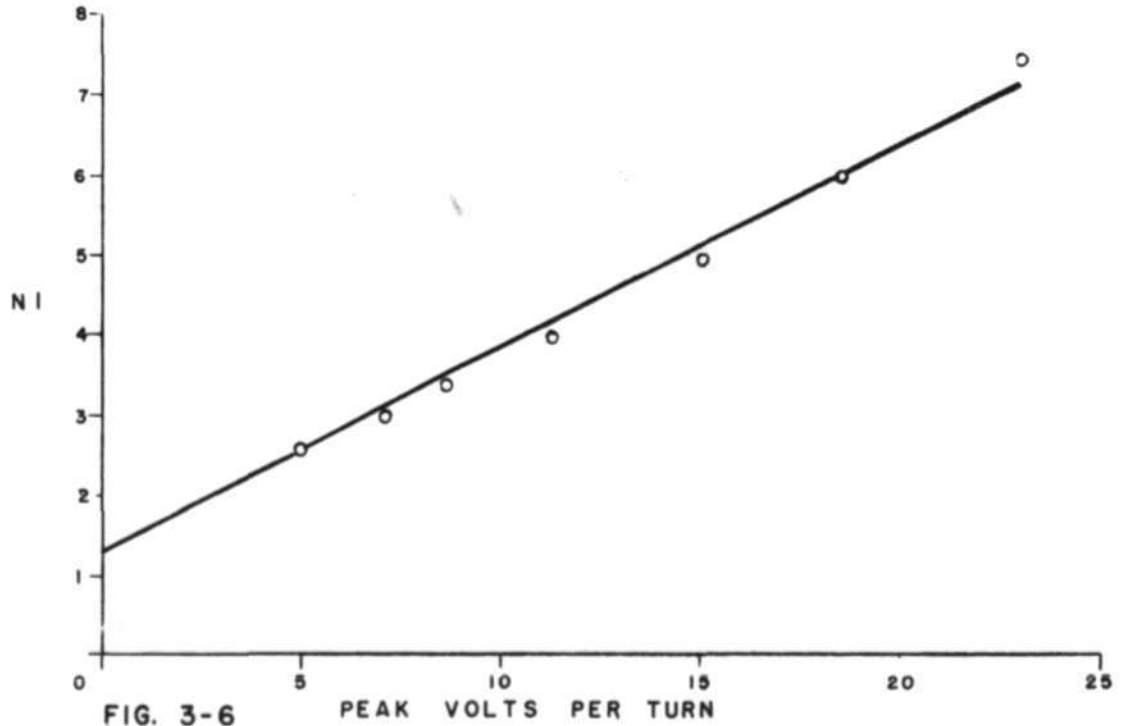


FIG. 3-6 PEAK VOLTAGE vs. AMPLITUDE OF CURRENT STEP FOR MF 1312 F-262 CORE

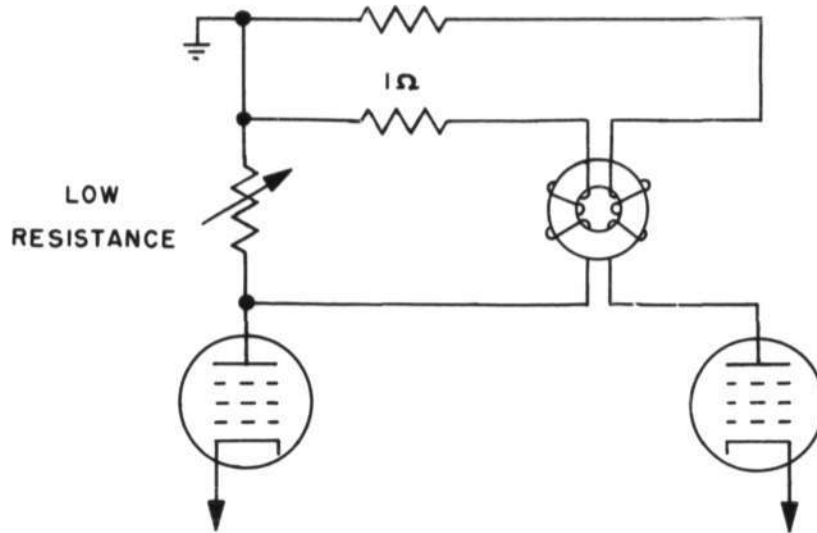
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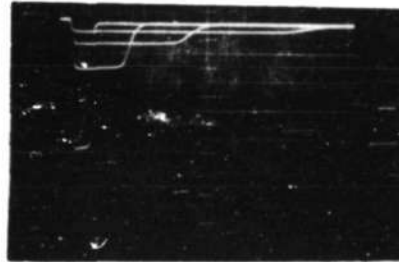
time approaches infinity, the d-c loop becomes valid, and this corresponds to an equivalent circuit having a current source in parallel with an inductance. In order to determine the equivalent circuit which is valid in the region between these 2 extremes, a series of experiments was devised.

3.3 Voltage-Source Tests

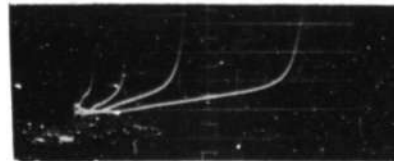
Consider what happens if an unloaded core is excited with a constant voltage source. If the source is of low enough impedance and no leakage is assumed, the voltage across the core will remain essentially constant as long as the core is switching, and equal increments of time will correspond to equal increments of flux. That is, for $d\phi/dt = V = \text{constant}$, ϕ will vary directly with t . The current exciting the core then, when viewed on an oscilloscope, will give a fairly good estimate of the I vs. ϕ relationship which holds for any given switching time and is, hence, a simple way of obtaining a hysteresis loop which is valid under pulsed conditions. Fig. 3-7 shows the voltage and current outputs for various values of switching time. If now the time scales are all normalized and the currents for various voltages are sketched approximately, they have the shape shown in Fig. 3-8 over the region in which the voltage across the core remains essentially constant. Actually, there is a hump on the current waveform at the beginning, but this will be neglected. The experimental setup used to obtain this data is shown in Fig. 3-7. The current driver on the right was merely used to switch the core back again. The driver on the left is the low-impedance source consisting of



EXPERIMENTAL SETUP
FOR "VOLTAGE SOURCE" DRIVE OF CORE



VOLTAGE OUTPUTS
FROM CORE EXCITED WITH STEPS OF VOLTAGE



MAGNETIZING CURRENTS
WHICH PRODUCE THE VOLTAGES SHOWN ABOVE

FIG. 3-7

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a pentode plate loaded with a low-impedance pot in parallel with the core winding which had 40 turns. The core tested was a General Ceramics MF-1312 of the F-262 type. Adjusting the resistance varied the voltage across the core and hence the switching time. A 1-ohm resistor in the winding was used to monitor the magnetizing current. Using the sketches of current shown in Fig. 3-8 an equivalent circuit consisting of a resistor, an inductance, and a current source in parallel can be obtained to represent the operation of the core for a particular range of switching times. The value of resistance can be calculated from the change in voltage over the change in current as measured by the vertical displacement between 2 lines in Fig. 3-8. The inductance is measured by measuring the slopes of the current waveforms. The equivalent current source is obtained from extrapolation using the value of R and the initial points on the current-waveform sketches. The data taken here was for switching times from 1.5 to 20 microseconds.

The values of R, L and I_0 which were obtained for the experimental setup described above are given below:

$$R = 5620 \text{ ohms,}$$

$$L = 2560 \text{ microhenries,}$$

$$I = 0.027 \text{ amperes.}$$

Since these were all on a 40-turn basis they must be normalized in order to be made independent of number of turns. To do this, impedances are divided by N^2 , or 1600, and currents are multiplied by N, or 40.

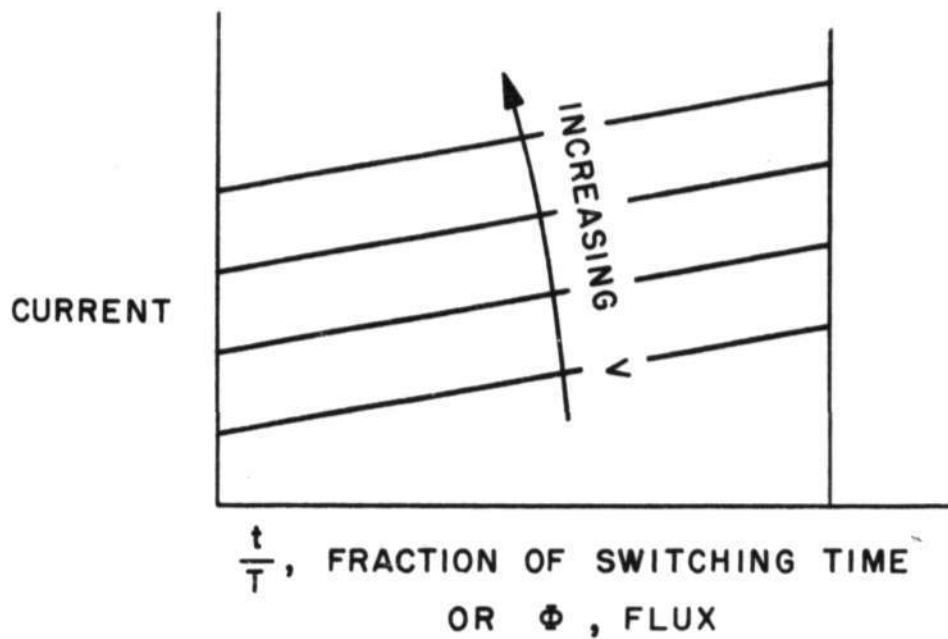


FIG. 3-8

SKETCH OF EXCITING CURRENTS FOR DIFFERENT MAGNITUDES OF VOLTAGE SOURCE EXCITATIONS ON NORMALIZED TIME SCALE

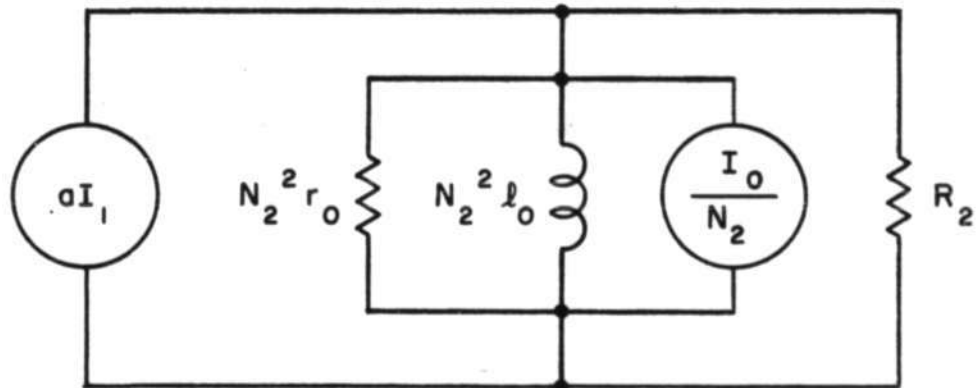


FIG. 3-9

EQUIVALENT CIRCUIT FOR CORE DRIVEN BY CURRENT SOURCE AND LOADED WITH SECONDARY RESISTOR

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This yields values of:

$$\begin{aligned} r_o &= 3.5 \text{ ohms per turn}^2, \\ l_o &= 1.6 \text{ microhenries per turn}^2, \\ i_o &= 1.1 \text{ amperes.} \end{aligned}$$

It should be pointed out here that a plot of V-peak versus I on a single-turn basis (using Rising's method¹⁷ to extend to the region for faster switching times) yielded the plot shown in Fig. 3-6 for this core. This yields a current source value of 1.2 amperes and a peak resistance of 3.8 ohms per turn² which check closely with those found above.

3.4 Universal Curves

Returning now to the original problem of a core loaded with some secondary impedance, it is interesting to see how the above analysis checks out with experimental results. Consider a core loaded with a secondary resistance and driven on the primary by a step of current. In switch design for driving a magnetic-core memory it is often desirable to obtain a secondary current pulse of specific amplitude and impedance level for a minimum amount of $N_1 I_1$. If leakage is neglected, the equivalent circuit reduces to a simple resistive divider in parallel with a current source and an inductance as shown in Fig. 3-9. If this circuit is solved for the maximum value of secondary current, I_2 , before the inductance begins to draw current, I_2 can be expressed as:

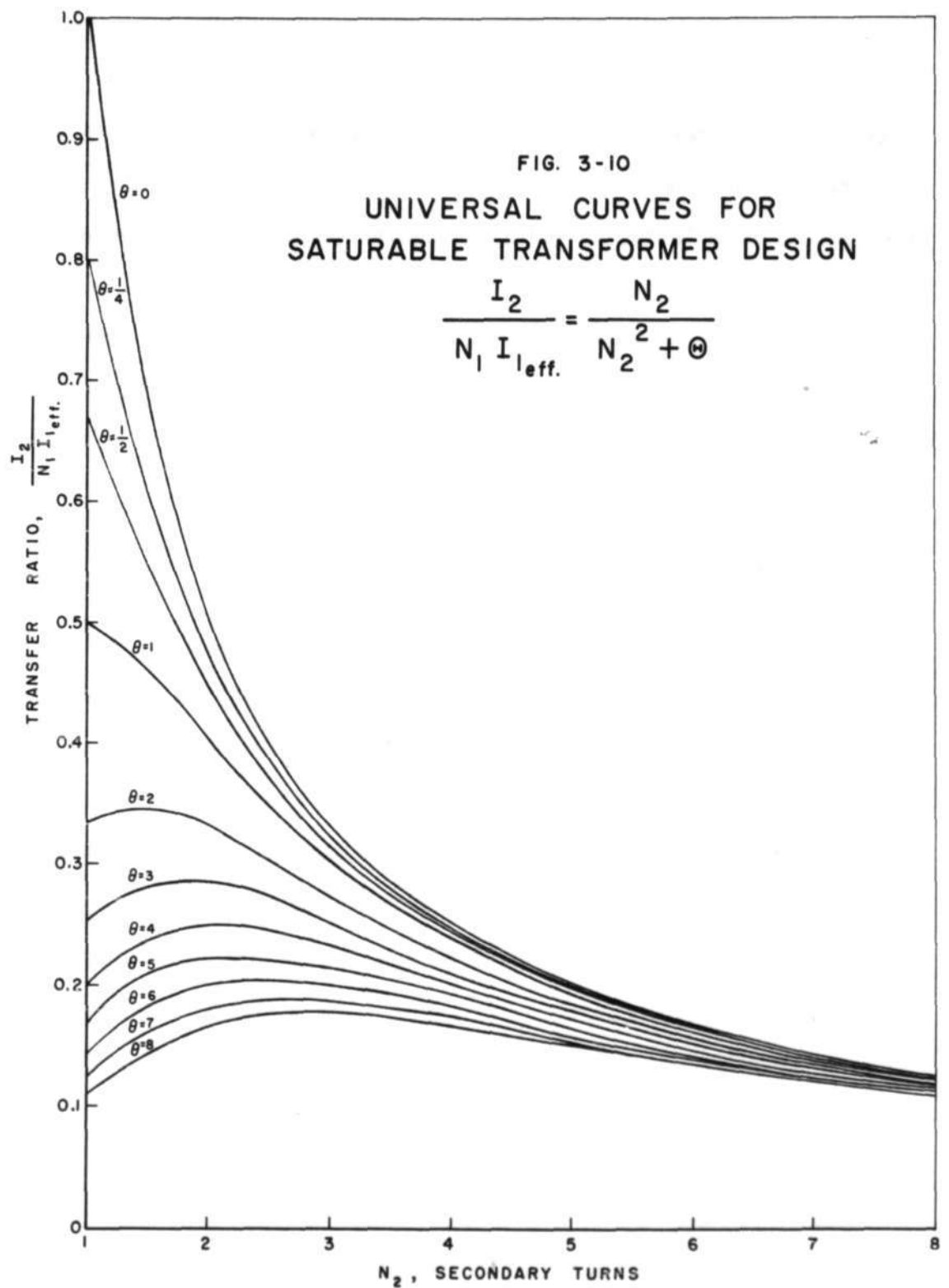
$$I_2 = \frac{N_1 I_{1\text{eff}} \times N_2}{N_2^2 + \theta}$$

where $N_1 I_{1\text{eff}} = N_1 I_1 - I_o$

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The ratio $I_2 / N_1 I_{1_{\text{eff}}}$ will be called the transfer ratio. This is the secondary current per unit of effective ampere-turn input and if plotted versus secondary turns with the ratio $\theta = R_2 / r_0$ as a parameter a set of universal curves is obtained which is useful for switch-design purposes. These universal curves are shown in Fig. 3-10. The following observations can be made about them:

1. The curve for $\theta = 0$ represents the ideal transformer curve.
2. As θ becomes larger the maximum value of transfer ratio occurs at larger and larger values of N_2 . In other words, for large values of θ the transfer ratio actually increases with N_2 over some region, which is never true of the ideal transformer.
3. The current regulation in the face of some change in secondary resistance, $\Delta\theta$, may be easily estimated from these graphs. The percentage change in transfer ratio for a given $\Delta\theta$ can be measured by the vertical distance between parameter lines on the graph. Thus, at a constant value of N_2 the vertical spacing of the parameter lines becomes closer for increasing θ due to the increased output impedance and hence better regulation resulting from higher secondary resistance. Similarly for constant θ as N_2 increases the spacing of the lines becomes much closer indicating the better regulation due to higher transformer impedance.
4. It should be pointed out that the emphasis of this analysis on transformer design in the region far removed from ideal is not merely gratuitous. In switch-core work, this is very often the region of most interest as will be pointed out later.



An interesting example of the practical use of this chart was demonstrated when an attempt was made to re-examine some of the early designs on switch cores made at M.I.T.⁸ At that time a switch was designed with MF-1118 cores using a strictly empirical method. Various values of secondary turns were tested experimentally, and a value of $N_2 = 2$ was finally chosen as having the best transfer ratio. The particular core and terminating resistor used in this design give a value of θ somewhere around 4 or 5. From the universal curves of Fig. 3-10, it is clear that the peak transfer ratio should be expected to occur at $N_2 = 2$, and, therefore, this empirically-derived design becomes readily understandable.

An experimental verification of the curves in Fig. 3-10 obtained from tests on an MF-1313, F-262 core are shown in Fig. 3-11. They show the same characteristic shape as the theoretical curves and illustrate well the variation of I_2 with R_2 and N_2 . At this point, it is necessary to emphasize that no consideration has yet been given to the transition from high to low impedance which is implied when it is said that the core has finished switching. Assuming for the moment that the low-impedance state is essentially zero, then the secondary pulse would be expected to terminate when the secondary flux linkages as given by the product $N_2 \times \Delta\phi$, have been dissipated in the secondary load ($\Delta\phi$ is measured as in Fig. 3-2). Actually, the transition from the high-impedance state is not sharply defined but is rather gradual in most materials. The low-impedance state can probably be well estimated by referring to appropriate portions of the d-c loop. It is important to

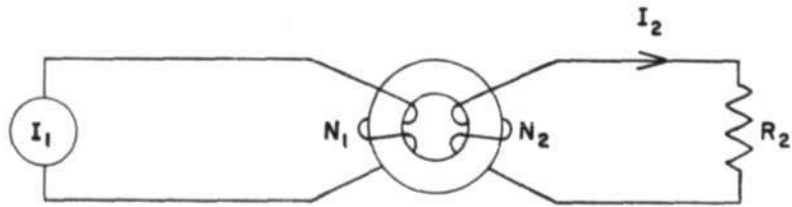
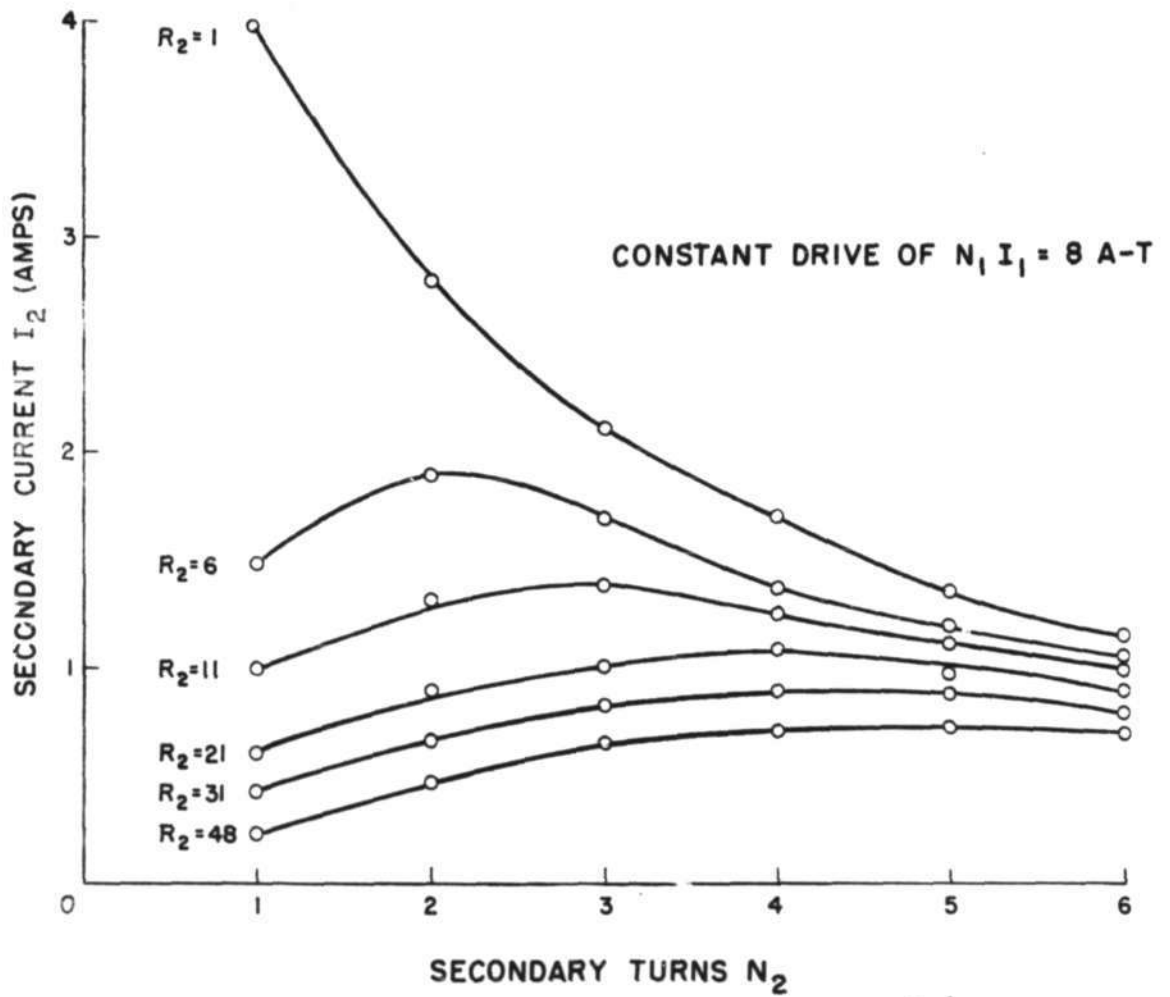


FIG. 3-II

EXPERIMENTAL CURVES FOR I_2 AS A FUNCTION OF N_2 AND R_2

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realize that the equivalent circuit developed above is only valid during the time the core is still switching.

3.5 Core Loss

It should also be emphasized that all 3 elements, current source, resistance, and inductance, are really dissipative in that the energy put into them in a single half cycle is not recovered again. The total energy loss in a core being switched is expressed by:

$$W = \int_0^t N_{i_{NET}} \times v \, dt$$

$$\text{where } N_{i_{NET}} = N_1 i_1 - N_2 i_2$$

For constant voltage this yields:

$$\begin{aligned} W &= \frac{\Delta \Phi}{T} \int_0^t N_{i_{NET}} \, dt \\ &= N_{i_{NET}}^{(T)}_{av.} \times \Delta \Phi \end{aligned}$$

where $N_{i_{NET}}^{(T)}_{av.}$ is the average net magnetizing ampere-turns for switching time, T.

Calculations of energy losses in cores and the effect of heating on core output have been discussed in another paper by the author¹⁸ and will not be considered in detail here.

3.6 Equivalent-Circuit Parameter Values

In selecting cores for use in specific designs it is useful to know how the equivalent circuit varies with various parameters. The following generalizations are fairly obvious: r_o and l_o both vary directly with flux density and cross-sectional area and inversely with mean radius.

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Unfortunately, however, $\Delta\Phi$ varies similarly with the first 2 items. Since the product $N_2 \times \Delta\Phi$ determines switching time it is impossible to vary $\Delta\Phi$ without compensating for it somehow to maintain the same switching time.

In the simple case of a resistive load, for instance, the switching time and flux linkages would be related by the following equation if a square pulse of secondary current is assumed.

$$N_2 \times \Delta\Phi = I_2 R_2 T$$

Aside from variations due to core size there is, of course, variation in materials. A detailed analysis of all materials is not available at this time, but preliminary evidence seems to definitely favor metallic cores over ferrites in that both the low- and high-impedance states approach more closely the ideal. In addition there is a good deal less sensitivity to temperature exhibited by the metals mainly because they have a higher Curie point. However, work is being done towards the development of ferrite materials having the desirable properties of metals.

3.7 Pulse-Sequence Sensitivity

In switches in which there are varying amounts of bias on different cores and in which the operation is in a region far removed from saturation, it is possible to encounter nonuniformity of outputs because of the many pulse sequences to which a core may be subjected, and which cause the core to operate on a variety of loops. In this respect it is important to note that metals tend to saturate much more readily than ferrites. The

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number of units of bias to which a core may be subjected depends upon the number of bias dimensions in the switch; therefore, this effect should be more noticeable in switches with more dimensions.

3.8 Noise

In considering noise outputs it should be noted that as the knee of the loop is approached from negative saturation, the slope increases considerably in the region of zero current. The allowable noise output will determine the region to which satisfactory low impedance operation is confined. It is also evident that the amplitude of the drive pulse will greatly determine the effective signal-to-noise ratio on a flux basis. The greater the basic unit of input excitation, the poorer the signal-to-noise ratio. This can be seen simply from the equation below

$$\begin{array}{l} \text{Ratio of signal flux} \\ \text{to noise flux} \end{array} \approx \frac{\Delta \phi}{\phi_n}$$

where $\Delta \phi$ is twice the remanent flux and ϕ_n is the flux change in a partially selected core due to an excitation such as X in Fig. 4-3. If ϕ_n increases with I (even though not necessarily linearly) this ratio becomes smaller for increased I. The influence of the size of R_2 on noise output must also be taken into account. In the limit as R_2 approaches zero the core would act as an ideal transformer even in the low-impedance state if secondary leakage and wire resistance are neglected. Actually leakage would be a significant factor at this low-impedance level, and the equivalent circuit would be an inductive current divider formed by the low-impedance magnetizing inductance and the secondary leakage inductance. The noise currents could thus be extremely high depending

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upon leakage. As R_2 becomes large, on the other hand, the secondary current would approach the open-circuit noise voltage divided by R_2 . In general it can be said of a particular design that the signal-to-noise ratio of secondary current can be no worse than the ratio of the amplitude of core voltage (obtained for specified switching time by the open-circuit voltage-source test described previously) to the open-circuit voltage amplitude for the specified $N_1 I_1$ excitation applied to the core in the saturated or low-impedance regions.

3.9 Summary

The design of a single saturable transformer to meet specific impedance level, amplitude, switching time, and noise requirements is a fairly complicated problem. The design of a large matrix of these transformers, including the choice of one of an extremely large number of selection systems, must necessarily entail a good many compromises, educated guesses, and experimentation. It is perhaps in order then to summarize the analysis given above and to indicate the nature of the compromises which will have to be made. If it is assumed that I_2 and T , the switching time, are fixed by the driving requirements of the memory and that the core material at hand most closely approaches the ideal, how should N_2 , $\Delta \Phi$ and R_2 be chosen? Increasing N_2 indefinitely, increases the transformer impedance and hence provides better current regulation, also making the output less dependent on the core characteristics but it also tends to increase the noise amplitude by increasing the impedance in the nonselect case. What is more, it tends to decrease the transfer ratio thus requiring more primary turns and/or current per unit of

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secondary current. On the other hand, increasing R_2 tends to decrease the transfer ratio and requires more $N_2 \Delta \Phi$ for the same switching time. However, it improves current regulation and reduces the amplitude of the noise pulse. The exact nature of the vacuum tubes available, the memory load to be driven, the noise pulses tolerable, the number of windings per switch core determined by the selection system, the size of the switch, and the physical dimensions of the core will all influence the final values of N_2 , $\Delta \Phi$ and R_2 chosen. In Chapter 4 an example will be given of the application of this analysis to the design of a working switch.

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CHAPTER 4

EXPERIMENTAL MEMORY SYSTEM USING A 256-POSITION
CORE SWITCH FOR REGISTER DRIVE

The decision to construct a working memory employing one-dimensional read supplied by a register switch was arrived at only after possible advantages and difficulties were evaluated. A block schematic showing the flip-flops, diode matrices, core switch, and memory is shown in the dotted box of Fig. 4-13. An inherent property of the system which greatly influences the switch design is the fact that while the total secondary load is rather small, (the register wire links only one core per digit plane) it varies greatly with the information stored. The switch core can be loaded with anywhere from 0 to n memory cores switching for an n-place memory. In an attempt to eliminate this variation in load a memory was proposed⁸ which requires 2 cores per cell. Each of these always holds information which is the opposite of that held by the other. A detailed description of such a system and some experimental results for single-register tests are given in Appendix 2 but will not be discussed at all here.

4.0 Memory Specifications

In designing an experimental switch for register selection, it was necessary to decide on a size that would be large enough to allow extrapolation of results to large-scale memories, yet small enough to allow completion of the project with a reasonable expenditure of time, effort, and material. A memory capacity of 256 registers of 16-digit word length was chosen as fulfilling these requirements. An access time

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of from 5 to 6 microseconds was accepted as a worth-while goal and the design, therefore, aimed at obtaining this.

4.1 Materials

It was decided that ferrite cores would be used, although metallic switch cores approach ideal characteristics much more closely and present a far less serious heating problem than ferrites. It was felt that the ferrites could probably be designed to work satisfactorily and the heating problem could be side-stepped temporarily, in this experimental model at least, by restricting operation to low pulse repetition frequencies. The significantly lower cost of ferrites and the availability of a ready supply for experimental purposes largely influenced this decision.

The material chosen was MF-1312. This mixture has a medium switching speed and a low S_w compared with most ferrites. A supply of General Ceramics MF-1312 cores part No. F-262 was available. This size core met the requirements for a workable design in 2 important respects: available flux and wiring convenience. These will be discussed in more detail in another section.

The core chosen for the memory which the switch drives is MF-1326-B part No. F-394. This is the same core that is used in the MTC memory.

4.2 Core Testing

The testing of switch cores was done in a crude but convenient manner. A batch of about 30 cores was driven successively by pulses of alternate polarity from 6CD6 current amplifiers. The large back voltage

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of all the switching cores caused the tube to bottom and the cores to switch at fairly constant voltage. Inspection of the output developed across each core allowed a ready means for selection of those lying within arbitrary voltage limits. In this manner the 256 cores needed were selected from the total of about 500 available. The outputs for acceptable, marginal, and unacceptable cores are shown in Fig. 4-1 along with the driving current waveform.

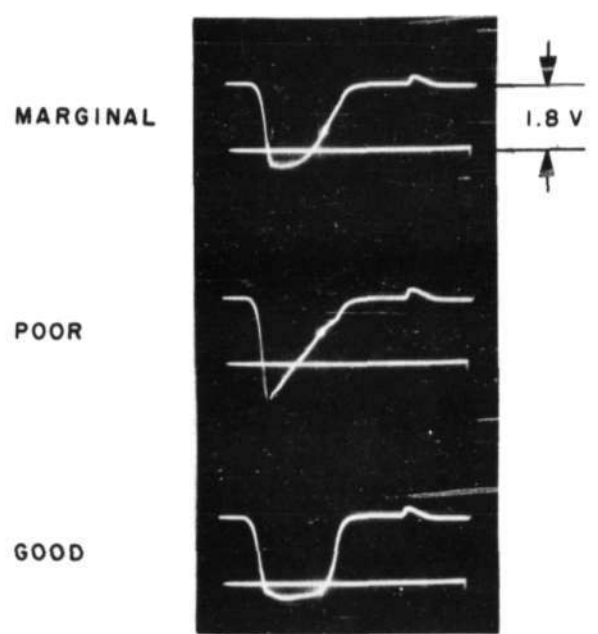
4.3 Saturable-Transformer Design

The analysis of Chapter 3 points out that the secondary impedance (which determines secondary current regulation in the face of changing load) is made up of 2 components, the secondary resistance and the magnetizing impedance of the transformer which varies with the square of the secondary turns. It is also necessary that the core have the proper amount of flux available when switching so that the prescribed access-time requirements are met. The approximation which determines the amount of flux required is given by:

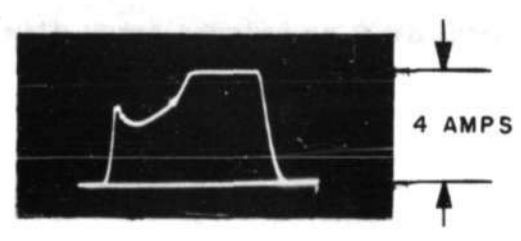
$$N_2 \Delta \Phi = I_2 R_2 T$$

In other words, the secondary-flux linkages must equal the product of secondary current, resistance, and switching time, which is the area of the voltage pulse appearing across the resistor. This assumes that the flux of the memory cores is small compared to the flux dissipated across the resistor.

The combination of secondary turns equal to 5 and secondary resistance equal to 10 ohms was found to give sufficient secondary impedance, while at the same time satisfying the equation above relating



OUTPUTS FROM GOOD, POOR, AND MARGINAL CORES



DRIVING CURRENT WAVE-FORM FOR SWITCH CORE TEST

FIG. 4-1

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flux and switching time. Substituting below in this equation and solving for $\Delta \phi$, we find:

$$\Delta \phi = \frac{0.9 \times 10 \times 2 \times 10^2}{5} = 360 \text{ maxwells}$$

where $N_2 = 5$, $R_2 = 10$, $T = 2$ microseconds, $I_2 = 0.9$ ampere.

The d-c hysteresis loop for this core (Fig. 3-2) shows a flux change of about 360 maxwells.

4.4 Preliminary Model

It was decided that a 2-dimensional selection system would be used in the switch. This would require 32 vacuum-tube drivers, 16 on each co-ordinate. It was felt that the saving in vacuum tubes in going to 3 dimensions would probably not be justified in this model. From the analysis of Chapter 3, the tube count would then be $4+8+8 = 20$, but the number of cores driven by some bias drivers would be as large as 64 and there would be an extra winding on each core.

Before building a full-size switch, a preliminary model was built using a plugboard layout with cores mounted on 9-pin bases and inserted in standard tube sockets. This model is shown in Fig. 4-2. It is a T-section of 31 cores representing a selected row and column, 15 partially excited cores in each line, and the selected core lying at their intersection. This model worked well giving very uniform outputs when different cores were plugged in the selected position. The primary turns used in this model were 25. This required driving currents of about 400 milliamperes on each line for a secondary current of about 900 milliamperes.

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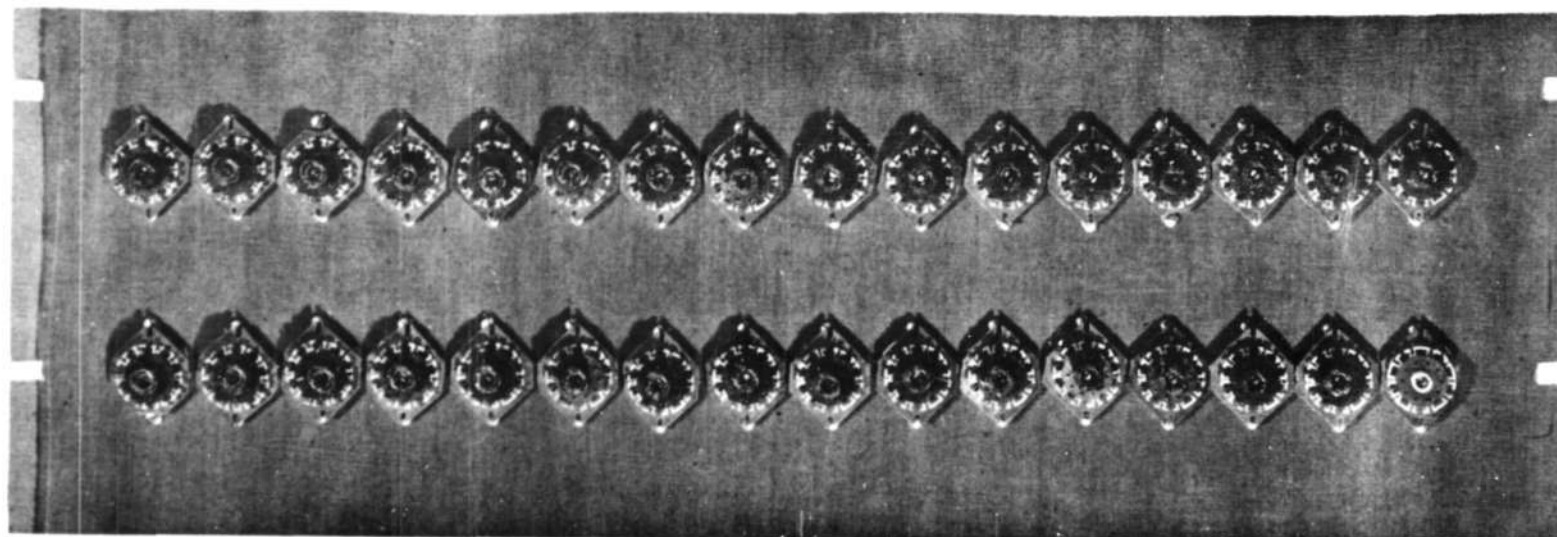


FIG. 4-2

SIMULATED T-SECTION OF 16 x 16 CORE SWITCH

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The back voltage which the vacuum-tube driver sees is made up of 2 components. One is the voltage of the selected core switching; the other is the primarily inductive impedance of the partially selected cores sliding on the flat portions of their loops plus leakage. In the plugboard model these 2 components had peak values which were within a few volts of each other.

4.5 Selection Logic

Two modes of switch logic were tested in this model and results compared. In both Modes I and II, a d-c bias current puts all cores at point 1 as shown on the loop of Fig. 4-3. An X and a Y line are excited, causing the selected core to move out to point 2, giving the read output. In Mode I, both X and Y drivers are turned off, and the core moves back to point 1, giving the write output. In this type of operation the write primary input is fixed by the bias and cannot be smaller than the read. This is evident from the 3 equations below:

$$B \geq X = Y$$

$$R = f(X + Y - B)$$

$$W = f(B)$$

The first equation states that the amplitude of the bias is such that neither the X nor the Y alone is sufficient to drive the core into the positive magnetomotive-force region. This is assumed in order to keep the noise outputs as small as possible.

The second and third equations say that the read and write currents are, respectively, the result of applying net magnetomotive force to the core primary of the amount indicated functionally in the parenthesis.

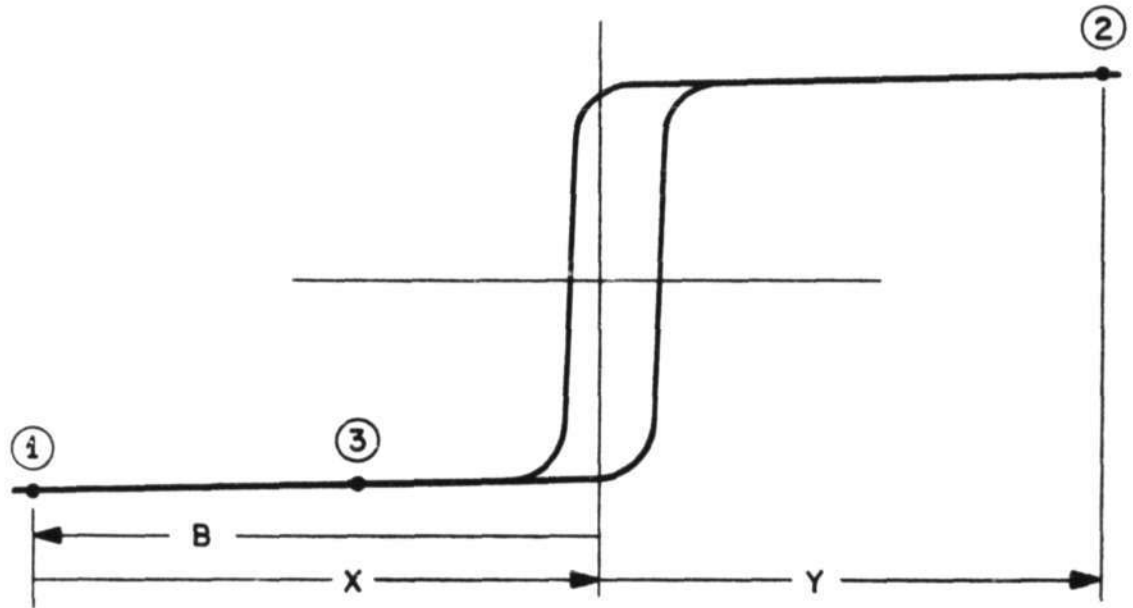


FIG. 4-3
OPERATING PATH OF CORE IN MODES I & II

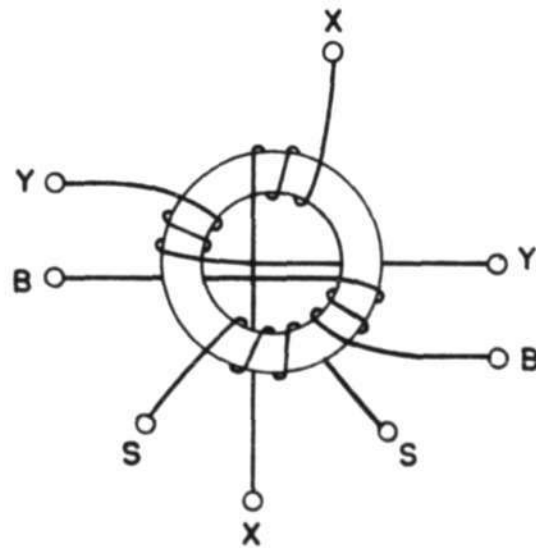


FIG. 4-4
ARRANGEMENT OF WINDINGS ON SWITCH CORE
SHOWING X, Y, BIAS AND SECONDARY

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Combining these equations, it is seen that the write is the result of a primary excitation equal to B, whereas the read is due to an excitation equal to or less than B. Therefore, it is difficult to obtain a read output which is larger than the write. Another disadvantage of this mode is that the fall time of the X and Y drivers determines the rise time and, hence, shape of the write output.

In Mode II, a separate driver pulses the core back to some point 3 which need not coincide with point 1 (the X and Y drivers remain on). This means that the read and write amplitudes are completely independent of one another. The main objection to this mode is that it requires an extra dynamic driver in parallel with the d-c bias driver. The design of a dynamic current amplifier for this job is extremely difficult, because it drives all the cores in the switch and the back voltage would be tremendous for any usable rise time. In the T-section tested, it was possible to operate in this mode because only 31 cores were driven by the dynamic driver. However, calculations showed that it would prove impractical in the full-scale switch. Another disadvantage is that the duty cycle on the X and Y drivers is twice that of Mode I.

The 256-position switch was designed with a greater number of primary turns (40 instead of 25) to lower the driving-current requirements. This increased the back voltage, but it was still possible to operate successfully. It is fairly close to the maximum number of turns that can be put on this size core conveniently. Fig. 4-4 shows the arrangement of windings on cores in the final switch.

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4.6 Noise

Inductive and capacitive coupling are minimized in this type of memory because the driving lines are perpendicular to the plane of the sense winding.

The number of memory-core outputs on the sense winding due to partially selected cores in the switch is the same as in a vacuum-tube-driven 2-dimensional read; 15 on a selected row and 15 on a selected column. On a 2-dimensional read the memory cores are driven with half-amplitude pulses. In this memory they are excited by the noise outputs of the switch which ideally would be zero. These excitations are small enough to assume that the memory core operates well down in the linear region and that the voltage across the memory varies as the derivative of this noise pulse. On the plugboard model, the noise currents from the switch were measured, and the assumption that the memory core voltage was the derivative of the exciting current multiplied by the slope of the hysteresis loop near zero magnetomotive force was borne out by the calculations and experimental results for 30 cores in using a value of L equal to 0.003 volt-microsecond per ampere. This yielded a peak noise of 0.01.

4.7 Current Drivers

The d-c bias current which passes through all the cores was supplied from a current amplifier using 6CD6 tubes. The bias winding carrying this current had 20 turns.

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In order to save time the X and Y drivings and selection circuits used to drive the first metallic-core memory arrays were adapted for driving the switch.¹⁸ The basic circuit as revised is shown in Fig. 4-5.

The main revision in the circuitry is the paralleling of the read and write drivers of the old system so that there are two 5687's or 4 cathodes on each drive line. Since the switch operation does not require separate write drivers there is no need to add any cathodes. A single 5687 could probably supply the current needed if the frequency were kept low enough, but since the extra cathodes were already installed in the setup it was decided to make use of them in case it was desired to go up to higher frequencies without undue dissipation in the drivers. This circuit employs a single common cathode resistor to obtain the high output impedance required of the current drivers. The read switch (Fig. 4-6) is essentially a low-impedance source which is used to hold the drivers cut-off by applying a large positive voltage across the common-cathode resistor. Removing this voltage allows the tube whose grid has been selected by the crystal matrix (Fig. 4-7) to conduct at the proper time. The matrix is driven by flip-flops shown in Fig. 4-8.

4.8 Memory Array

The memory was designed to have a 4-turn winding to be used for both inhibiting and sensing. This provides an increase in memory signal and a reduction in inhibiting current, each by a factor of 4. It requires a digit-plane winding which links the memory cores all with the same polarity. This is made possible by the very low noise level obtained with one-dimensional read selection. The increased space available inside

A-58804

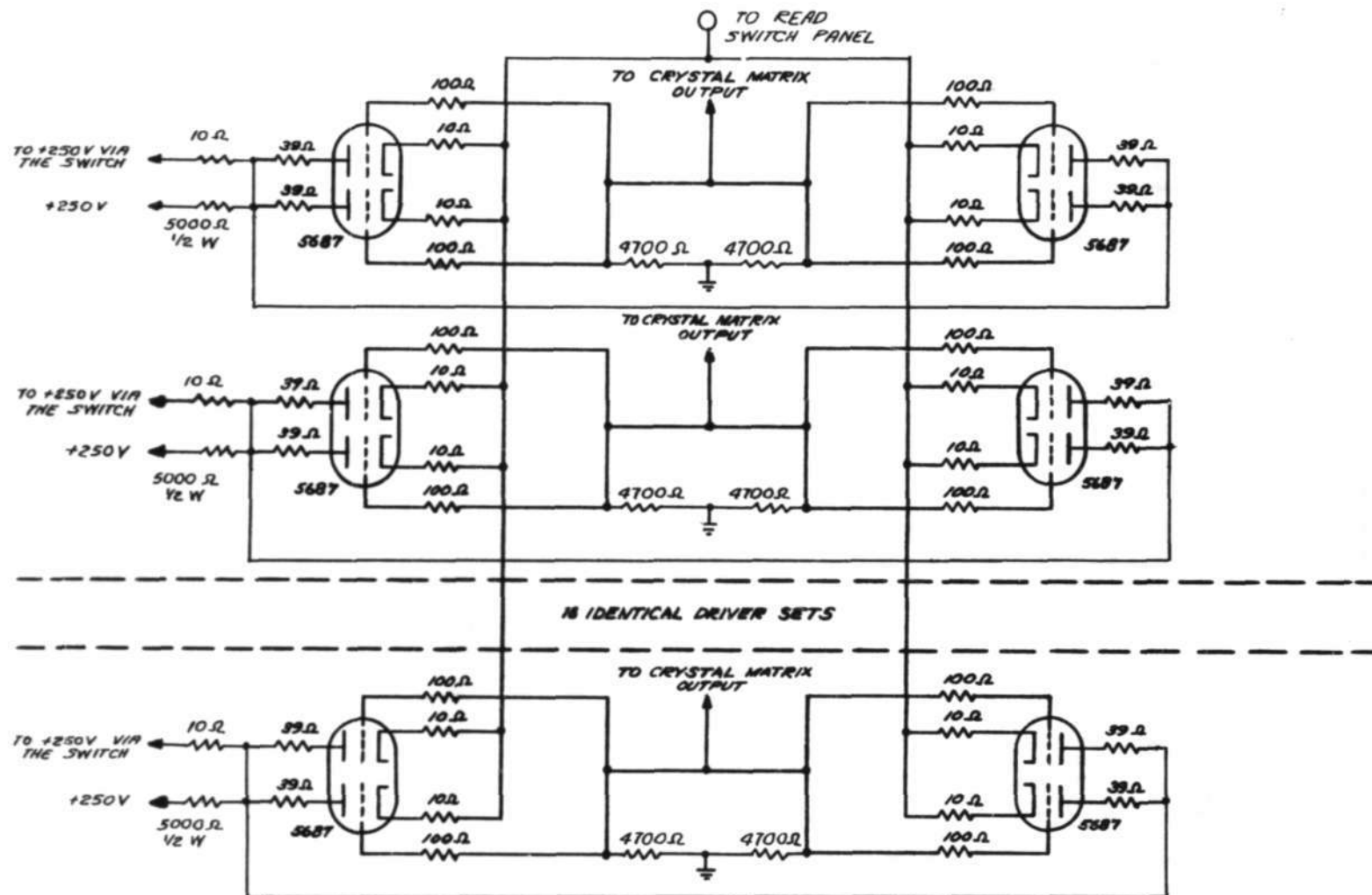


FIG. 4-5

X OR Y DRIVER PANEL FOR 16x16 SWITCH

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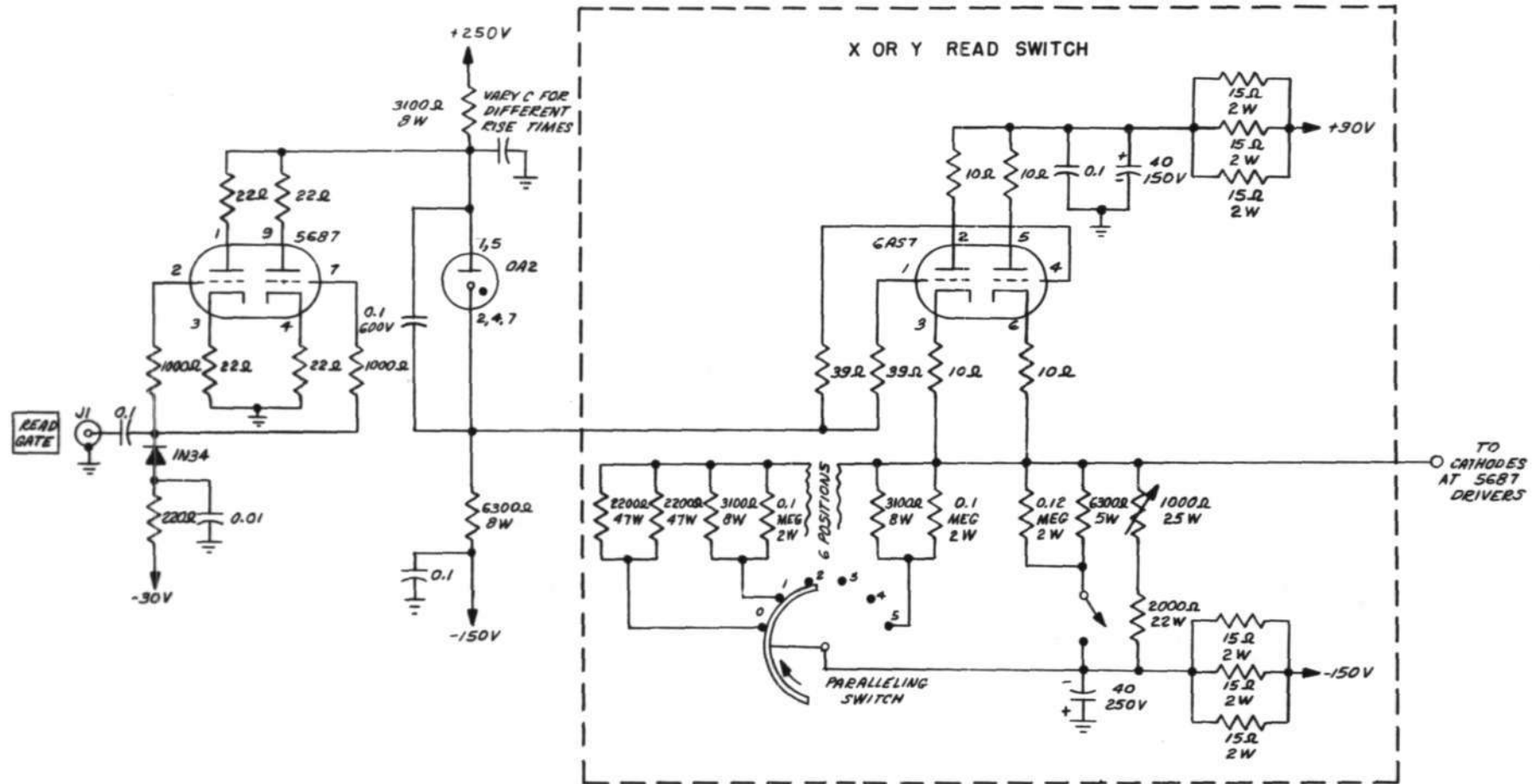
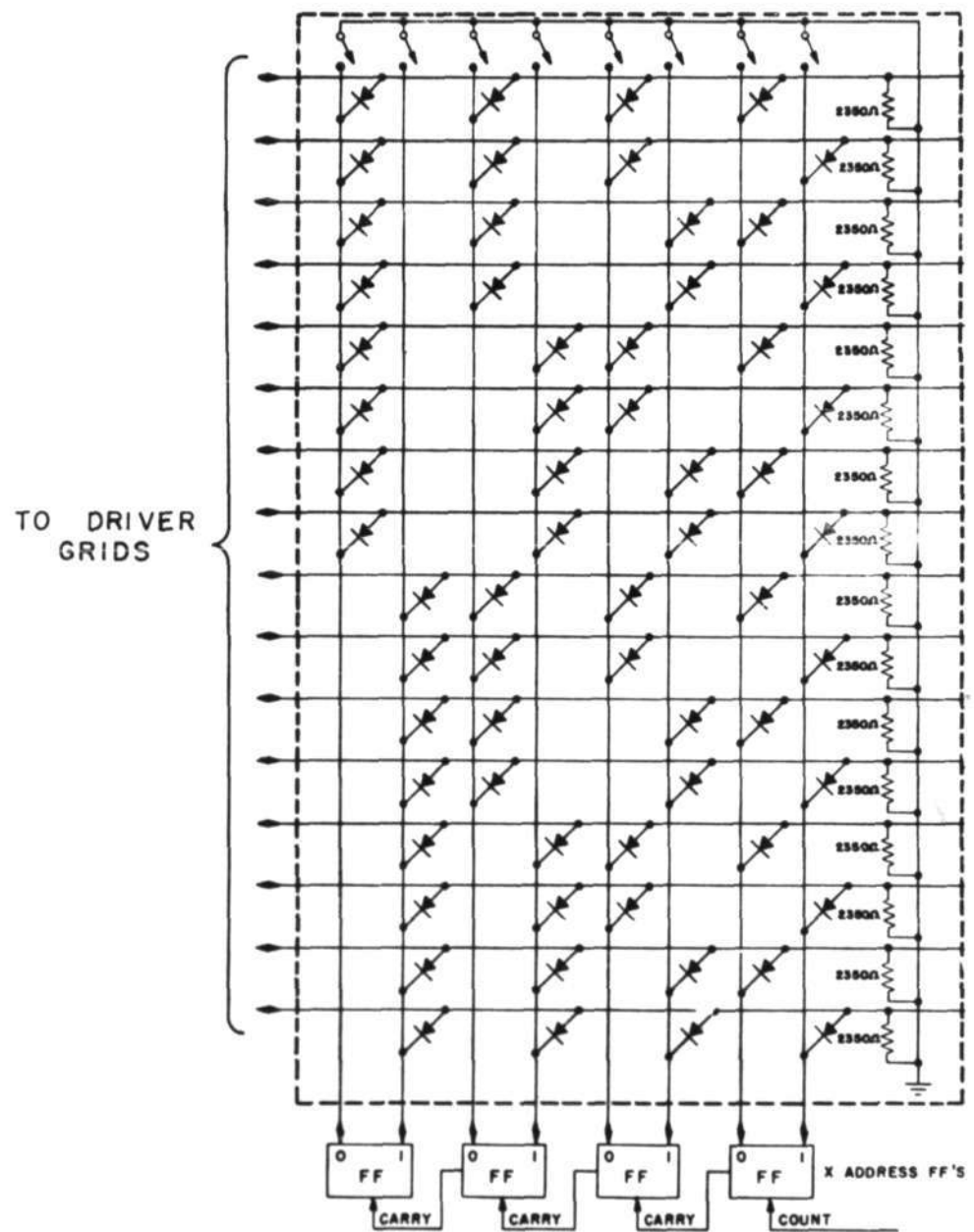


FIG. 4-6
CIRCUIT SCHEMATIC, READ SWITCH PANEL



NOTE:
ALL DIODES ARE IN34'S

FIG. 4-7

FUNCTIONAL SCHEMATIC
16 X 16 SWITCH X OR Y CRYSTAL MATRIX

A-52066

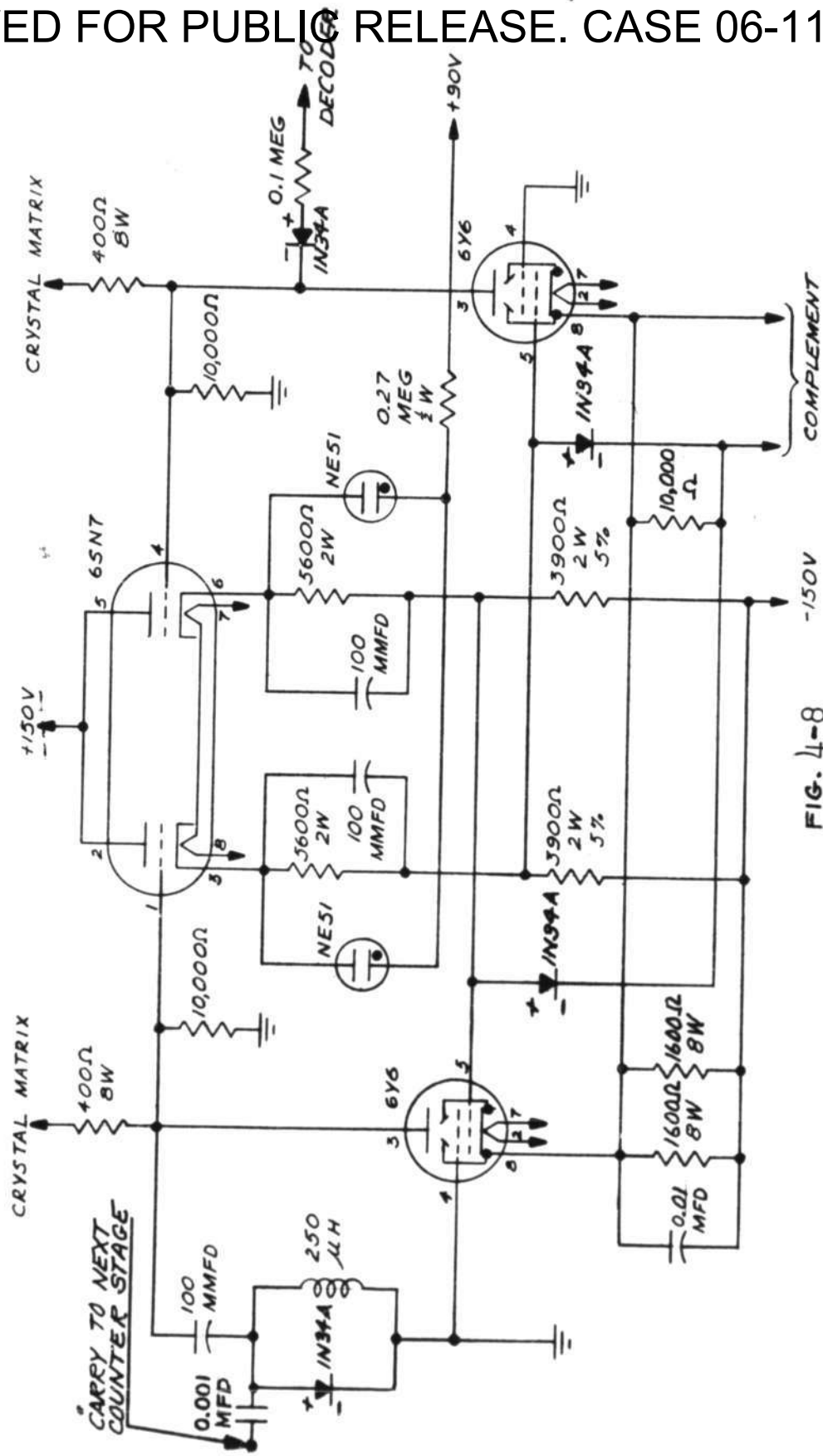


FIG. 4-8
CIRCUIT SCHEMATIC
ADDRESS SELECTION FLIP-FLOP

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the core because of the single driving line and combined driving and sensing on a single wire makes the insertion of a multiple-turn winding rather simple. In the actual wiring process the 4 turns were looped through the cores at the same time as 4 separate pieces of wire and then joined in series at lugs provided on the terminal strips.

The complete test system with logic, core switch, and memory is shown in Fig. 4-9. Memory-plane construction is also quite different geometrically from that used in the conventional MTC or WWI memory plane. The memory windings are shown sketched in Fig. 4-10. The matrix consists of 256 register lines in 2 layers of 128 each. Intersecting these are 16 digit windings of 4 turns each. Placing the register wires in 2 layers makes for compactness, allows each side of the array to be worked on separately, and permits the digit winding to close back on itself in a small-area loop, thus reducing pickup problems.

In a system of this type the very pedestrian but painful problem of what to do with the register line terminating resistors presents itself. It should be remembered that there is one of these for each output of the switch or, in other words, for each register of memory. If we assume a secondary current of about 1 ampere and a maximum duty factor of 50% for a given register, then the wattage dissipated in the resistor is given by:

$$\begin{aligned} P &= I^2 R \times 0.5 \\ &= R/2 \end{aligned}$$

where R is the resistance of the terminating resistor. For the design

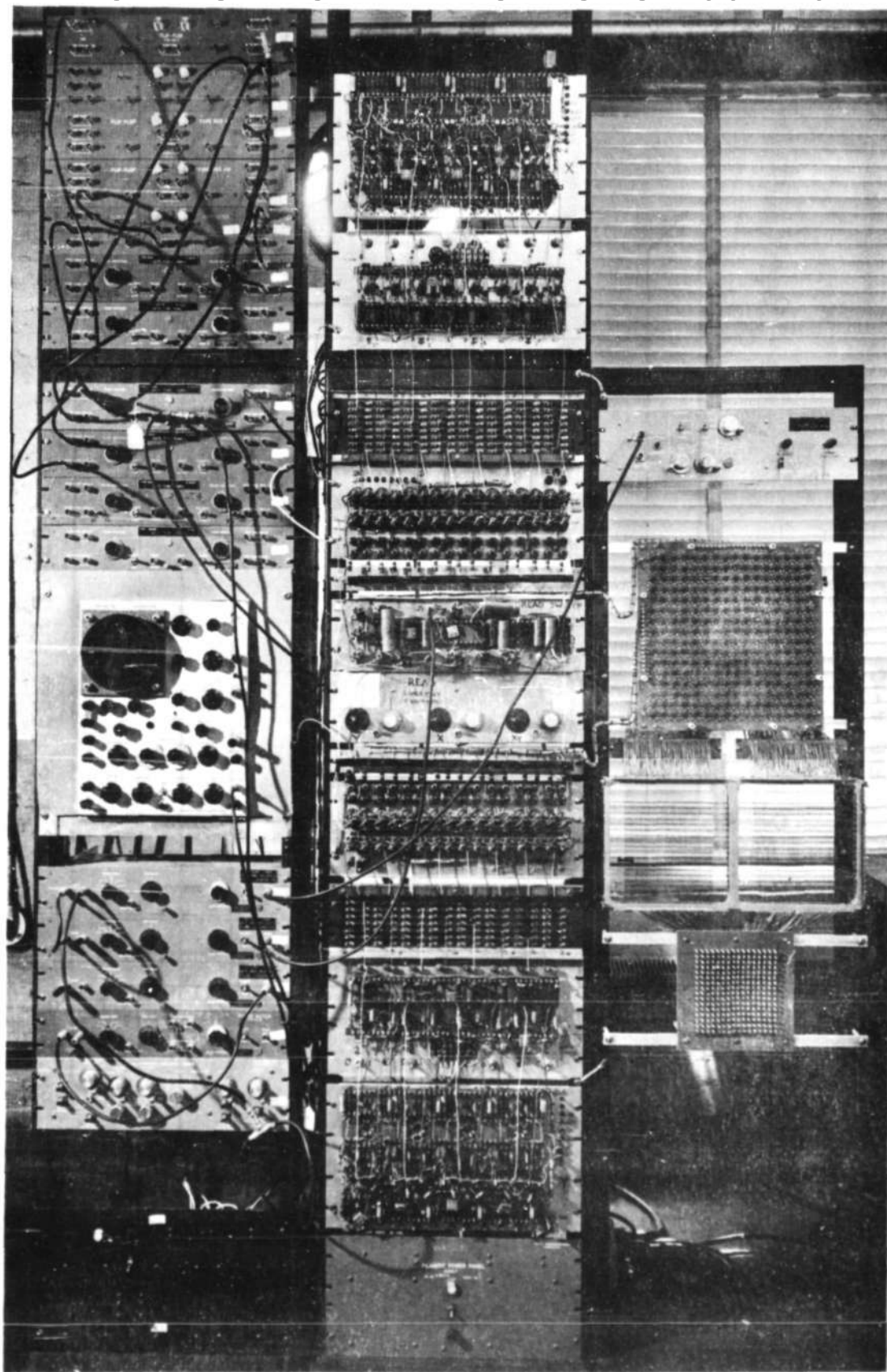


FIG. 4-9
MEMORY TEST SET-UP
WITH REGISTER SWITCH AND MEMORY ARRAY

A-58864

A-58850

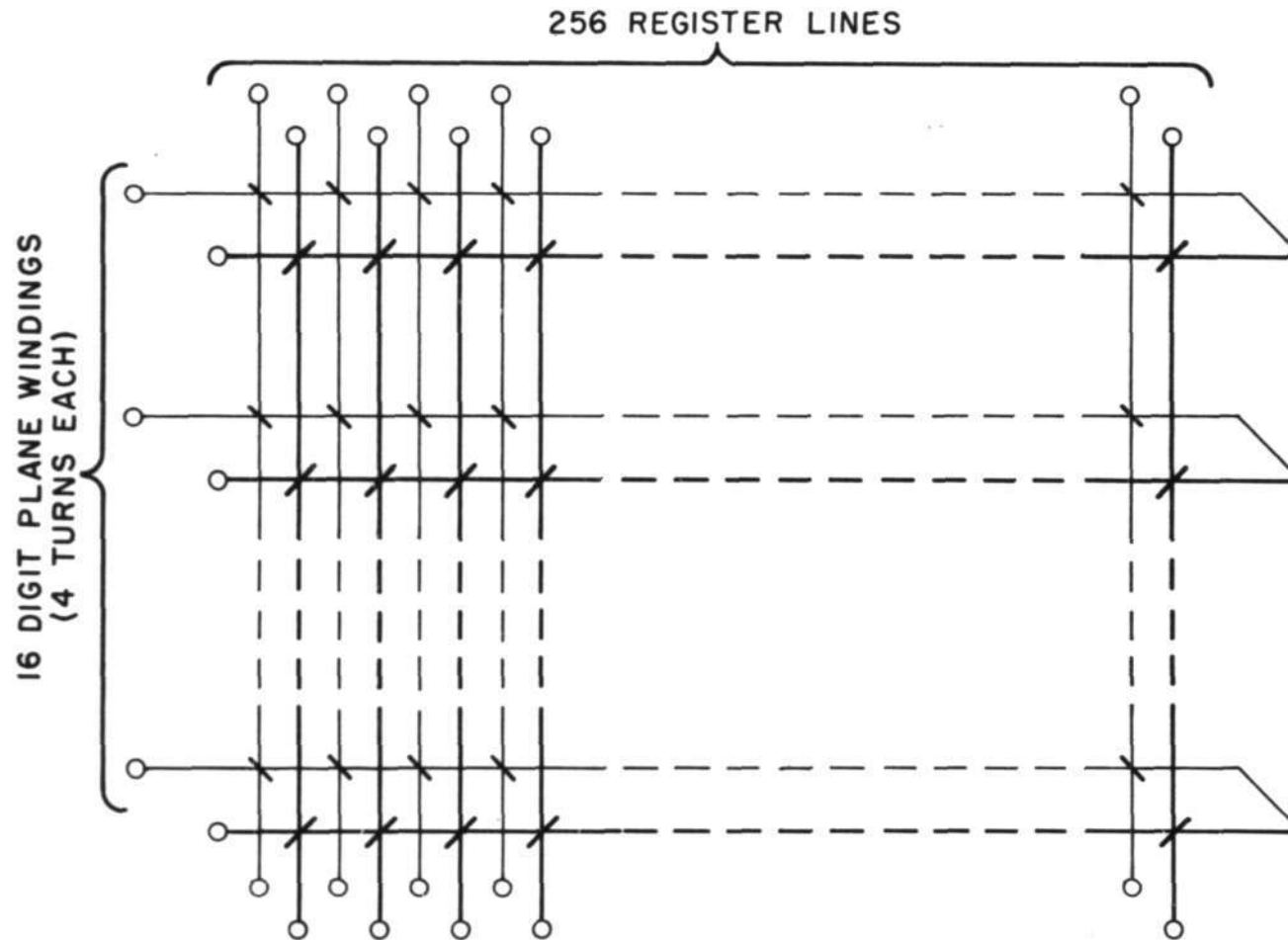


FIG. 4-10
MEMORY ARRAY

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considered here in which $R = 10$, this means 256 resistors each capable of dissipating 5 watts. Since this experimental model was planned to run at greatly reduced duty cycles, 2-watt resistors were used. In order to simplify measurement and trouble-shooting work, a phenolic board (Fig. 4-11) with a 16 x 16 square layout of lugs was used to fasten one side of each terminating resistor. The common side of these resistors was returned to a common-bus network located on standoffs attached to the phenolic board. In any final working switch of considerable size the location of these resistors is one of the most serious, albeit straightforward, problems that faces the designer. The most desirable solution would be to reduce the resistance to the order of 1 or 2 ohms requiring a dissipation of 1/2 or 1 watt, respectively. This could probably be obtained by using nichrome or other high-resistivity wire at some point in the register line. This, of course, requires a major change in the switch-core design. The problem is to maintain the same transformer output impedance and switching time when the secondary resistance is multiplied by a factor of x . The approximate solution is to decrease N_2 by a factor of x and increase ϕ by a factor of x^2 . This multiplies transformer impedance which is proportional to $N_2^2 \phi$ by x^2/x^2 or 1 and multiplies flux linkages which is $N_2 \phi$ by a factor of x^2/x or x . Since flux linkages should vary directly with secondary resistance for constant current and switching time, the basic conditions have been satisfied. It is important to realize that the above analysis only holds for the region in which the resistance is large enough so that the major part of the flux may be said to be dissipated in it, rather than the memory

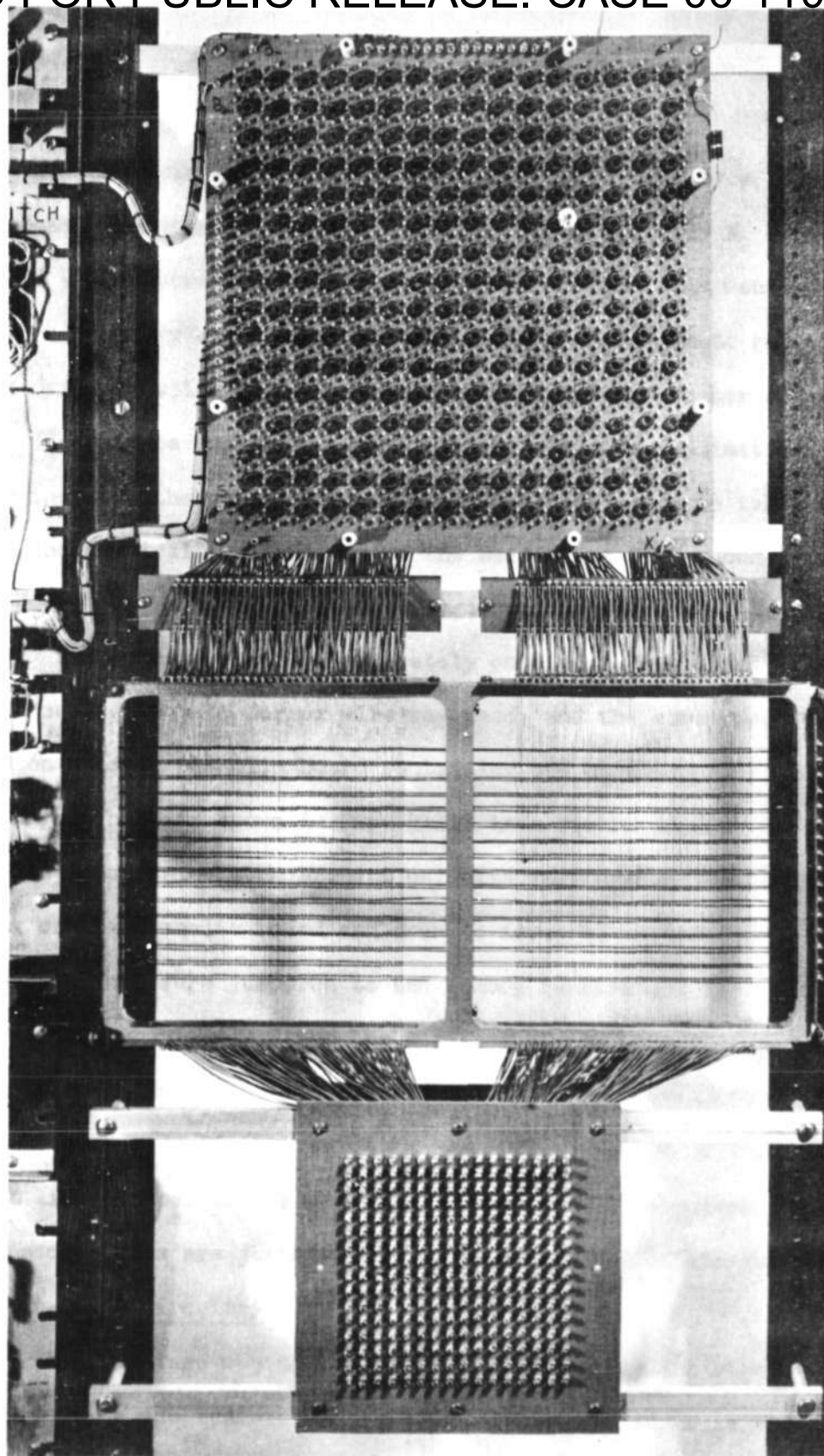


FIG. 4-II
256 REGISTER, 16 PLACE MEMORY
AND CORE SWITCH FOR REGISTER DRIVE

A-58863

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cores. If the resistance in the present case is reduced by a factor of 5 to 2 ohms, the approximate solution would be to multiply N_2 by a factor of 5 and decrease the flux by a factor of 25. This would yield a 25-turn secondary and would make it extremely difficult to get a decent current transformation without running to an excessive number of primary turns. It is to be emphasized that this is only an approximation, but it does indicate the general trend the design would have to take.

The physical construction of the switch was influenced primarily by the desire to have all cores readily accessible for replacement and testing. The cores were wound separately on a poor machine by some very patient people. No. 36 formex wire was used, and the cores were then mounted on a large phenolic board containing the thousand or so miniature solder lugs (which is shown in Fig. 4-11) in a square 16 x 16 layout. The switch secondaries were brought out with feedthrough lugs through the back of the phenolic board and down to terminal strips adjacent to the memory. They were jumpered to the memory terminating strips to which had been previously wired the register lines. The other ends of the register lines feed the resistor board. There is no return lead from the common ends of the resistor. The low impedance of the 255 non-selected lines in parallel makes this unnecessary. The common sides of all the secondaries are jumpered together at the back of the switch.

4.9 Digit-Plane Circuitry

Full advantage was taken of the 4-turn digit-plane winding to simplify sensing and inhibiting circuits. These are shown in Fig. 4-12.

C-58780

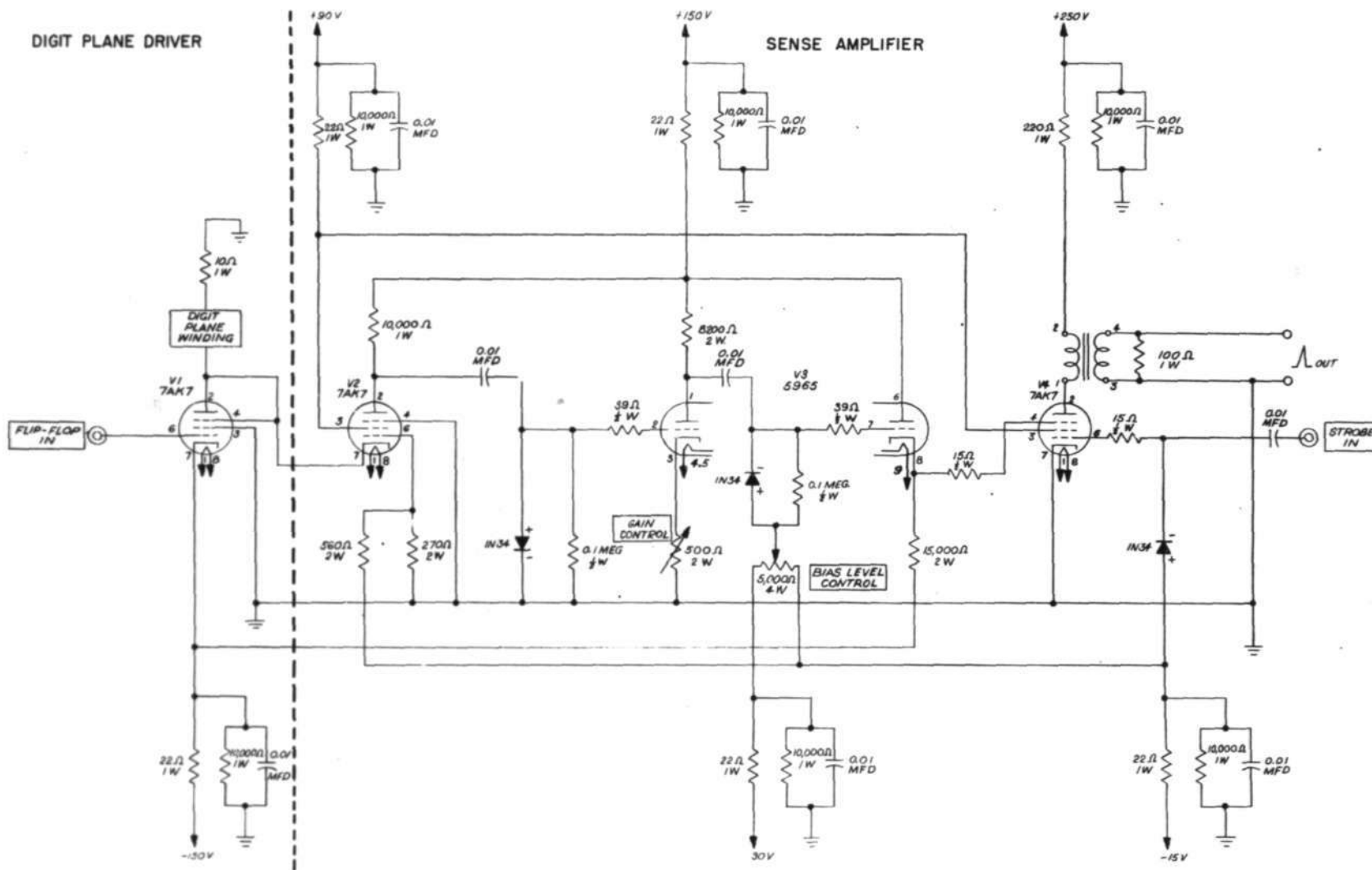


FIG. 4-12

DIGIT PLANE DRIVER & SENSE AMPLIFIER

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The digit-plane driver uses a single 7AK7 tetrode connected and is driven directly from a flip-flop.

The sense amplifier has 2 stages of amplification followed by a cathode follower and a gate tube used for strobing. The first stage is a grounded grid amplifier driven directly from the digit-plane winding. The low impedance of the winding makes this feasible; however, it introduces a quiescent current of a few milliamperes in the winding which is not too desirable but which is probably negligible. A grounded grid stage is used only because it provides the proper polarity at the gate tube after 2 stages of amplification. The stages are a-c coupled with a fairly long time constant. Blocking of the second amplifier stage is prevented by working the **first** stage close enough to cutoff so that large positive signals at the cathode drive the tube into cutoff and are, therefore, clipped. It should be noted that the sense-winding configuration used here produces unipolar ONEs so that the amplifier need not provide the symmetrical input and inversion stages needed with a canceling-type winding which produces bipolar ONEs.

The gate tube at the output of the sense amplifier is strobed by a 0.1-microsecond pulse applied to its control grid. The suppressor receives the amplified read output. A bias control on the suppressor controls the level of pulses which the gate tube will pass. This level is set just low enough to insure that no ZEROS pass through the gate tube.

4.10 Block Diagrams

The logic necessary for supplying the sequences of pulses needed to operate the memory is shown schematically in Fig. 4-13. The schedule

B-47110

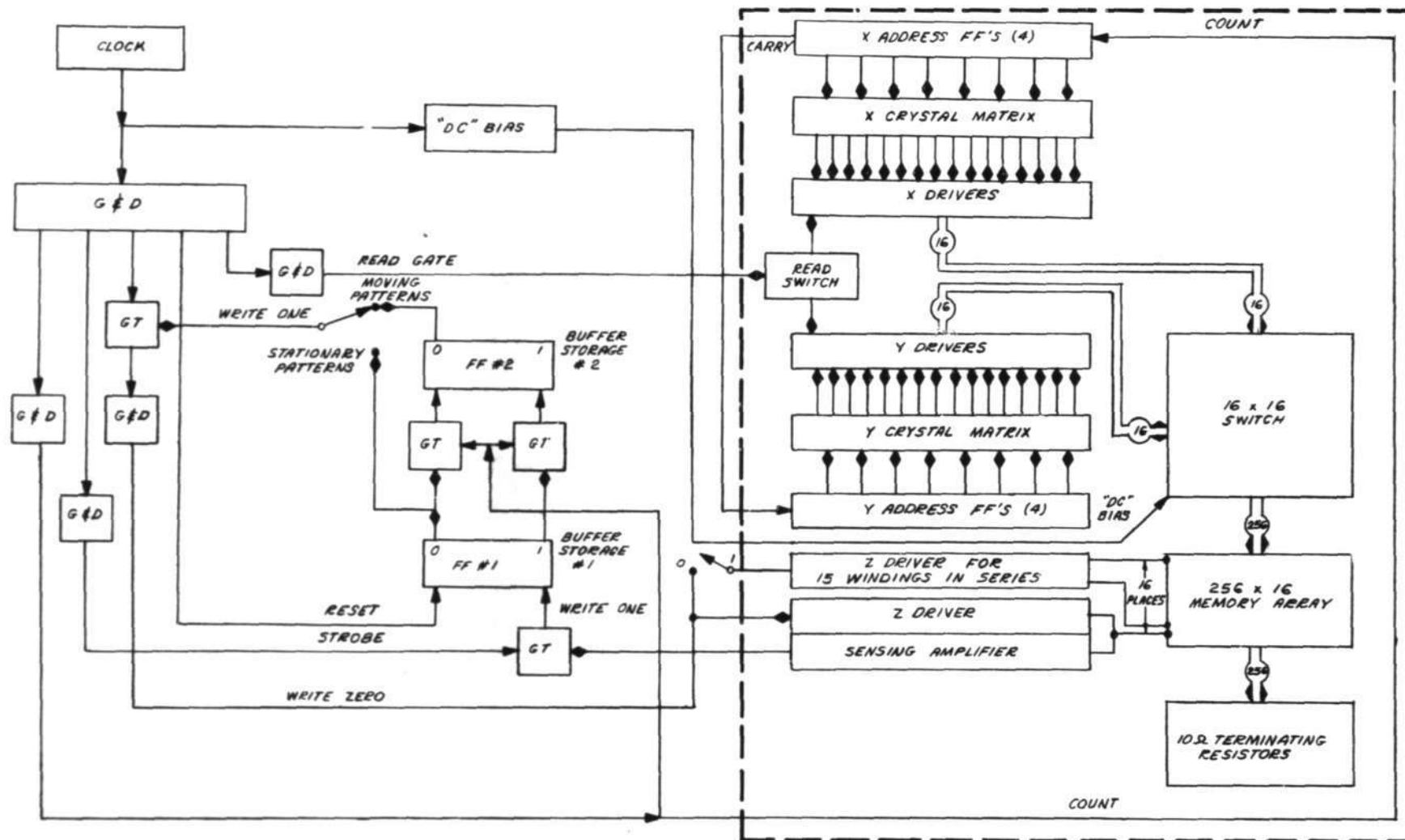


FIG. 4-13

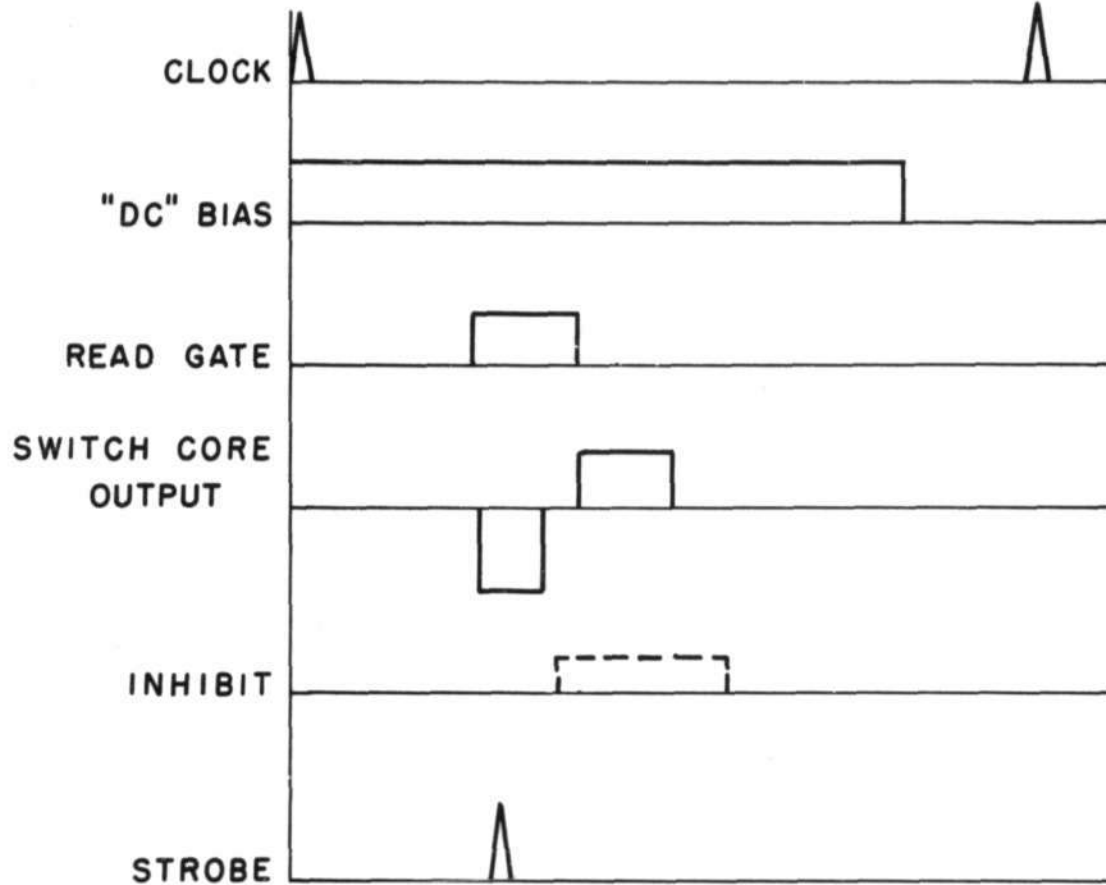
BLOCK DIAGRAM, BASIC TEST SYSTEM OF MAGNETIC MEMORY AND 16 x 16 SWITCH SHOWING CONNECTIONS OF DRIVERS AND ADDRESS SELECTORS

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of pulses is shown in Fig. 4-14. In this setup a single digit plane was operated at a time with sense amplifier and digit-plane driver. The other 15 were put in series with a common inhibit driver so that the full effect of the variation in load due to varying information in the other digits would be observed on the plane being tested. The logic is set up to address and read and write successively in the 256 registers.

The system is capable of having any arbitrary information pattern read in and out of the memory plane under test repeatedly or of causing a pattern of ONES and ZEROS to move through the array, shifting over, a register at a time. The information is displayed visually on a scope. The 16 x 16 array of spots is obtained from decoders operating from the address flip-flops and intensity-modulated by the output of the sense amplifier, a bright spot appearing wherever a ONE is stored.

In order to write in particular patterns such as the one shown in Fig. 4-15 it was not necessary to use a light gun as in previous memories. Instead, the memory is filled with ZEROS, and a clip lead from the common side of all the secondary resistors is touched to the appropriate lug on the resistor board corresponding to the position in which it is desired to place a ONE. This shorts out the secondary resistance and causes the register line current to become too large for the digit plane driver to inhibit successfully when writing ZEROS; as a result, ONES are written in every position to which the clip lead is applied, thus enabling any desired pattern to be written in the memory.



PULSE SCHEDULE
FIG. 4-14

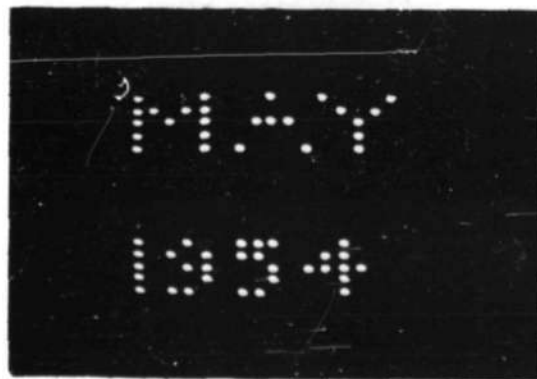


FIG. 4-15
PATTERN OF ONES
DISPLAYED ON OSCILLOSCOPE

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4.11 Experimental Results

The system described above was made to operate successfully although a number of setbacks were encountered in the course of the work. The most serious of these was the occurrence of short-circuits from windings to switch-core bodies due to the wearing away of the insulation during the winding of the cores. Another problem was the lack of uniformity in number of turns. These problems could be eliminated by a systematic winding technique on a good machine and by painting and sanding the cores before wiring.

A small conflagration, fortunately local, occurred when the switch was first put into operation. This was due to the shorts mentioned above. It was then decided to raise all the windings to the same potential so that the effect of the shorts could be minimized. Fortunately this measure has proved successful. In addition it was decided to run the d-c bias in a pulsed fashion. It is turned on and off far enough outside the operating cycle so that to all intents and purposes it simulates direct current. This is the reason that a 6CD6 amplifier is used. Ordinarily no vacuum tube would be required at all. A steady drain of about 400 milliamperes from the 90-v supply, for instance, could be obtained with the appropriate series resistance and a healthy choke could be put in series to guarantee a good current source. Since this current could remain on all the time, there would be no need to worry about the problem of pulsing it on and off through the large inductance. Such a panel has been constructed but has not yet been used. Pictures

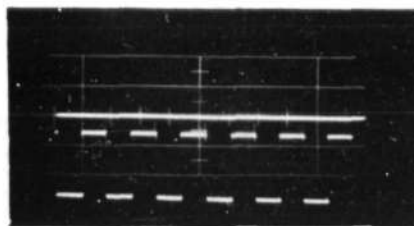
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of typical waveforms of the cathode and plate voltages of the X-Y drivers and the "d-c" bias output current are shown in Fig. 4-16. Inhibit-current waveform and diode-matrix selecting and nonselecting outputs are also shown.

The spread in memory-core outputs from all positions is shown superposed in Fig. 4-17. It shows both the 256 ONEs and 256 ZEROs. These were obtained by photographing the sense winding output for the case of a plane holding all ONEs and for that of a plane holding all ZEROs. It should be noted that there is a good deal more uniformity in the read output than in the write. This is thought to be mainly due to 90-volt supply ripple which is being eliminated at the present time. The large pulse during write times comes from the inhibit driver, when ZEROs are written. Also shown are the 256 ZEROs and ONEs at the output of the last stage of the sense amplifier. The ZEROs are slightly negative at strobe time. This is due to the fact that the 30 noise currents from the partially selected cores in the switch are decreasing in amplitude at strobe time and the memory-core noise outputs which are proportional to the derivative of this current are, therefore, all negative.

At this point it is helpful to consider the safe operating regions of memory cores used in different selection systems. B. Widrow¹⁹ has developed the concept of the shmoo as the safe operation region of any system which is a function of N variables. In particular, if we consider a memory with external register drive and assume a core having

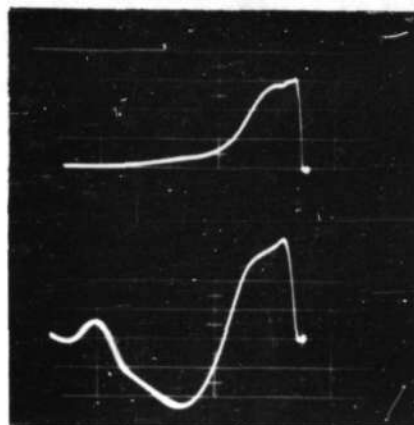
10 V / DIV.



500 μ SEC / DIV.

MATRIX OUTPUT
ALTERNATING
BETWEEN SELECTED
AND NON-SELECTED
LEVELS.

10 V / DIV.



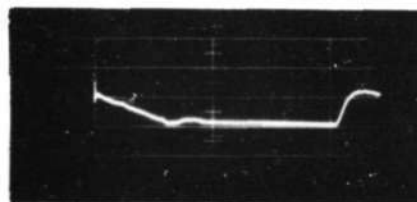
50 V / DIV.

1 μ SEC / DIV.

DRIVER
CATHODE

DRIVER
PLATE

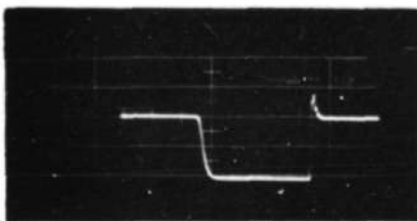
500 ma. / DIV.



1 μ SEC / DIV.

"DC" BIAS
OUTPUT

50 ma. / DIV.



1 μ SEC / DIV.

DIGIT PLANE
DRIVER OUTPUT

A-58819

FIG. 4-16
CIRCUIT WAVE-FORMS

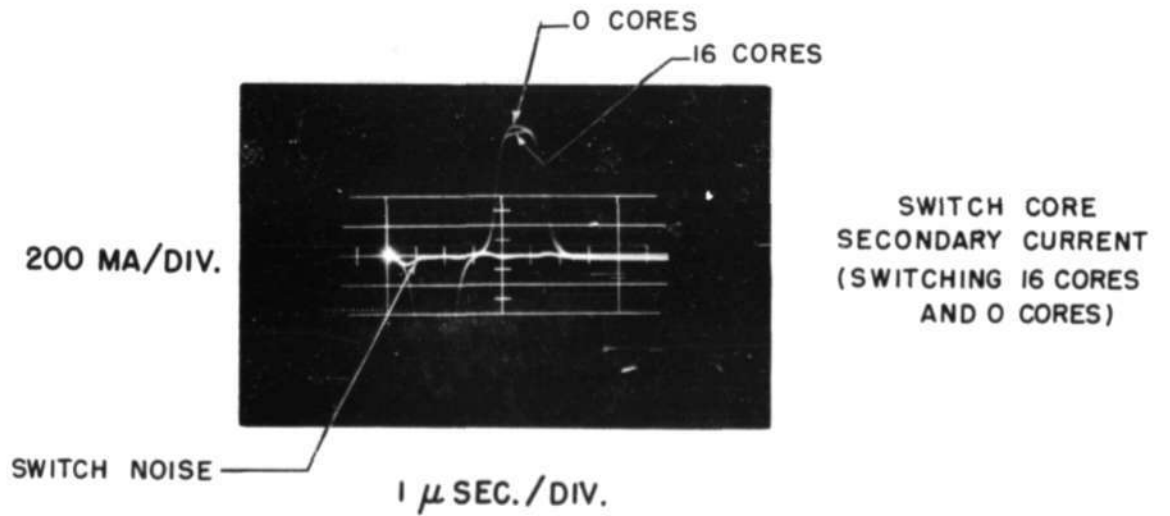
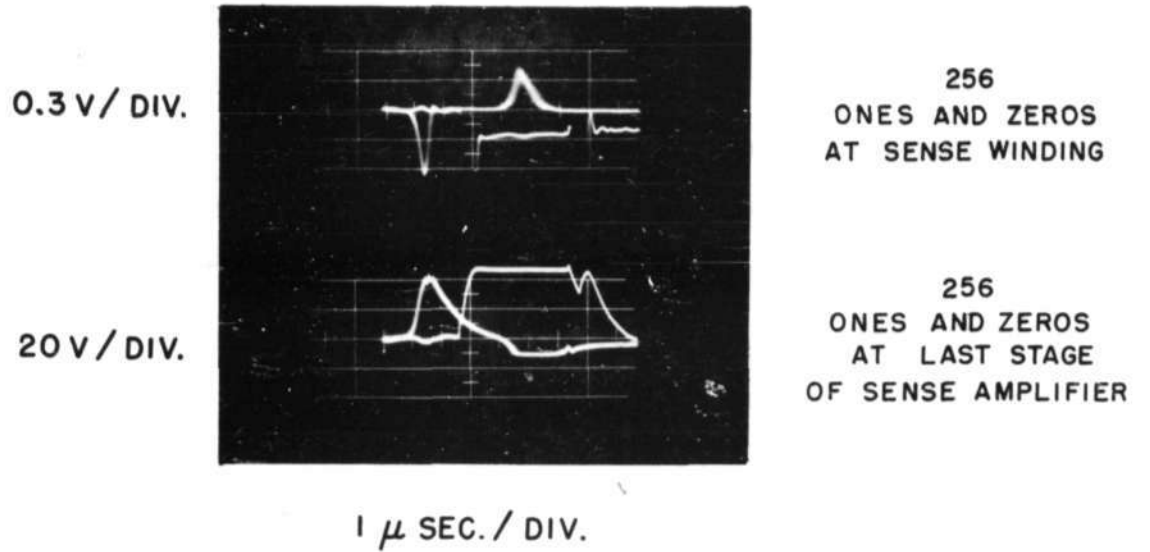


FIG. 4-17
CORE OUTPUTS

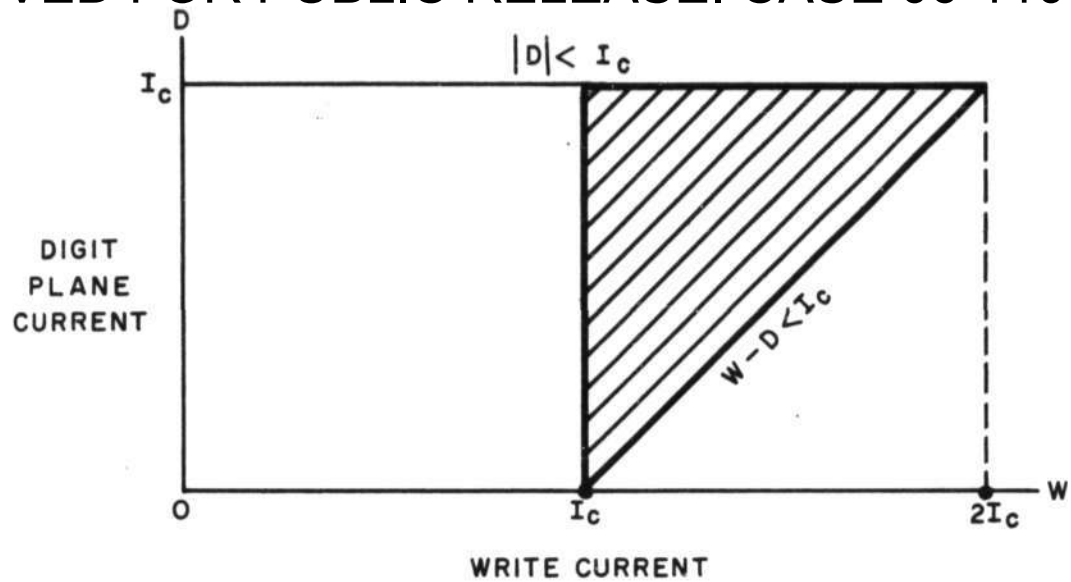
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an ideal loop, then the write operating shmoo for a single core as a function of write current, W , and digit-plane current, D , can be shown from the necessary conditions for 2:1 selection to be that shown in Fig. 4-18. Similarly, the shmoo for 3:1 write system is also shown. These figures illustrate the increased operating region which can be obtained with 3:1 selection. The system designed here has not been run at 3:1, but such operation should be attempted in order to get a full evaluation of its possibilities.

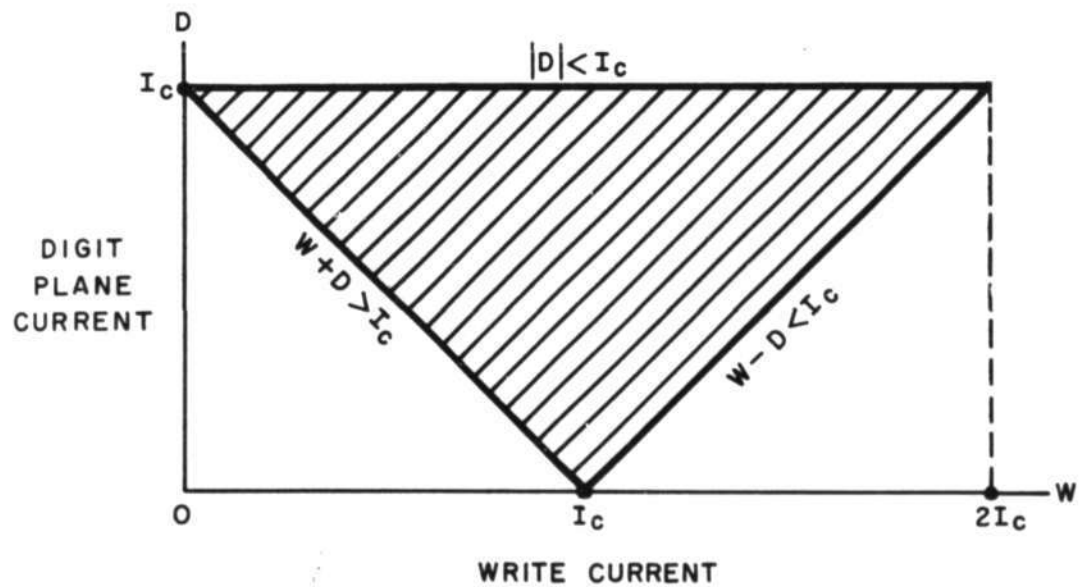
It is important to realize that with respect to a single digit plane there is no so-called worst pattern of information as there is in the conventional memory of the WWI. Experiments have shown that the noise outputs from the memory due to partially selected switch cores are too small to be significant in an array of this size even with a non-canceling winding.

A worst pattern, or what is perhaps better called a worst sequence, would involve the loading effect due to variations in the information in the remainder of the digits. The extremes of this effect would result from alternating all ONES or all ZEROS in the remaining 15 planes for various patterns of information in the plane under test. If the output impedance of the switch core is high enough, the secondary current will remain unchanged in the face of the changing information, and the variations due to this effect will be negligible.

Fig. 4-17 shows the current in the 10-ohm terminating resistor in a typical secondary line. The shape of the write pulse is helped by slowing down the fall time of the X and Y drivers with capacity at the



THEORETICAL SHMOO FOR IDEAL MEMORY CORE USING A "2:1" WRITE



THEORETICAL SHMOO FOR IDEAL MEMORY CORE USING A "3:1" WRITE

FIG. 4-18

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grid of the read gate. The picture shows the superposed outputs for the cases where first all ONES and then all ZEROS are written in the register; that is, for the cases when no cores are switched and when 16 memory cores are switched. The difference between the 2 is greater on the write than the read, a bite being taken out of the waveform when all 16 cores are switching; the difference is small enough so that margins should not be noticeably affected. The low trace appearing just above the base line is the partially selected core or "noise" output. The ratio between peak-signal and peak-noise outputs is somewhere between 15 and 20 to 1; at strobe time, it is considerably better than this. The read amplitude is about 1.2 amperes; the write about 800 milliamperes. It has been possible to get the write bigger than the read by working the unselected cores out closer to the knee of the loop and by slowing down the fall of the X and Y drivers to reduce the write current.

The core loss per read-write cycle for the MF-1312, F-262 core for a switching time of 2 microseconds is given by:

$$\begin{aligned}
 W &= 2 \times N_i (T)_{\text{NET. av.}} \times \Delta \phi \\
 &= 2 \times 2.5 \times 360 \times 10^{-8} \\
 &= 18 \times 10^{-6} \text{ joules/cycle}
 \end{aligned}$$

Assuming a maximum duty cycle of 50% for any nontrivial program the maximum power loss would be:

$$\begin{aligned}
 P_{\text{max}} &= 18 \times 10^{-6} \times 10^5 \\
 &\approx 2 \text{ watts}
 \end{aligned}$$

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Neither the driving circuits nor the cores (without some kind of forced-air cooling) would be capable of running at maximum duty cycle; therefore, no attempt was made to run at these speeds.

Precise measurements of margins were not taken because the driving circuitry did not allow wide variation in currents. However, with the read-write currents set as in Fig. 4-17 it was possible to store any arbitrary information pattern for a range of digit-plane currents from 80 to 140 milliamperes. In order to allow an unlimited number of disturbs for testing the upper limit in digit-plane current, the memory is filled with ONES, it is stopped at an address and a ZERO is forced in. If after remaining at the address for a number of seconds the counters are again allowed to address sequentially, the memory should hold all ONES (except for the address at which a ZERO was placed). The upper limit in digit current is marked by the point at which the first of the ONES is changed to ZERO.

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CHAPTER 5

CONCLUSIONS

Any comparison between magnetic-core-memory systems depends considerably on the state of development of core materials. One of the difficulties in evaluating the present system is that the cost and quality of memory cores in the near future is difficult to estimate. If cores are perfected to the point where uniformity and low half-select noise are no longer difficult or expensive to obtain, the major advantages of the system designed for this thesis over the 2-dimensional read will largely disappear. The results obtained with the system designed here indicate that the basic principle of the register switch for one-dimensional read is sound and that the main potential advantage, the reduction of noise, has been realized.

The noise problem in 2-dimensional systems increases directly with the size of the array. Unfortunately the experiences encountered in constructing the 256-position register switch make it appear that the extension of this system to sizes larger than 1024 registers (32 x 32) would probably entail some very serious construction problems because of the physical dimensions of the switch and terminating resistors and the large number of solder connections. In other words, for large memories, in which one-dimensional read is most advantageous, the register switch to provide it is hardest to build.

It is to be emphasized that complete tests have not yet been made. In particular, the possibility of running at 3:1, which might make a considerable difference in margins or core specifications, should be looked into. Also, the possibility of overdriving on the read to get

faster, larger signals has not yet been fully explored. The present driving circuits are not capable of producing the currents needed for this.

In general, it is felt that while this system has a number of desirable features such as reduction of tube count and greater memory-wiring simplicity, it is too early to say whether or not it will have any marked superiority over present methods as an economically competitive system.

So long as memory systems require the memory-core to perform part of the selection function it is difficult to see how memory-core specifications and the need for carefully controlled driving currents can be significantly reduced. This fact led to the suggestion of the system proposed in Appendix 1, and it is believed that with the development of more sophisticated wiring techniques this system holds the greatest promise for faster, more reliable computer memories.

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APPENDIX 1

CORE MEMORY USING EXTERNAL BIT SELECTION

A memory system in which the memory function (remanence) and the selection function (nonlinearity) are performed in separate cores may have the following advantages over the present (coincident-current) system:

1. Much broader tolerances on core acceptability
2. Reduced noise out of the memory array
3. Larger signals out of memory
4. Shorter memory access time.

Some of the costs may be:

1. Two or three times as many cores required
2. More complex construction problems

A.1-1. Statement of the Problem

Consider the problem of using switch cores to perform the selection function for a magnetic-core memory completely external to the memory cores themselves.

A.1-2. The Functions This Selection System Must Perform

It must be capable of subjecting any memory core in a selected register to either of two cycles:

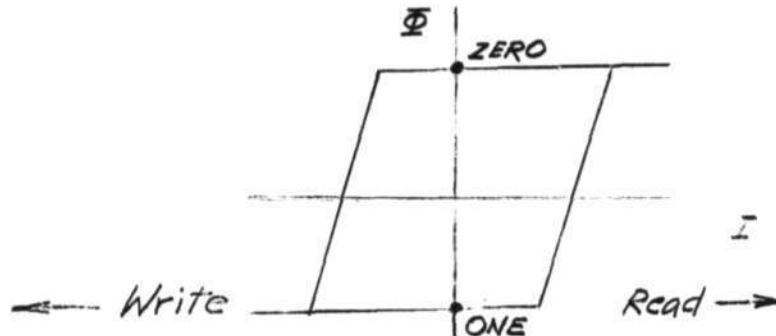
Read, Write ZERO (R-W₀)

Read, Write ONE (R-W₁)

without exciting any other cores in the array.

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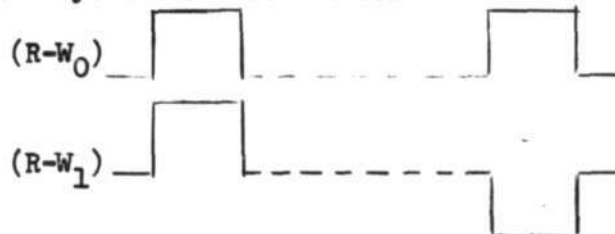
(A ZERO and a ONE are represented in the usual manner as shown on the hysteresis loop below along with Read and Write polarities.)



A.1-3. The Necessary and Sufficient Conditions Imposed on the Excitations Which the Switch Cores are to Provide to the Memory Cores

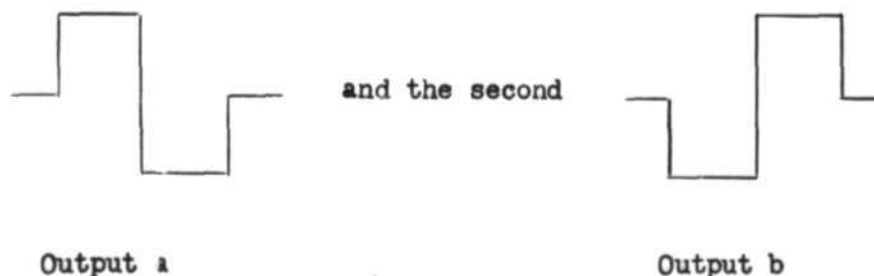
For cycle R-W₀ it is only necessary to have a sequence which has a first pulse plus and a last pulse plus.

For cycle R-W₁ a first pulse plus and a last pulse minus are required. These two cycles are shown below.

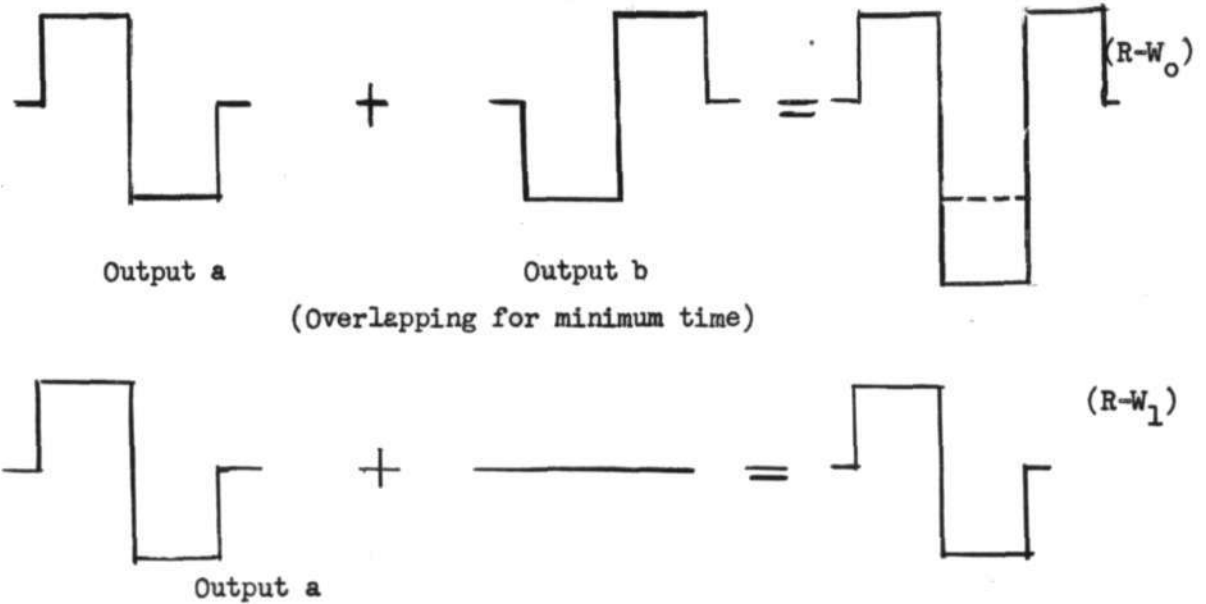


A.1-4. The Minimum Number of Cores Which Can Perform the Switching Function Outlined Above

Recall that a switch core must be reset to its original flux state before the start of a new cycle; that is a natural for R-W₁ cycle. However, the R-W₀ cycle cannot come from a single core; it could, though, come from the properly combined outputs of two switch cores, the first of which produced:



The two cycles desired can now be obtained as shown below:



It is also evident from above that the minimum number of switch cores needed is one core per register to supply output a (all the cores in the register receive it) and one core per bit to supply output b (each core in the register may or may not receive this depending on whether a ONE or a ZERO is being written).

A.1-5. Operating Characteristics

By completely separating the switching and memory functions the cores are no longer restricted to the critical requirements on driving current and hysteresis-loop squareness imposed by coincident-current operation. The main requirement of the switch core is that it be saturable; of the memory core, that it have two distinct remanent-flux states.

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In addition to reducing the core-uniformity requirements this system makes possible increased signal outputs, shorter cycle times, and reduced noise.

A.1-6. Physical Realization

The main problem in constructing a memory of this sort is the increased wiring complexity which results from driving each memory core individually rather than from common lines. This requires small coupling loops linking pairs of cores, and these may be difficult to fabricate unless done perhaps by machine.

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APPENDIX 2

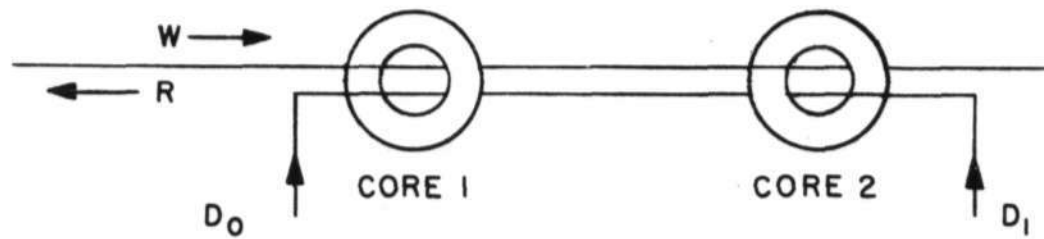
TWO-CORE-PER-CELL MEMORY

A.2-1. Operation

The two-core-per-cell memory was first proposed by K. Olsen.¹⁵ It involves the use of a register switch for selection with all its consequent advantages and materially simplifies the design and construction of the switch. The scheme may be best understood by considering the diagrams below. Fig. A.2-1 shows the two cores representing a single storage cell. A register wire goes through both cores in the same direction. A digit wire linking all the pairs of cores comprising a single digit plane goes through each of the cores in a cell in opposite directions.

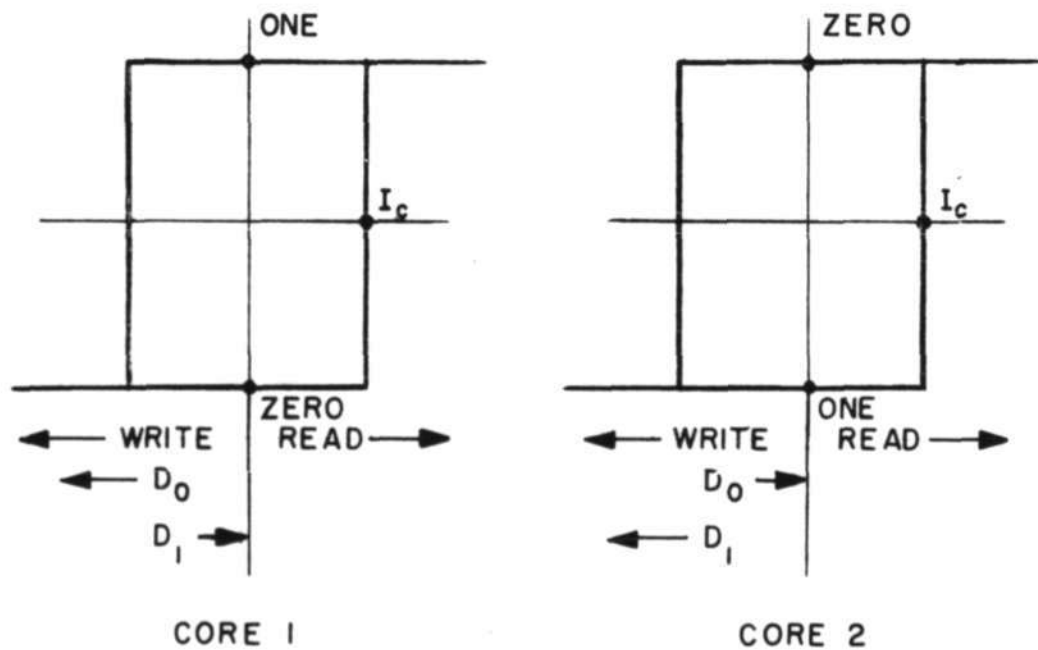
Fig. A.2-2 shows the hysteresis loops of the two cores with the direction of the read and write pulses coming from the register line indicated.

During the read process, both cores are driven to the tops of their loops by the register excitation, R. On the write the excitation W tries to drive both cores to their lower flux states. At this time it is possible to prevent either one of the two cores from switching by applying current D in one direction or the other on the digit winding. This, of course, is because the digit winding links the cores in opposite directions so that one core receives $W + D$ and the other $W - D$. Thus, when writing, one core switches from the top to the bottom of the loop while the other core remains at the top. A ONE can then be defined as core 1 in the upper state and core 2 in the lower as shown in Fig. A.2-2.



TWO-CORE CELL

FIG. A2-1



HYSTERESIS LOOPS SHOWING OPERATING PATHS
FOR EACH CORE IN TWO-CORE CELL

FIG. A2-2

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A ZERO is then core 1 in the lower state and core 2 in the upper. If the digit winding is used for sensing a ONE output will be made up of a large voltage from core 2 switching minus a small voltage from core 1 being driven further into saturation. A ZERO will be a similar output in the opposite direction. Each digit plane then has two drivers, one for supplying current D_0 to write ZEROS and the other which supplies D_1 excitation for writing ONES. The polarities of these excitations with respect to the cores and their loops are shown in Figs. A.2-1 and A.2-2, respectively.

It is important to note here that D_1 and D_0 cannot exceed the knee of the hysteresis loop; otherwise, information in other cores in the plane may be destroyed. It is also clear that W must be limited in size in order to be able to inhibit successfully the core that is not to be switched on the write. This limit is the same as for the conventional selection systems, i.e., twice the excitation to the knee of the loop, and the maximum selection ratio is 3:1 which is the best possible for two-dimensional selection.

A fundamental characteristic of this scheme is that one core always switches for each digit in the register both when reading and writing, independent of the information stored. In designing a switch to drive such a memory it is no longer necessary to consider current regulation under varying memory load. This means that clumsy and inefficient secondary resistance and large numbers of secondary turns are no longer necessary. What is required is that the switch core have just enough flux (assuming leakage is very small) to switch one memory core

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per digit.

The most obvious advantages of this system in addition to those previously considered for external register selection are:

1. As large as 3:1 selection on the write;
2. Positive ONES, negative ZEROS;
3. Simpler switch construction.

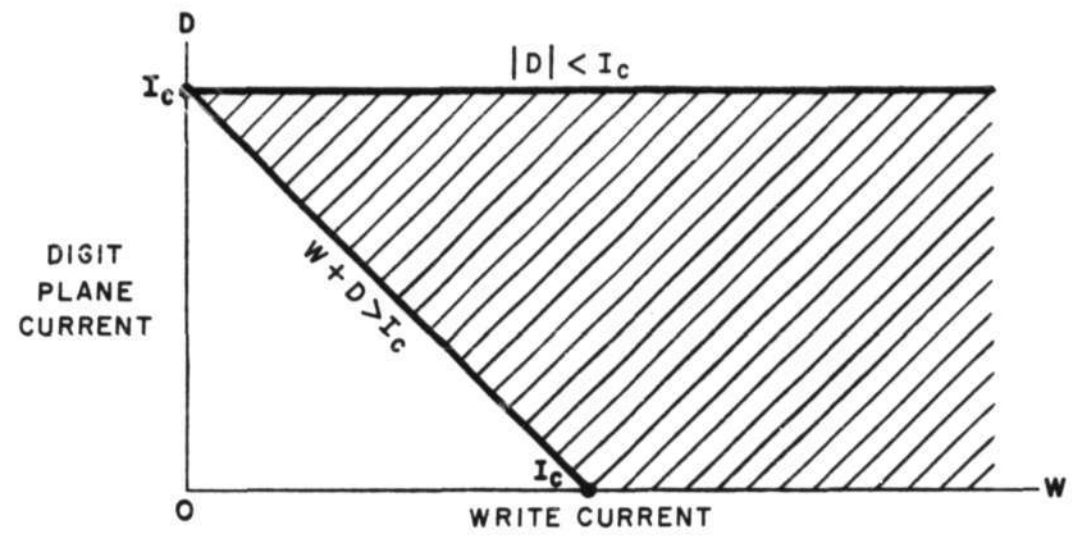
The costs are:

1. An extra driver and winding per digit plane;
2. Double the number of cores.

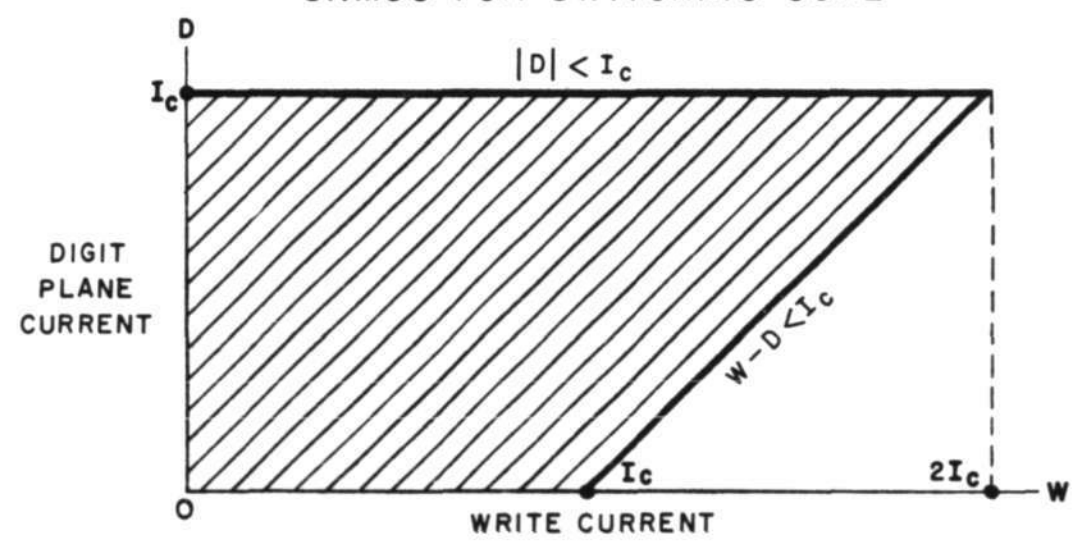
The ideal shmooos for each core in the two-core cell scheme are shown in Fig. A.2-3 as the two cross-hatched areas. A composite shmoo for the whole cell would then theoretically be the area common to both. This would yield an operating area identical with that of single-core-per-cell, 3:1 selection scheme.

There are two factors which make the above picture somewhat unrealistic:

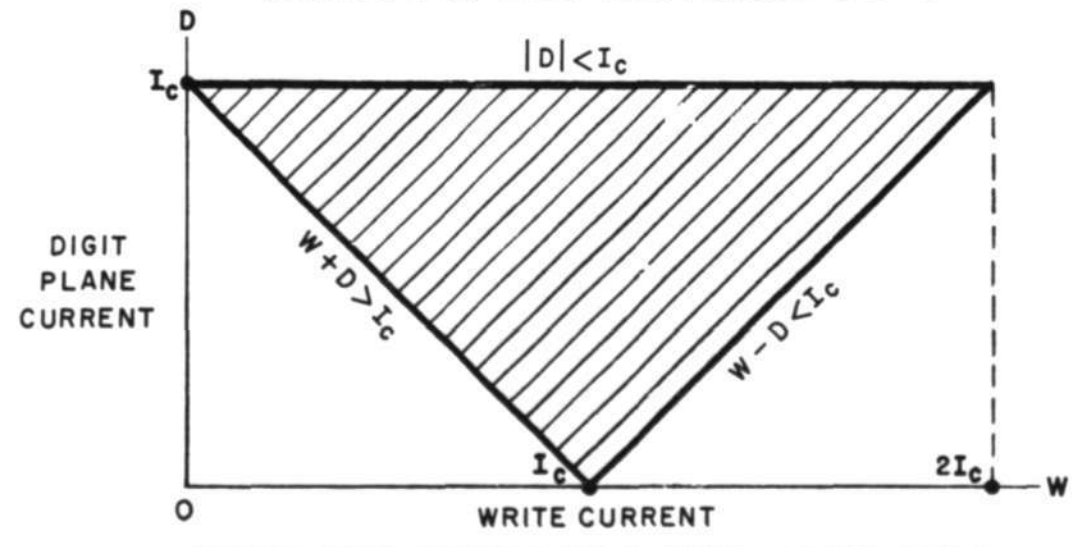
1. The current in the register is supplied by a core rather than a vacuum tube and, therefore, comes from a fixed flux source.
2. The ideal loop postulated above differs from the actual d-c loop and is even further from that which the memory core follows under pulsed conditions.



SHMOO FOR SWITCHING CORE



SHMOO FOR NON-SWITCHING CORE



COMPOSITE SHMOO FOR TWO-CORE CELL

FIG. A2-3

A-58833

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A.2-2. Experimental Work

In order to make a preliminary evaluation of this system the following series of experiments was performed.

Two registers were constructed each containing 32 two-core cells driven by a switch core. Two digits each had their own D drivers, the other 30 were connected in series and had a single pair of D drivers.

The switch cores were excited by a two-dimensional selection scheme similar to that described in Chapter 4. It simulates the operation in a full-size switch. A d-c bias is applied to all cores, and an X and a Y line are excited, the selected core switches providing the read pulse. A dynamic bias linking all the core then drives the core back, providing the write pulse. The X and Y drivers are then turned off, and the cycle is completed by turning off the dynamic bias driver.

The first experiments used 3 MF-1312 F-304 bodies for the switch core. This drove a register of DCL-370 cores fabricated at the Digital Computer Laboratory, a material which switches much more slowly than the switch cores. This resulted in operation which was far from optimum.

For switching times corresponding to less than 3:1 selection for the memory core, the switch core which is of a relatively fast switching material is operating at currents below H_m and does not, therefore, switch fully. For excitations greater than H_m on the switch core, the memory core will be forced to operate beyond its safe operating range which is three times the knee of the loop. This, of course, means that

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the memory core which is supposed to be kept from switching can no longer be successfully inhibited.

When a register of 1326-B cores was substituted for the slower switching memory cores, much more satisfactory operation was obtained, and it was possible to inhibit successfully the core in the cell which was to remain unswitched.

A great deal of data was taken with very encouraging results before it was discovered that by putting in sufficient disturbing pulses of the most adverse kind it was possible to destroy the information held in the register.

To understand the process by which information can be destroyed consider again the loops shown in Fig. A.2-2. In a switch having two or more dimensions of selection it is impossible to eliminate the small noise outputs from partially selected switch cores on both the read and the write. In addition, there is always the digit-plane current D , which partially excites the memory cores. It is only during the write process, however, that these two occur simultaneously. At this time the write noise pulse plus the D current which is in the write direction add and tend to switch both cores to the lower flux state.

It was found that even at low values of D current there was partial switching of the core due to this disturbing action.

Neither the D current nor the switch-noise output seemed to be sufficient to cause creeping up the loop but the combination of the two was sufficient.

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Three solutions readily suggested themselves at this point:

1. Using a switch core much closer to ideal;
2. Eliminating the D current which goes through the core in the write direction;
3. Placing resistance in the switch-core secondary to limit the current due to partial-select excitations.

A metal core was tried which has a much lower slope in the saturation region than the ferrite originally tested. This helped some, it took more disturbs to destroy the information.

The second solution still requires the use of two D drivers per digit plane but only allows a selection ratio of 2:1 as opposed to the 3:1 originally anticipated.

The third measure moves in a direction directly opposed to the motivation behind the entire two-core-per-bit system. It will be recalled that the original object of the scheme was to eliminate secondary resistance and the high flux, many turn, switch core this necessitates. Some resistance, perhaps, in the region of 1 ohm would probably be feasible. An attempt was made to put some resistance in the secondary. This had the additional attractive feature of allowing for the first time inspection of the secondary current feeding the register by placing a scope across this resistor.

It was found that the current spikes due to noise outputs in the switch were 300 to 400 milliamperes in amplitude. Since the current with no resistance in the secondary (except that of the wire) was probably a good deal larger, than this, it is not surprising that when added to the D current it was sufficient to bring the core out past

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the knee of the loop and hence to destroy information in the core.

A compromise solution might be to have the D winding link one core with two turns in the read direction and the other with one turn in the write direction. Thus, on the write the switching core receives $W + D/2$ excitation and the nonswitching core $W - D$. This yields a selection ratio of

$$R = \frac{2 + 1/2}{2 - 1} = 2.5 : 1$$

A.2-3. Conclusion

The two-core-per-cell system while undoubtedly leading to the simplest possible register-switch design requires double the number of memory cores and double the number of drivers per digit plane. It does not eliminate the problem of secondary resistance, and, so long as the 3:1 system is used, there is the possibility of destroying information even with large secondary resistance if, for instance, the switch noise output is of the order of 50 milliamperes peak.

In addition the lack of resistance in the secondary means that the readout noise may be rather high because of switch-noise outputs during read time. In order to take full advantage of the nonlinear characteristics of switch core and memory core in cascade it is desirable that there be sufficient decoupling impedance between the two. To some extent leakage inductance serves this purpose, but added resistance may be required to insure a low enough noise level. Since it is possible to build a register switch to drive a single-core-per-cell memory with as

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low as 10 ohms secondary resistance, as demonstrated by the results of Chapter 4, the two-core-per-cell memory would seem to be unjustified unless it could be made to operate with substantially less secondary resistance than this. The limited experimental results obtained here indicate it will not operate with 1 ohm and could probably operate using somewhere between 1 and 10 ohms.

APPENDIX 3

EQUATIONS FOR MEMORY SWITCHING SYSTEMS

Using the following equations to describe the general selection system of Fig. 2-2

$$\prod_{f=1}^F \mu_{fms} = \prod_{f=1}^F 2^{F_{ms}} = 2^{F_{ms}} = \mu_{ms}$$

$$\prod_{m=1}^M \mu_{ms} = \sigma_s$$

$$\prod_{s=1}^{S'} \sigma_s = C$$

It is found that:

Number of Memory Cores } = $\prod_{m=1}^M \prod_{s=1}^{S'} 2^{F_{ms}}$

Number of Switch Drivers } = $\sum_{s=1}^{S'} \sum_{m=1}^M \mu_{ms}$

Number of Matrix Buffers } = $2 \sum_{s=1}^{S'} \sum_{m=1}^M F_{ms} = 2 \log_2 C$

Number of Switch Cores } = $\sum_{s=1}^{S'} \sigma_s$

Number of Diodes } = $\sum_{s=1}^{S'} \sum_{m=1}^M F_{ms} \cdot 2^{F_{ms}}$

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