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Memorandum M-2511

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Division 6 - Lincoln Laboratory  
Massachusetts Institute of Technology  
Cambridge 39, Massachusetts

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SUBJECT: BIWEEKLY PROGRESS REPORT FOR LIN/FSQ-7 November 6, 1958  
To: J. W. Forrester, R. R. Everett, Division 6 Group Leaders  
From: A. P. Kromer, P. J. Gray

Building A Preparation

A request for additional building space for the XD-1 installation has been submitted to the Air Force by Lincoln. No decision has yet been reached. Various types of prefabricated buildings are being studied as a possible solution to the problem of having the building when needed. Current planning calls for a prefabricated structure containing a 17,000 square foot operational area with an 18-foot ceiling and a two-ply wood floor. A 12-foot-high crawl space beneath would provide sufficient room for air and wire ducts, air-handling equipment, SDV and display generator frames, and any refrigeration equipment that may be necessary.

Arithmetic Element & Control

The plans to rebuild the 4 digit arithmetic element model at IBM have been crystallized. It is expected that this model will be built in approximately two weeks, and will be tested and operational in two additional weeks. The A register will be simulated with toggle switches; the B register will be Burroughs test equipment. The adder and accumulator will approximate the physical arrangement and wiring layout using etched wiring and the pluggable unit plan anticipated in the final design. The control will also be Burroughs test equipment.

Memory

Further work on testing the 64 x 64 memory planes now being built for MTC will be necessary to permit final determination of the memory cycle time for XD-1. It is expected that this can be determined by approximately December 15. In the meantime, design should continue on the basis of the memory time being as fast as 6 microseconds, but work on drums should also recognize that the time may be as slow as 8 microseconds.

Memory Cores

IBM is taking emergency steps to make core testing facilities available so that they will be in a position to assume the full load of testing cores for XD-1 by about the middle of November.

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Drums

The general reexamination of the drum system with the objective of reducing tube count is continuing. As part of this study the following modifications of the drum system were studied:

1) Elimination of in-out break system

Equipment saved: 600--700 cathodes by eliminating IO Buffer, IO Register, Drum Control Register, Word Counter, Address Counter, a transfer path from LA Register to L Memory Buffer and miscellaneous cathodes in the Control Element. Cost in information-handling capacity: 3/4 second per 10 second frame.

2) Doubling or quadrupling number of registers per field

This might be done by increasing drum diameter or increasing information density on drum surface or both. If this can be accomplished within the AN/FSQ-7 time schedule, savings are estimated at 5500 ± 1000 cathodes. Cost in capacity: nothing.

Studies also indicate that the combination of several physical rotating drums into a single rack so as to facilitate switching of write, read and other electronic circuits seems to offer most of the potential savings that might be realized through the use of larger physical drums. This type of combination would avoid the necessity for doing development work on the larger drum units.

M-2494 will be issued by R. P. Mayer to report in detail on the estimated reduction in tube count through the various proposals now under study.

Input Equipment

Raytheon has submitted to IBM for approval a block diagram of the magnetic core part of the input counters which Raytheon will develop. This development is to be carried on in parallel with the present development at IBM.

An IBM-type magnetic-core counter is being built at MIT for a determination of margins. The stepping register for this counter has already been tested for sensitivity to drive-pulse variations.

The proposals made for manual inputs employing relay switching in the consoles have made it fairly apparent that relays are too slow, and more storage is needed for an efficient system. It has been proposed, therefore, that consideration be given to magnetic-core storage without relays so that the manual inputs will operate similarly to the radar input system.

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Display

Extensive testing of the Charactron tube with MTC has been underway for some time. Demonstrations have been conducted for various persons in Lincoln Laboratory and representatives of IBM. At a demonstration on Thursday, November 5, in Poughkeepsie, IBM presented their character generating system for consideration. At a meeting following this demonstration it was decided that the Charactron tube will be used in AN/FSQ-7.

The Charactron tubes now at MIT will be placed in consoles to make one permanently available to MTC and to have the second available at the Barta Building for study and demonstration in connection with the Cape Cod System.

It is expected that considerable attention will now be given to the matter of digital expansion now that the Charactron tube has been accepted.

Output Equipment

The recent meeting covering the study being carried out on outputs provided a decision to assign 4000 registers (2 fields) on the output buffer drum as available capacity for all weapons direction information. The amount and kind of information to constitute the output data for each type of weapon was also determined. Complete notes regarding this information are being prepared by D. C. Ross of IBM.

The output group is currently engaged in preparing the specifications for the output buffer drum.

Power Equipment

The systems offices at both MIT and IBM have been asked to look into the matter of input power frequency, and the degree to which this must be uniform. Exhibit AFCRC-1 indicates power frequency to be  $60 \pm 5$  cycles as one of the service conditions under which the system should operate. Although commercial power would not vary this much, this type of variation might be encountered during emergency operation with diesel generated power. The study is to determine the maximum probable frequency variation and its effect on the circuits and design of the system.

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Marginal Checking

Work is continuing on the division of computer control for marginal checking. The major portion of the work on marginal checking is being done by IBM. MIT reports M-2459, "Marginal Checking for Circuit Designers," and M-2469, "Marginal Checking without Shutdown" have been issued.

Signed: *A. P. Kromer*  
A. P. Kromer

Signed: *P. J. Gray*  
P. J. Gray

Approved: *N. H. Taylor*  
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