APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: A LINEAR SELECTION MAGNETIC MEMORY USING AN ANTI-COINCIDENT CURRENT SWITCH

To: N. H. Taylor

From: Kenneth H. Olsen

Date: May 8, 1953

Abstract: A linear selection memory in which each word is driven independently from a multi-position switch might have the following advantages over a coincident current memory:

1. No outputs from non-selected cores.
2. No limitation to memory size by delta voltages.
3. Large unipolarity output voltage pulses.
4. Possibility of operation on saturation ϕ-I loop.
5. Common z and sensing winding.
6. Simpler construction because only two windings are necessary per core.

An anti-coincident current switch which operates like the coincident current memory, but with the same lack of critical current adjustments as the magnetic matrix switch, is proposed to drive the memory.

Operation of Memory

It has been pointed out by several people that many of the problems in the coincident current magnetic memory would be simplified if each word in the memory were read out independently by driving that word with a single winding.* Selection is accomplished by a large multi-position switch each output of which drives all the cores in a single word in the read direction and causes an output from each core that held a one as in Figure I. The sensing winding in each digit is common to all the cores in that digit but it only picks up a signal from the core in the selected word because none of the other words were pulsed -- not even with half current. There are, therefore, no spurious signals from non-selected cores as in the coincident current memory.

This memory would use a coincident current write. To write in a word, half the current necessary to write a one is supplied to the whole word from the switch. In the digits where ones are to be written, another half current is

---

* IBM Report IM-5, G. E. Whitney

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

supplied and those cores will be driven to the one position. Where zeros are to be written no current is supplied by the digit winding. For 3:1 write, two-thirds I is supplied by the switch and digits to have ones are driven by + 1/3, and those to be left in the zero position are driven by - 1/3. In the first scheme it would be possible to make the memory of planes with only two single turns per core using the digit winding for both sensing and driving. With the 3:1 write, it would probably be necessary to have two digit windings, one for writing ones and one for writing zeros.

Because the read currents can be made very large, it is possible to get large and short pulses out from the memory. Another advantage of reading with large currents is that the memory cores are driven to saturation during read so that the core is on the saturation hysteresis loop. In the coincident current memory a minor hysteresis loop is used which is significantly less rectangular than the saturation loop. Figure 2 is a saturation loop of a ferrite and Figure 3 is the minor loop of the same core when used in a coincident current memory. Figure 4 shows the loop that might be traversed in a linear selection memory using 2:1 write ratio. With 3:1 write, the loop would be even more like the saturation loop.

Switch

The switch for driving linear selection memory should be a several thousand position switch. A magnetic matrix switch of this size would be difficult to build and a coincident current memory plane used as a switch would be difficult to use because of the critical current adjustments. The coincident current plane, however, could be used as an anti-coincident circuit with no critical currents. If the cores in the plane of Figure 5 are considered saturable transformers whose secondaries are the outputs of the switch, it is then necessary to select a certain core for each operation. If it is desired to select core F, then lines y_2 to x_3 are the selection lines for that core. To drive that core, all lines on the y coordinant are driven in the negative direction except the line passing through the selected core. Positive current is driven down only the selected line on the x coordinant. Only core F will have positive current and no inhibiting current and so will be switched. The currents are not critical and the positive driving current can be varied to obtain the desired waveform, just as long as the inhibiting current is always equal to or greater than the driving current.

Construction of Memory

Construction of the memory could be much simpler than that of the coincident current memory because there are only two windings per memory core. These would probably be put at right angles to each other as the x and y windings are in the present memory. However, the planes would be a different cross section of the memory cube. The physical arrangement of the planes is illustrated in Figure 6. The switch is in what is now considered the xy plane, but the memory planes are in the yz plane. In actual memory part of the switch might be built into the end of each plane.

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

Using Two Cores Per Bit

Each output of the switch must drive only n cores where n is the number of digits, but this load is variable because these cores hold an arbitrary combination of ones and zeros. To keep this load constant it may be desirable to have two cores per digit, one for zero and one for one, so that half the cores will always be in the one position. The sensing winding would then be made to subtract the outputs of the two cores so that the output will be positive for a one and negative for a zero. This is a very desirable feature.

Signed Kenneth H Olsen
Kenneth H. Olsen

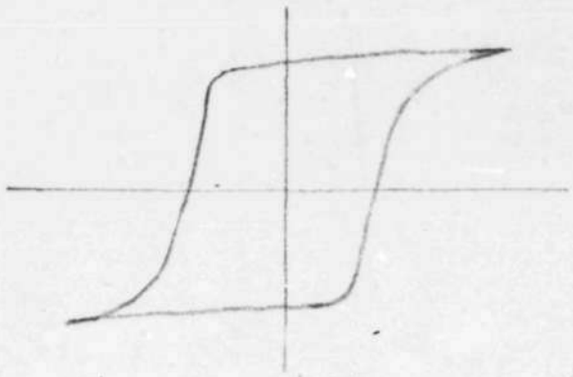
KHO:jrt

Attached drawings: SA-50603
SA-55233
SA-55228
SA-55229

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

SA-57233



Saturation Φ-I Loop (MF1113)

Fig II

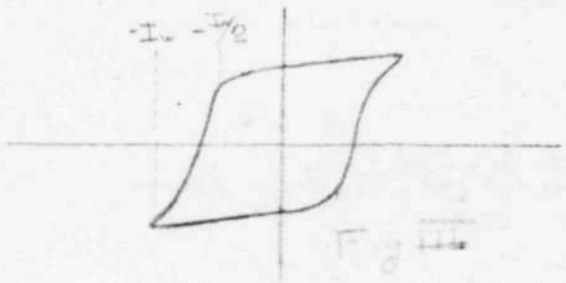


Fig III

Φ-I Loop Used in Coincident Current Memory

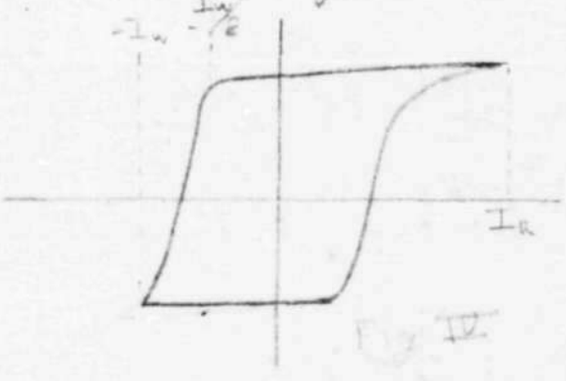
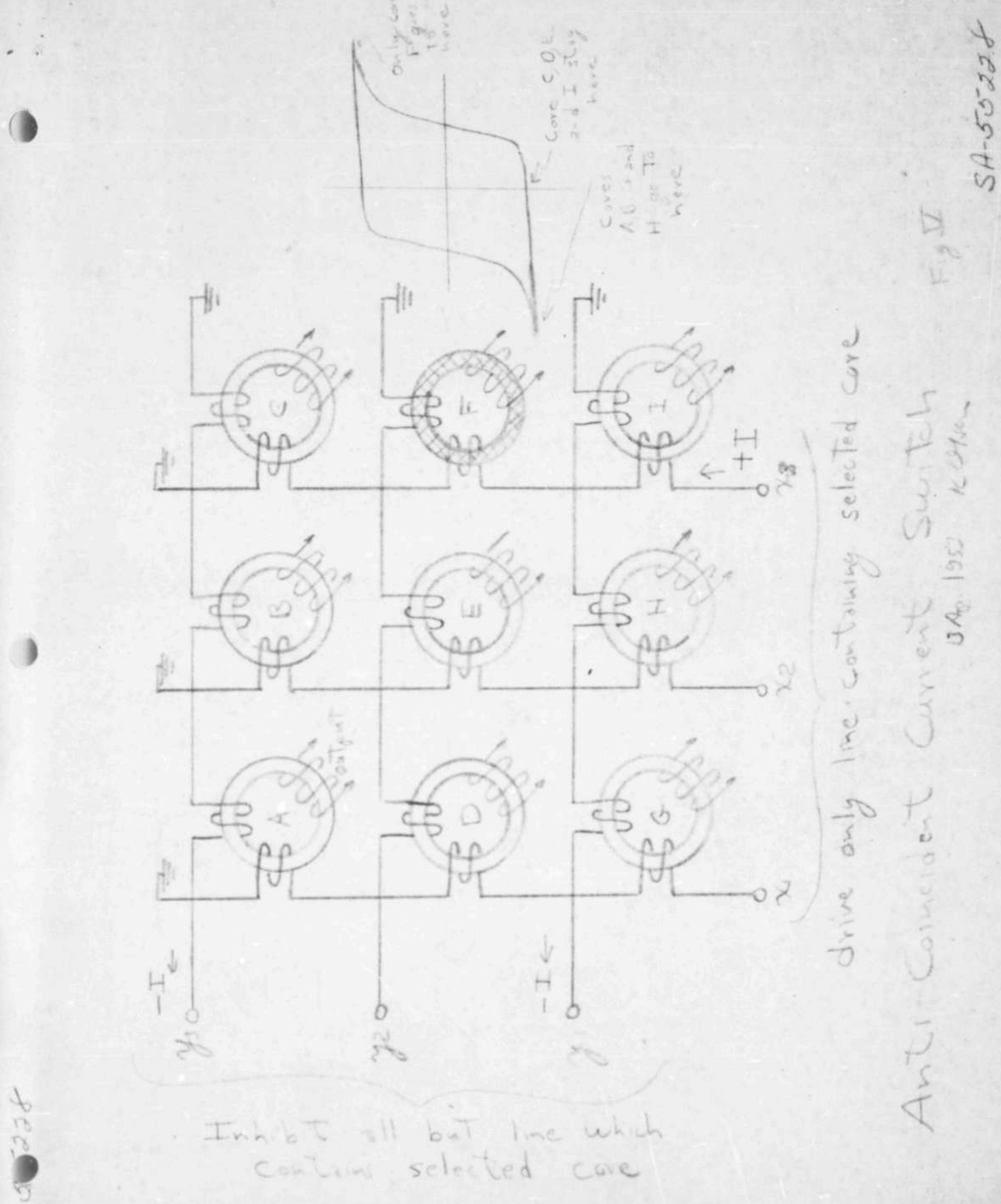


Fig IV

Possible Φ-I Loop in a Linear Selection Memory

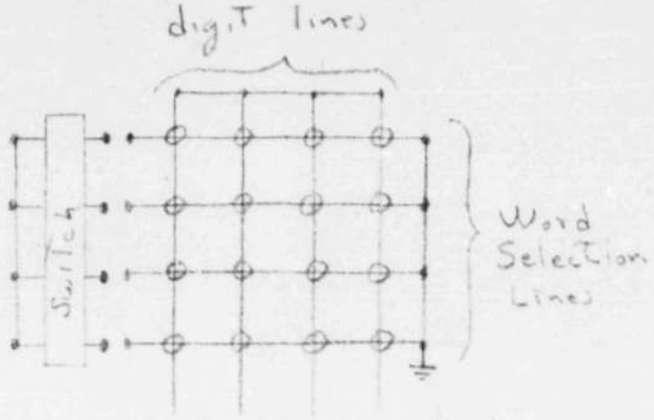
SA-57233

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

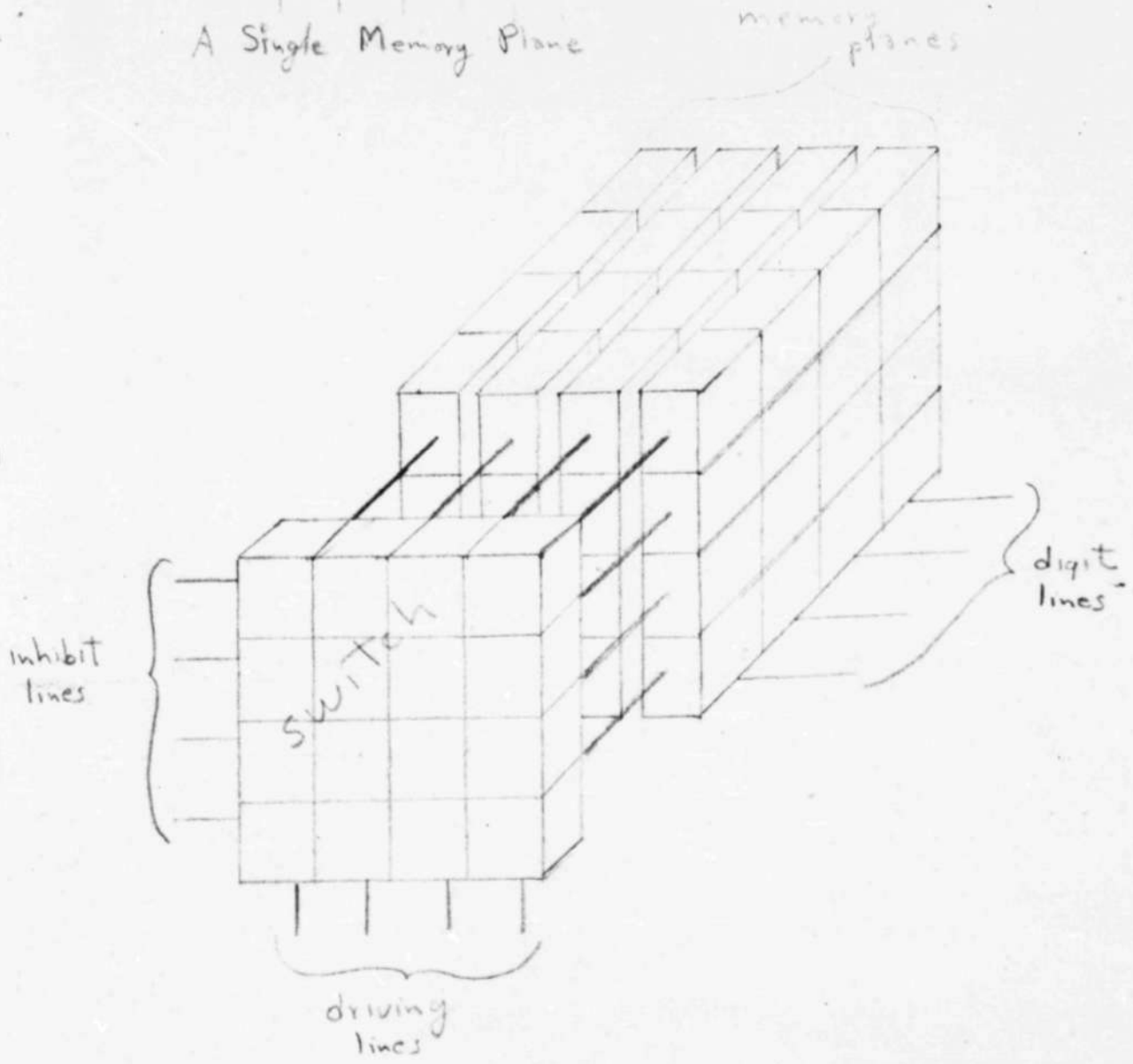


APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

SM-55279



A Single Memory Plane



Arrangement of Planes in Memory

Fig VI

SM-55279

13 Apr 1953