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Memorandum M-2162

Digital Computer Laboratory
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Subject: WWII MEMORY ADDRESS SELECTION SYSTEMS - P. B. No. 62

To: N. H. Taylor

From: J. L. Mitchell

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Abstract: This note contains a survey of the existing memory-address selection systems as well as a survey of some of the more promising new systems that have been proposed.

The function of the memory-address selection system is to take the memory address from the memory-address register and either read from or write into the selected memory register. In order to do this, two pieces of equipment are needed: a translator and a set of current drivers. The translator takes the output of the memory-address register flip-flops, converts from the base 2 to the base 64, and thus selects the proper driver. The selected X driver and the selected Y driver drive the X and Y selection "planes" with the currents necessary to read from and write into the memory.

Basically there are two types of translators and two methods of driving that will be considered. The two types of translators are the crystal-matrix and the magnetic-core matrix. The two methods of driving are driving a selection "plane" directly from the plate of a vacuum tube and driving a selection "plane" from the secondary of a magnetic device. The subsequent discussion will describe some of the combinations which have been proposed. Throughout this note we will talk about a 4096-register memory.

Following the description of the various systems, there are two charts: a chart, Figure 4, listing the equipment needed for each system and a chart, Figure 5, showing some of the advantages, disadvantages, and other peculiarities of each system.

Equipment counts, Figure 4, include all the equipment needed to operate the entire memory-address selection system. In the tube counts, the tubes will be separated into five types, as follows:

1. Memory drivers. These tubes drive the X and Y selection "planes" directly and must supply rectangular 500-ma current pulses about 1.5 μsecs long at a duty cycle of something less than 50%.

2. Pulse-transformer drivers. These tubes drive the memory through current step-up pulse transformers and probably will have to supply 100-ma pulses 1.5 μsecs long at something under a 50% duty factor.

3. Magnetic-core matrix drivers. These tubes drive the magnetic-core matrix and probably will have to supply the same sort of pulses as the memory drivers, or slightly greater.

4. Buffer amplifier tubes (including crystal matrix drivers).

5. Gate tubes.

A. <u>Crystal-Matrix Translator with Vacuum-Tube Drivers</u>

In order to select and drive one of the selection planes, we need a 64-position crystal matrix, 128 drivers and their associated buffer amplifiers, and read and write switches to gate the drivers on. Figure 1 shows a block diagram of the system. The outputs of the six flip-flops are run through buffer amplifiers into the crystal matrix. Each of the 64 outputs of the matrix goes to two buffer amplifiers which are normally-on tubes. The selected pair of buffers is cut off by the matrix, and as a result they tend to gate a read and a write driver on. However, all the read-driver cathodes are connected to ground through a common resistor, the voltage drop across this resistor being determined by the read switch. This voltage drop is adjusted so the driver tubes that have been gated will not turn on until the read switch is pulsed. When the switch is pulsed, the drop across the read resistor is decreased, causing the read driver to conduct and send $1/2\ I_m$ to the selection "plane." The write operation is performed in the same manner. Each driver used to drive a memory plane would contain one tube of the "memory driver" size. The buffer amplifiers used with these drivers would also consist of one tube. The read and write switches would each be made up of five memory-driver tubes in parallel, a buffer amplifier tube, and a gate tube.

This scheme could be varied in a number of ways, one way being to gate the buffers in place of the drivers. Crystal diode gates could be placed in the input lines to the buffers and used to control the read and write operation and thus eliminate the read and write switches. This would eliminate about 25 tubes and add 256 crystals to the system.

B. Crystal-Matrix Translator with Pulse-Transformer Drive

This system is similar to the system described under part "A"; the difference is that pulse transformers have been added to the system. The memory planes are driven by three-winding, current step-up, pulse transformers which might give a current gain of about five.

C. Magnetic-Matrix Translator and Driver

To select and drive the selection "planes" along each coordinate axis, a 64-position magnetic-matrix translator and driver and 14 vacuum-tube drivers and their associated buffer amplifiers are needed, as shown in Figure 2. The switch is set up by the 12 drivers controlled by the address flip-flops; then, during read time, the read driver is turned on and causes the selected core to switch and produce a current pulse which drives the selection "plane." The write operation is carried on in a similar manner; this operation both resets the switch and supplies the write pulse to the memory. All the driver tubes would be of the "magnetic-matrix driver" type. A one-tube buffer amplifier could be used between each flip-flop output and driver; however, the read and write buffer amplifiers would need about six tubes each for pulse shaping and current regulation. There are several variations which can be made on this basic scheme, but none of them makes an appreciable change in the tube count or operation.

A good deal of work is being done on the analysis of the switch, and the feeling is that there is a fair chance that a satisfactory switch can be built in the near future.

D. Magnetic-Matrix Translator with Vacuum-Tube or Pulse-Transformer Drive

Another possible system has been suggested which uses a magnetic-matrix in place of a crystal matrix. Each core in the switch has two output windings, one going to the grid of the write driver and the other to the grid of the read driver. The secondary windings on the switch cores have a large number of turns and give enough voltage out to drive the grids of the driver tubes directly, eliminating the need for buffer amplifiers. The equipment needed to drive the switch would probably consist of single-tube drivers and a single-tube buffer amplifier for each switch driver.

E. 4096-Position Magnetic-Core Translator and Driver

This system would use a 4096-position magnetic-core "switch," with each output of the switch driving one register of memory cores. Register selection within the memory would be on a one-coordinate basis (not using coincident currents). There are several ways a switch like this could be built; for instance, it could be built using the same principles that are used in present matrix switches; this seems, as yet, infeasible. Another way to build the switch is described in M-2110 by K. Olsen. The equipment needed for this switch when it is, in turn, driven by crystal matrices and vacuum tubes is shown in Figure 4.

F. Crystal-and-Transformer Matrix Translator and Drive

In order to select and drive one selection "plane", this system requires two 8-position crystal matrices, 24 drivers and their associated buffer amplifiers and gates, and an array, or matrix, of 64 pulse transformers connected as shown in Figure 3. Selection of a selection "plane" is accomplished by obtaining coincidence between the read and write drivers connected to crystal matrix number one and the condition drivers connected to crystal matrix number two. The condition drivers are on during both the read and write operation, and the read and write drivers are gated on for their respective operations. The diodes in the primaries of the transformers are necessary to prevent "back" circuits in the transformer matrix. The drivers are all one-tube units, as are the buffer amplifiers and gates. IBM is building up an experimental system of this type at High Street.

Signed J. L. Mitchell
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Approved WNP
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JLM/bs

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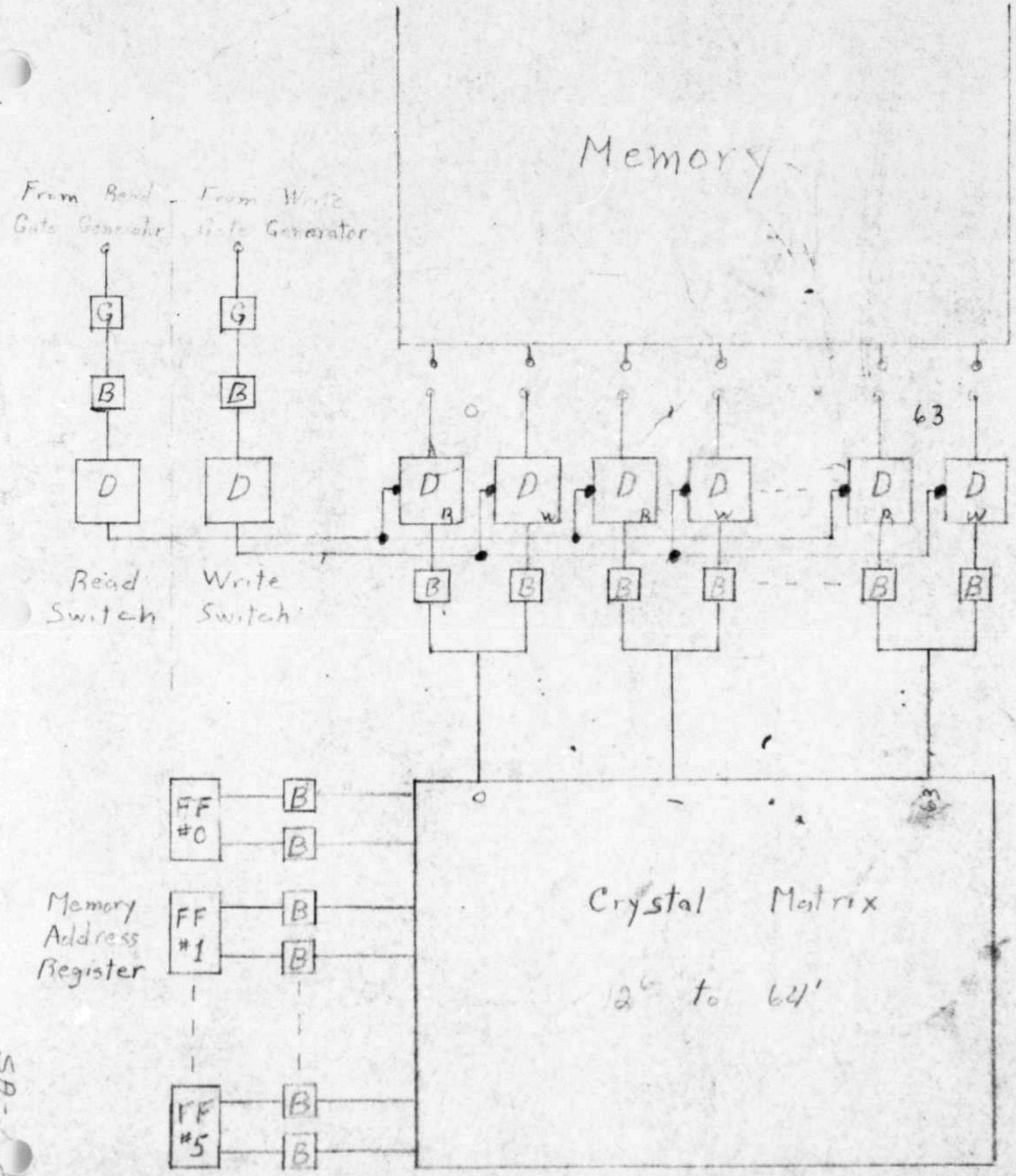
Drawings attached:

Figure 1, SA-54789-2
Figure 2, SA-54790-1
Figure 3, SA-54791-3
Figure 4, SA-54911
Figure 5, SB-54912

SA-54789-2



Crystal - Matrix Translator With Vacuum - Tube Drive

Figure #1

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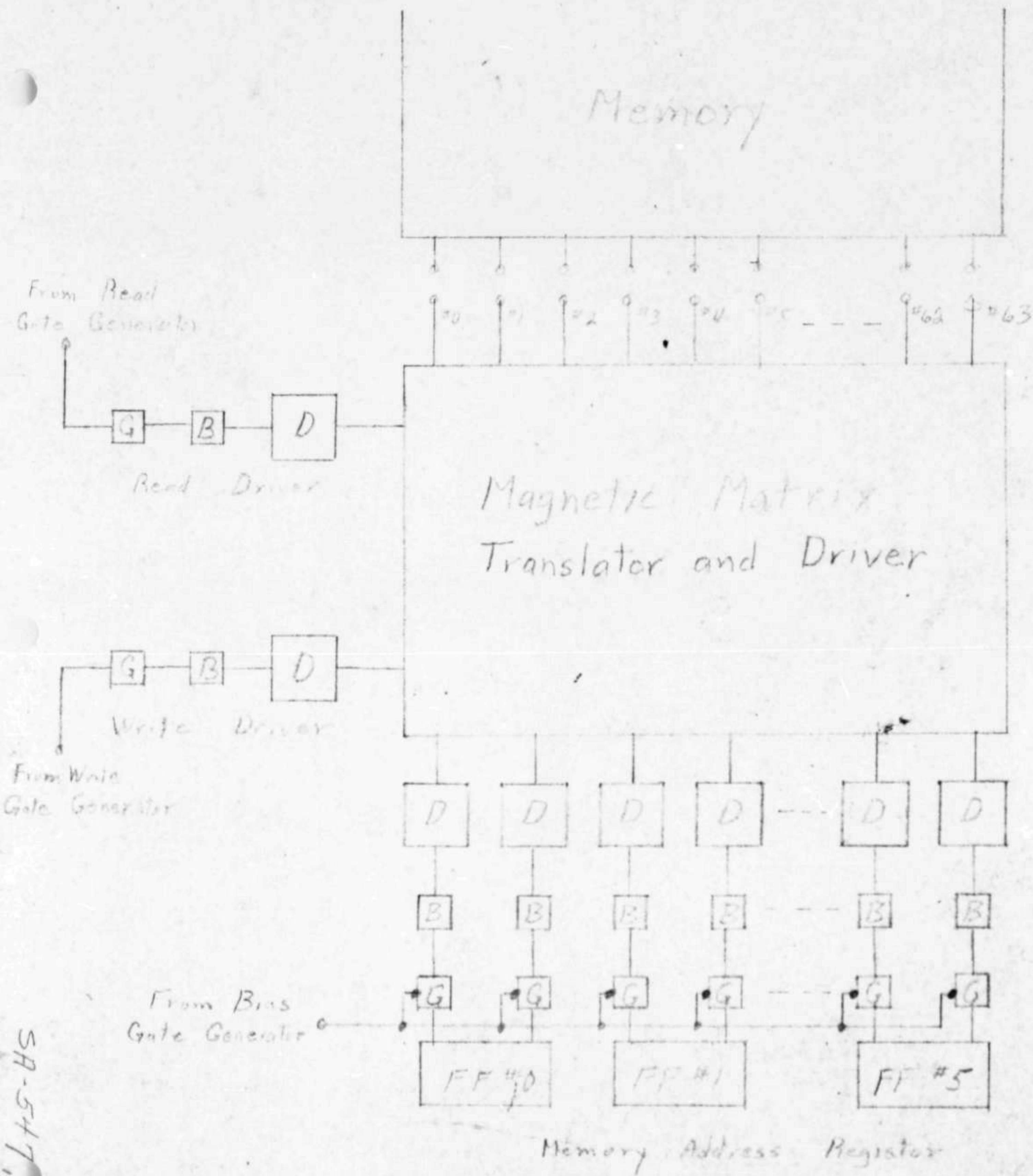
SA-54790-1



Magnetic - Matrix Translator and Driver

figure #2

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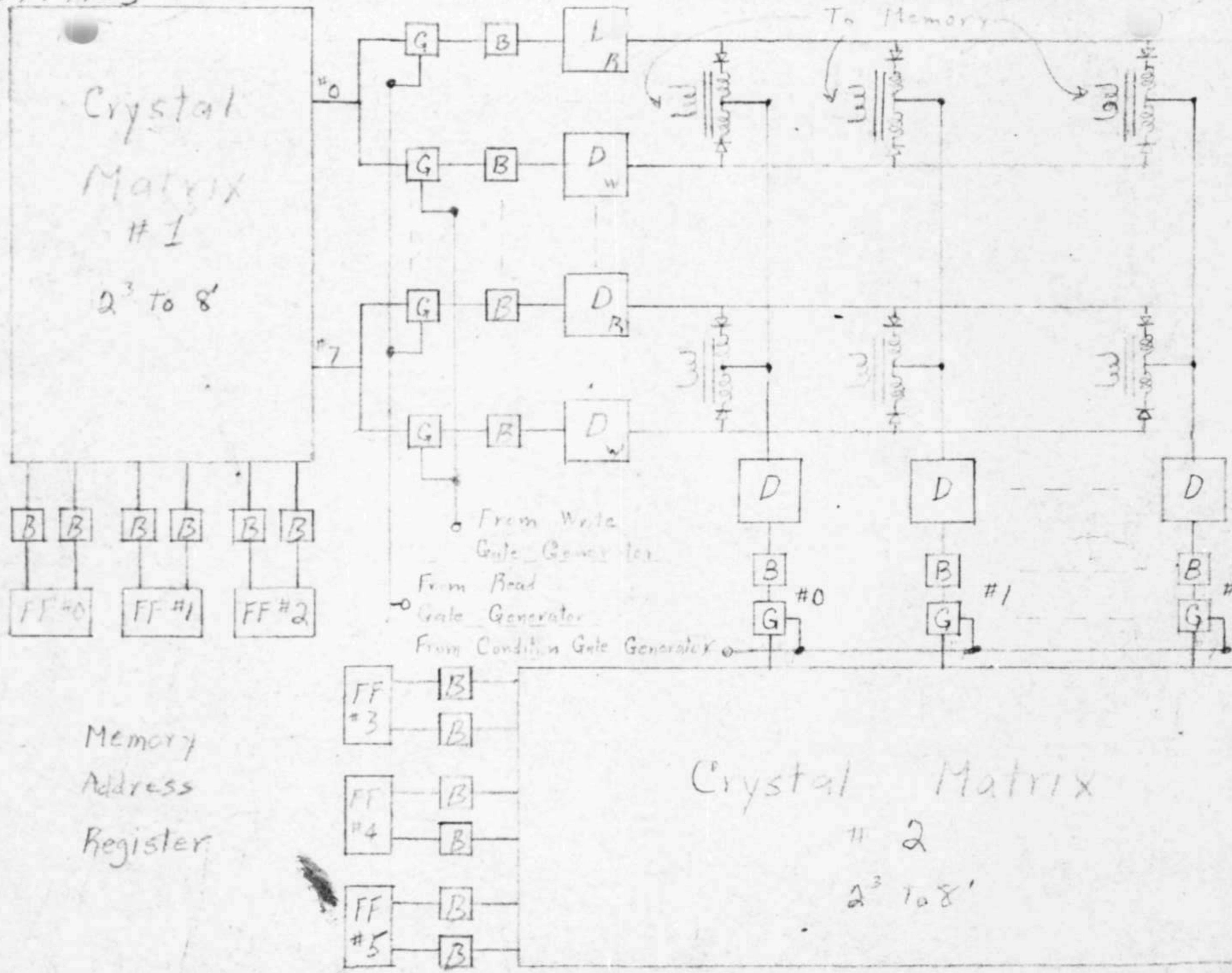
SA-54791-3



Crystal-and-Transformer Matrix Translator and Drive

SA-54791-3

SA-54911

Equipment Count for Memory Address Selection Systems

4096 registers

figure 4

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	A Crystal-Matrix Translator, Vacuum-Tube Drive	B Crystal-Matrix Translator, Pulse-Transformer Drive	C Magnetic-Matrix Translator and Driver	D Magnetic-Matrix Translator, Vacuum-Tube Drive	D′ Magnetic-Matrix Translator, Pulse-Transformer Drive	E 4096-Position Magnetic-Core Translator and Drive	F Crystal and Transformer Matrix Translator and Drive
Memory-Driver Tubes	276	-	-	256	-	-	-
Pulse-Transformer Driver Tubes	-	276	-	-	256		48
Magnetic-Matrix Driver Tubes	-	-	28	28	28	207	-
Buffer Amplifier Tubes	284	284	48	28	28	219	72
Gate Tubes	4	4	28	28	28	3	48
Total Tubes	564	564	104	340	340	429	168
Crystal Diodes	768	768	-	-	-	768	352
Pulse Transformers	-	128	-	-	128	-	128
Switch Cores	-	-	128	128	128	4096	-

SA-54911

SB-54912-1

	A	B	C	D	D'	E	F
	Crystal-Matrix Translator, Vacuum-Tube Drive	Crystal-Matrix Translator, Pulse-Transformer Drive	Magnetic-Matrix Translator, and Driver	Magetic-Matrix Translator, Vacuum-Tube Drive	Magnetic-Matrix Translator, Pulse-Transformer Drive	4096-Position Magnetic-Core Translator and Drive	Crystal-and-Transformer Matrix Translator and Drive
Experience with System	A rather large amount of experience has been acquired; more than any other system	Experience with components, but none with system	Some experience with 16 position switches driving a 16×16 memory	None	None	None	None
Output Current Shape and Line-to-Line Regulation	Good; common cathode resistor gives regulation	Could be obtained by feedback around transformers, precision transformers, or vernier adjustments on drivers	Input must be shaped to get desired output. Line-to-line regulation may be difficult	See A	See B	Requirement on current pulses are not as strict as in other systems	See B
PRF Sensitivity	None	Read pulse must immediately be followed by a write pulse	Some trouble may be encountered due to asymetrical operation on B-H loop	Less troube than C	See B	Same as C but probably less critical	See B
Number of Drive Wires in a Memory Selection Plane	2	1	1	2	1	Different winding mode.	1
Memory Array Impedence	Not critical	Should be low to keep back-voltage down	Not too critical	Not critical	See B	Not critical	Must be very low to keep back-voltage on diodes down
Memory Fabrication Ease	Standard	Standard	Standard	Standard	Standard	Memory easier to build	Standard
Signal-to-Noise Ratio in Memory Output	Standard	Standard	Standard	Standard	Standard	Better because no cores are disturbed during read time	Standard
Memory Core Specifications	Standard	Standard	Standard	Standard	Standard	Can be relaxed	Standard
Quality of Driver Tubes Available	A very reliable tube not yet found	Unknown	Unknown	Unknown	Unknown	Unknown	Unknown
Dynamic Load on Driver (effect of cores switching)	0-32 cores out of 2048 being driven can switch	See A	See A	See A	See A	0-32 cores out of 32 being driven can switch	See A
Miscellaneous Comments			Uses fewer components than any other system	Requirements on switch core are reduced.	See D		① Diodes in transformer primary are not desireable ② Electronics of this system is more complicated than any othe system

Comments on Memory Address Selection Systems

figure 5

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