

Memorandum M-2387

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Division 6 - Lincoln Laboratory
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Cambridge 39, Massachusetts

SUBJECT: CURRENT STATUS OF BASIC CIRCUIT WORK
To: Holders of Circuit Application Manuals
From: Arthur W. Heineck
Date: August 21, 1953

ABSTRACT: This note contains most of the important points discussed at a joint meeting of the IBM-MIT circuit design groups on August 19, 1953.

The main points made at the meeting were:

- a. High-Speed Flip-Flop: The only remaining circuit problem is to eliminate a 16 volt noise pulse which occurs when a set trigger is applied to a flip-flop already in the set condition.*
- b. Gate Tube Circuit:
 1. More data must be taken on the gate tube circuit pulse transformer before the number of turns, turns ratio, and winding geometry can be decided upon.
 2. The effect on output voltage of the forward resistance of diodes in the control and suppressor grid must be investigated.
- c. Pulse Amplifier: There seems to be a clear cut need for two different pulse amplifiers, the register driver and a general purpose pulse amplifier.
- d. Delay Unit: If the proposed 0.25, 0.5 and 1.0 microsecond delay units are to be used, the Standard Component Subcommittee must investigate the distributed constant coax-type delay lines and others and issue a C.A.M.

* H. Boyd has eliminated this noise pulse by the addition of one RC circuit and a change in value of the cathode bypass capacitor. With the new changes all of the output waveform specifications are met; however, margins have not yet been taken.

e. Cathode Follower:

1. Clamping diodes must be used at the output of cathode followers to protect logical diodes in case of a power failure.
2. Cathode follower bias resistors should be used when several levels of diodes and cathode followers occur in series.

Resume of the Joint MIT-IBM Circuit Meeting.

A. High-Speed Flip-Flop:

1. A noise pulse is developed at the output of the cut-off portion of the high-speed flip-flop if an attempt is made to set or clear a flip-flop that is already in the set or clear condition. This occurs when a shift is performed. This pulse is as much as 16 volts when a 30 - 40 volt trigger is applied. It was generally agreed that this noise pulse must be eliminated.*
2. The marginal checking voltage will be applied to only one grid through a resistance divider. This will allow a swing of 75 volts around -150 volts. Another scheme which saved resistors and required a 7 volt swing around -150 volts was discarded because of noise which might appear on the marginal checking line. This noise might be an appreciable part of 7 volts but would be insignificant compared to 75 volts.
3. It was generally agreed that the flip-flop can control the suppressor of a gate tube directly. This means that under light loads no additional cathode followers are needed. Previously it was thought that an additional cathode follower would always be needed, to handle the suppressor current, whenever a gate tube is controlled.
4. It was decided that when data is taken to determine what loads the flip-flop can drive, critical components or perhaps just one critical component should be in the end of life condition. These components have not been selected yet.

* Refer to footnote on page 1.

B. Gate Tube Circuit:

1. A 10 ohm parasitic suppressor will be used in both the control and suppressor grids.
2. The gate tube circuit pulse transformer is still a problem. The following choices still have to be made:
 - a. Number of turns: 32:8, 28:7, or 30:6
 - b. Turns ratio: 4:1 or 5:1
 - c. Winding geometry: solenoid, tight or loosely coupled.

The decision was made to have Sprague wind about 25 pulse transformers from Ferramic cores supplied by MIT. These samples would cover all possibilities mentioned above. MIT and IBM will receive half the transformers and take data. The transformers will be interchanged and the data repeated. This should lead to the choice of the optimum transformer.

The transformers will be tested under the following load conditions:

- a. 1 gate tube
 - b. 5 gate tubes
 - c. 3 gate tubes and 2 flip-flops on complement input.
 - d. For each of the above loads use screen voltages of 70 and 90 volts.
3. Data must be taken to determine the effect on output voltage of the forward resistance of level diodes in the suppressor grid and pulsed diodes in the control grid.
 4. It was agreed that a common pulse transformer might be used whenever the outputs of two gate tubes drive a common load. This occurs in the parity count. No work is being done on this circuit.

C. Pulse Amplifier:

1. A 10 ohm parasitic suppressor will be used in both the control and suppressor grids.
2. Two different pulse amplifiers might be useful:
 - a. A register driver.
 - b. A circuit to drive loads which are a little too heavy for the gate tube circuit.
3. Register driver: The register driver will probably have a step-up transformer in the input and a step-down transformer in the output. Some typical applications would be to set, clear or complement 16 flip-flops or to sense 16 gate tubes.
4. General purpose pulse amplifier: This pulse amplifier will just have a step-down transformer in the output. It will not require a step-up transformer input.
5. If at all feasible, the transformer selected for the gate tube circuit should also be used in the pulse amplifier circuits.

D. Delay Unit:

1. It was not definitely decided whether a distributed line, lumped line, or multivibrator would be used for delay purposes.
2. If the proposed 0.25, 0.5 and 1.0 microsecond delay units are to be used the Standard Components Subcommittee must investigate the distributed constant coax-type delay line and issue a C.A.M.
3. IBM will continue their investigation of multivibrators.

E. Cathode Follower:

1. Clamping diodes must be used at the output of cathode followers to protect logical diodes in case of a power failure.
2. Cathode follower bias resistors should be used when several levels of diodes and cathode followers occur in series. These bias resistors help to keep the "bias buildup" at a minimum.

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3. IBM will continue to investigate the plate-cathode transformer-coupled cathode follower. Initial results seem to indicate that 30-50% more capacity can be driven, within the established rise and fall time specifications, when the transformer coupling is used.

F. Level Inverter and Level Setter:

Circuits have been designed both at MIT and IBM to do the job of level setting and level inverting. The IBM circuits differ only in minor details from the MIT circuits. The design engineers will get together in the near future and try to agree on one circuit for each job.

Signed: Arthur W. Heineck
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Approved: John F. Jacobs
John F. Jacobs

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