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Memorandum M-1402

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Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II MEETING OF FEBRUARY 8, 1952

To: Whirlwind II Planning Group

From: Norman H. Taylor

Date: February 18, 1952

Members Present: R. Everett, H. Fahnestock, H. Grosch, W. Hosier, J. Jacobs, R. Jeffrey, W. Linvill, W. Papian.

To open the meeting, Norman Taylor presented a possible starting point for work aimed at using an Iron Core Memory Unit with a transistor as a combination memory and gating device. The idea stemmed from the circulating delay line type of memory common to the SEAC system and later used by Mr. Felker in his BTL Adder Circuits. By replacing the Delay Line with an Iron Core, it seems possible that the read out of the Iron Core could be simultaneous with a sensing pulse, and with a suitable delay mechanism it would be possible to re-write the contents of an Iron Core immediately after sensing it. Such a system would allow the use of "and" gates and inhibitor gates in the same logical arrangement as the circulating technique uses. It does seem, however, that considerable flexibility in timing would result if this approach proved fruitful. Since the meeting, we have started one engineer investigating the possibility of using this general approach. He will start by using Vacuum tubes to drive the available Iron Cores and then work towards using transistors to drive Iron Cores which may become available in the future.

Papian discussed some of the work of D. R. Brown in plotting up the response time and signal-to-noise ratios as they are measured on the single pulse core tester. We hope to hear more about this from Brown at the next meeting.

Taylor presented the plan to build a prototype system within the next twelve months to test out the new ideas in circuitry, using both transistors and iron cores.

A rather interesting discussion followed which attempted to give a first approximation of a prototype system. It was suggested that a Single Register Computer be started with a 16 bit word length, the memory to consist of 16-256 bit storage elements made from the Magnetic Ribbon with an over-all access of approximately 20 μsec.

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There was considerable discussion concerning the advisability of using the Magnetic Cores as elements in the Control Matrix. This is certainly a new and novel idea stemming from a suggestion by R. Mayer a few weeks ago. We were unable to decide as to whether we should consider this for a Prototype Computer. Further discussion will be necessary in order to decide the possible advantages of such a system.

Another possible method of building a Control Matrix which places one of the Magnetic Switch Cores at the inter-section of the matrix in place of the Crystal Diode now used was discussed by Olsen. It was pointed out that this core provides gating action as well as making the connection at the junction of the matrix and considerably more flexibility is inherent in such a scheme.

The following list of orders seem to be basic and necessary to any such computer if it is to be useful:

1.	ca	9.	ri
2.	ad	10.	rd
3.	sl	11.	rc
4.	sr	12.	qd
5.	ts	13.	qh
6.	cp	14.	spare
7.	sp	15.	
8.	su	16.	

It is quite evident in reviewing the above comments that such a prototype system is quite an ambitious one and perhaps is beyond the scope necessary to provide a testing ground for new componentry and new ideas. However, it does not seem impossible that such a Computer could be built on a prototype basis if we are willing to freeze the specifications at an early date and allow a small integrated group of engineers to go ahead and build such a system. There is little doubt that some such prototype program would help us realize a Whirlwind II system with a minimum of delay but further discussion will be necessary to decide just how ambitious this prototype should be.

N H Taylor
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NHT:rdf