Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WWII BLOCK DIAGRAMS MEETINGS OF MAY 6 & 8, 1952

To: WWII Planning Group

From: W. A. Hosier

Date: May 13, 1952

Abstract: This note summarizes the discussion at the above meetings for the benefit of those who may wish to trace the course of thought on the subject.

Present:

May 6:	May 8:	
R. C. Jeffrey	G. R. Briggs	I. S. Reed
W. A. Hosier	D. R. Brown	N. H. Taylor
R. P. Mayer	R. C. Jeffrey	
I. S. Reed	W. A. Hosier	
N. H. Taylor	R. P. Mayer	

R. Mayer began the first meeting by displaying a simplified block diagram of WWI, which he felt might apply in outline to WWII as well. He followed this with a discussion of the initial read-in program, which in WWI is accomplished by the registers of test storage; some sort of semi-permanent or manually-set part of the WWII storage would presumably need to be devoted to this. Mayer proposed one method which would take only 10 such registers to read in from 5-5-6 tape; the sequence of orders runs as follows:

```
1.  qr  5      4.  qr  5      6.  qr  5      9.  ao  8
2.  ca  FF3    5.  ad  FF3    7.  ad  FF3    10. sp  1
3.  cp  40                    8.  ts  40
```

If the proper sort of orders were built into WWII, said he, this program could be done with only three registers of the above type. The orders required would have to be (a) to read in the full-length word from tape; (b) to transfer it to the proper memory register; (c) to determine whether all words have been read in from the tape.

Since for all practical purposes it would seem that three registers and a program counter are the minimum one can expect in a computer which is to multiply (additional registers will doubtless be determined by the nature of the terminal equipment), Mayer had prepared some detailed traffic schedules of orders as executed by such a machine, indicating the command pulses which

would have to be generated in its magnetic stepping registers. He pointed out that orders can be grouped into four or five categories each of which has its own "fundamental sequence" of commands: ca, ad, sa, su, cm resemble each other; likewise ts, td, ta; sl, sr, sf; mr, mh, dv; etc. It is likely that one "trunk" stepping register can serve each such class of related orders. Nearly all program timing can probably be done in a single stepping register; however, certain slight variations of program timing among orders will necessitate careful scrutiny of all orders before the number of "trunks" and "branches" in the control can be fixed. The group agreed to pursue this grouping of orders in more detail.

As an aid in simplifying the symbolic expression of transfer of information within the machine, it was proposed that single letters be used to designate components originating and receiving information: C for Control Switch, P for Program Counter, A for A-Register (which doubles as Program Register in Mayer's machine), W for Storage Switch, S for Storage (Memory), U for Accumulator, and B for B-Register. Subsequent additions were D for a delay element and G for another ("general") counter which it seemed advisable to include. The ca order in Mayer's machine can then be summarized as follows: (O → A means "clear A"; SAM means "special add memory".)

(1) O → A, P → W
(2) S → D
(3) D → A
(4) A → S, O → W, A → C
(5) A → W
(6) S → D
(7) O → A
(8) D → A, SAM → U
(9) A → S, O → W, A → U

In this proposed machine, Mayer had entertained the idea of using a few gate generators or pulse stretchers; Taylor vetoed this, saying he would rather see flip-flops used to obtain delays of this sort, because of their greater reliability. He (Taylor) also pointed out that we are by no means committed to driving the stepping registers by 1 megacycle clock pulses; that 2 megacycle pulses could be split into two 1-megacycle "phases", or 3-megacycle into three phases. (Here Jeffrey remarked that we were on the way back to the 8-phase time pulse distributor of WWI.)

Mr. Reed asked why flip-flops couldn't be read into and out of on the same pulse, since this seems to be a widespread practice in other machines. Taylor's reply was that it is a question of speed; if the time constant of the flip-flop is so short as to approximate the driving and gating pulses, its output will be unpredictable.

A discussion of multiplication and division evolved the notion that it might be profitable to be able to do these operations in some cases with reduced accuracy - say, half the number of significant digits.

Questions about the usefulness of transistors as logical circuit elements brought out the fact that nearly all present transistors are of the type known as P-N-P: when conducting in a forward direction, this transistor has emitter positive, base negative, and collector positive, thus makes a good "and" gate. A dual of this, the N-P-N transistor, has been made experimentally in small numbers, and would give promise of being a satisfactory "or" gate (mixer).

The second (Thursday, May 8) meeting was opened with a presentation of the sl order in Mayer's previously-mentioned machine: P → W, S → D, 0 → A, D → C and D → A, A → S, A* → G, followed by successive shifts until the counter G overflows. (A* denotes partial contents of A--the n part of the sl n order, indicating number of shifts.) Mayer originally had a B-register which held the contents of the program counter P while P was used as a step-counter; however, it seemed more useful to omit this and add the counter G.

The discussion of this order brought up the issue of whether a bus system is desirable for a computer of this design. A summary of information-transfer operations was made, including the B-register, but not the counter G:

P → W, B	U → B, S	B* → S
A → S, W, P, U^+, U^-	U* → S	S → D
A* → S	B → S, U	D → C, A

With the exception of the last two transfers, which are best done on "private lines" anyhow, all other registers read into two or more places, and this would seem to argue for use of a bus. To be sure, the necessity for time-sharing the bus may slow down a few orders: storage operations may tend to conflict with arithmetic manipulation (more likely if the machine has two memories), and internal operations may tend to conflict with input and output. This last matter, of the demands to be made on the computer by input-output equipment, was thought to warrant our getting more familiar with current thought on the subject, through the men who are working on it. N. Taylor commented that direct wiring is probably of most help when a machine has 3 or 4 registers at most; beyond that it begins to get intricate and cumbersome. Fewer registers, however, would also mean a shorter bus, more easily driven; so the bus dies hard, if indeed at all.

The general question of whether to have a bus and if so, how many, Taylor thought to be one of the basic decisions affecting WWII; further, to be in large measure an engineering decision, depending, for example, on whether it is easy to drive a bus with transistors.

The B-register came under scrutiny to see whether it was really necessary. Half-length multiplication and division would seem to have no need for it; Mayer had used it as a temporary repository for the old address on sp orders, but this function, Taylor pointed out, does not require a register as complex as the usual B-register. Hence the B-register was deemed superfluous, unless other need for it can be shown.

Two basic arrangements of cores in a stepping register for shifting were suggested by Mayer: the first using a string of cores, one for each place shifted; the other using only two cores, taking shift pulses from them alternately. In the 2-core arrangement as well as in one technique of using the "string", the shift cycle is stopped by an end carry from the counter G; in the other string technique a decoder would determine where in the string to start the cycle, which would then run to the end of the string. All in all, the 2-core scheme seemed to have a decided advantage in size and simplicity.

N. Taylor remarked that he would like to see vacuum-tube flip-flops entirely removed from WWII. Two types of transistor flip-flop, the "static" or 2-transistor, and the "dynamic" or 1-transistor, are being worked on now. It is thought that the necessity for synchronized "restorer" pulses in the "dynamic" circuit may impair its efficient use with terminal equipment.

Having surveyed the logical design problem from some of its most general aspects, we probably would do well, thought Taylor, to approach it now from the other end - the input-output requirements of the air defense problem. In this connection he suggested talking with Ed Rich, reviewing the evolution of present drum proposals; also possibly a review of the "VOLAIRE" system, which collects radar data on CR tubes and transfers it to magnetic drums. I. S. Reed mentioned that we might also benefit from an exchange of ideas with Hugo Lodermann of Project Lincoln, who is conducting work on terminal equipment for CADAC.

SIGNED W. A. Hosier
W. A. Hosier

APPROVED N. H. Taylor
N. H. Taylor

WAH/cp