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Memorandum M-1428

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Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

CLASSIFICATION CHANGED TO:
Auth: *DD 254*
By: *R. R. Everett*
Date: *2-1-60*

SUBJECT: WHIRLWIND II MEETING OF MARCH 14, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and R. P. Mayer

Date: March 18, 1952

Members

Present:	C. Adams	J. Jacobs	R. Olsen	R. Sims
	D. Brown	R. Jeffrey	K. Olsen	N. Taylor
	R. Everett	W. Linvill	R. Pacl	R. Wieser
	W. Hosier	R. Mayer	W. Papian	
	J. Hughes	R. Nelson	C. Schultz	

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N. Taylor began the meeting by pointing out that there are a number of questions which remain to be settled before attempting to build a prototype Computer. The tentative design so far is as follows: It should be a 16-bit parallel computer with a 256 word memory and 8 or 16 control orders. There would be two operating registers external to memory and there would presumably be some terminal equipment which has not been discussed yet. Questions on the above are as follows: Is a 16-bit word length too ambitious? Should the memory use Mo-Permalloy or ferrite and should we use vacuum tube drivers or a magnetic switch? Should ease of programming be a factor in deciding how many orders should be built-in? Is speed of operation a factor in determining how many operating registers we should have? As far as terminal equipment is concerned, what do we want the prototype to do and why are we building it?

In answering these questions, the purpose of the prototype was discussed first. The primary purpose is to test techniques and components which are to be used for the building bloc's in WWII. The secondary purpose is to try out new logical ideas (such as a single register computer) which might be used in WWII. And a third purpose is to provide incentive. The function of WWI 1/2 (or WWI A), therefore, could parallel the function of the Five Digit Multiplier in that it should provide us with the answers necessary for using the proper equipment and techniques for WWII. After the Five Digit Multiplier served a similar purpose, it was used for extended life tests. WWIA could also be used for life tests after it has served its primary purpose, but on the other hand, it is possible that it could be turned over to the

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WWI Group for special uses (for instance, as a Terminal Equipment Computer). R. Wieser pointed out that there might be some trouble if we tried to design WWIA to satisfy both of these purposes. This difficulty can probably be avoided if we do not consider at all the secondary purpose but simply turn WWIA over to the WWI Group at the proper time and let them make modifications as they wish.

However, it would be a shame to build WWIA with almost, but not quite, enough digits to work efficiently with WWI. Since it requires about 10 digits to represent an instruction with its address, WWIA might as well be built with a 16-digit word length.

A memory capacity of 256 words looks optimum, but R. R. Everett proposes that 1024 Registers be used because it might show up various electronic problems more rapidly. A definite decision about memory was reached: Ferrites should be used and a magnetic storage switch should be used in WWIA because these elements are proposed for WWII, and there is no point in not trying them out.

It is probably not necessary to consider terminal equipment until the Cape Cod Project has progressed somewhat further.

The big question seems to concern control and whether 8 or 16 orders should be used. A further suggestion is that we might be able to get along with 4 orders. Some proposals are as follows:

If 4 orders are used,

ts
su
cp
io

If 8 orders are used,

tc cr
td cp
ad mr
su io

If 16 orders are used,

ts tc
td dc
ad su
cr sr
sp cp
mr lm
qr qr*
qd qh

* Pronounce "star"; refers to a programmed modification of a standard order.

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The su is designed so that even with a 9's complement system, "zero" will in general be positive. Thus a tsx followed by an sux will clear the Arithmetic Element.

The io order exchanges external information with internal information, and its address could be used to specify the input and output devices (assuming a fixed storage address).

The tc order transfers to storage and then clears the Arithmetic Element (AE), which seems to be more efficient than ca, cs, etc.

The cr order cycles the Arithmetic Element right n times.

The dc transfers digits and clears AE.

The lm is a logical multiply, but is proposed only if convenient and if mh is not desired.

The qr and qr* operate 2 separate readers.

The qd and qh operate both the scope and the typewriter by a method of inhibitions sequenced by proper programming.

The 16 orders listed above are not supposed to be the most efficient group of 16, but they were arrived at by taking the group of 8 orders and providing a very small modification of each of these 8 orders by a technique similar to the sl* technique used in WWI. With this arrangement, the programmer would have available 16 orders, but the control switch would have only 8 positions. There is some question as to whether it would be more efficient to build a control switch with 16 positions, but if it is decided to build it with only 8, then the "star" technique could be used later if it is desired to increase the number of orders available. R. R. Everett suggested that 8 sounds like a minimum number of orders and suggests that a 16-position switch should be built in order to provide flexibility, especially if it is not electronically inconvenient.

It is assumed that the 9's complement system would be used, but no definite decision has yet been reached. C. W. Adams pointed out that instead of having a cp and an sp, it might be better to have a cp+ and a cp- or possibly a cp- and a cp "zero". It would be possible to do away with the td order if a B-box were used, but this is probably a luxury and will not be used in WWIA. It was pointed out that WWIA should not be used for testing complicated orders, since it should be kept electronically simple.

The problem boils down to a question of being ambitious enough to check the components and logic for WWI and yet not make WWIA so complicated that it can not be built within a year. We should not worry about packaging

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and compactness except where it is electronically desirable, such as in the memory. We should not hesitate to use a vacuum tube to substitute for an element which we feel can be built after a little more development. The first step in building memory will be to get a complete single digit operating reasonably well before continuing with the remaining digits. The goal will be to have WWIA, with a 1024 16-bit word memory, operating in less than a year or else find out why we can not do so.

The remainder of the meeting was concerned with electronic considerations for WWIA. Taylor pointed out that he is least confident of making an efficient central control system. There should definitely be no separate Arithmetic Element control; instead, central control should be used for controlling such processes. One proposal for control is to replace the Control Matrix TPD by a set of "domino" magnetic cores arranged so that each one triggers the next one. Once an order is started, all the steps for the order are carried out automatically. Experience with WWI has shown that it is not necessary to provide the ability for stopping the Computer in the middle of an order. Some time has been spent thinking about Arithmetic element, but now it is time for intensely considering Central Control.

Work is now progressing on a Magnetic Adder and on magnetic gates controlled by transistors. R. Jeffrey asked if it would be possible to consider using coincident pulses which cancel each other out. R. Everett suggested that it might be possible to use ORDVAC techniques with transistors. This makes use of D-C levels exclusively, and so is basically faster than using pulse techniques. It should be remembered that transistors burn out if they carry too much current for too long a time. Taylor described Wieser's idea for a non-destructive read-out from a core using carrier techniques. This raised the question of whether a non-destructive read-out is basically impossible, and it was pointed out that if the same part of an element is used for both remembering and reading-out, then the process of reading-out will probably destroy the memory. If the memory part is sufficiently separate from the read-out part, then this is not necessarily so.

D. Brown pointed out that we should not try to force the new components such as cores and transistors into the old block diagrams but should instead thoroughly investigate the capabilities of the new components and draw the block diagrams around these new capabilities. For instance, a core is not exclusively a flip-flop or a gate in the WWI sense.

Papian suggested that a committee should be formed for finding the basic uses and abilities of cores. The following people were suggested for this committee:

D. Brown	W. Linvill
D. Buck	H. Rising
R. Jeffrey	R. Sims

Rollin P. Mayer

(Rollin P. Mayer)

Norman H. Taylor

(Norman H. Taylor)

RPM/NHT:bs

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