Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

Subject: WWII MEETING OF SEPTEMBER 12, 1952

To: WWII Planning Group

From: N. H. Taylor, W. A. Hosier and K. H. Olsen

Date: November 18, 1952

Abstract: This meeting was devoted to a brief survey of present plans for logical design and physical layout of the Memory Test Computer, simply to introduce it to those members of the group not working directly on it.

Present:

H. Anderson	W. Hosier	W. Papian
R. Best	R. Hughes	R. Pfaff
R. Callahan	J. Jacobs	H. Rising
J. Crane	W. Klein	D. Shansky
D. Eckl	R. Mayer	N. Taylor
S. Fine	D. McCann	S. Thompson
E. Gates	J. Mitchell	B. Widrowitz
A. Guditz	W. Ogden	J. Woolf
A. Heineck	K. Olsen	R. von Buelow

Though the logical arrangement of MTC has been covered in the WWII meeting of July 18th (see M-1562), N. Taylor felt that a brief review of this - and the presentation of some further information regarding it - would be of benefit to those present.

K. Olsen first discussed the mounting and packaging to be used in MTC.

W. Hosier then drew a block diagram showing how the principal parts of MTC are organized and interconnected and followed this by a step-by-step analysis of program timing and the "read out" orders (add, clear-and-add, subtract, clear-and-subtract). Some aspects of display orders were also taken up, and the parity check was discussed in detail. In tracing the control sequence of orders, reference was made to H. E. Anderson's "guided-tour" drawings, Nos. SB - 52370-1 and SB - 52371-1.

N. Taylor mentioned that those people who are finding it difficult to follow the discussions on MTC should let him know, and he will either arrange special tutoring or plan for some sessions with W. Hosier so that they may become familiar with the terminology and thinking needed to understand discussions of computer logic.

W. A. Hosier

K. H. Olsen

N. H. Taylor

WAH:KHO:NHT/bs