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Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II MEETING OF JULY 25, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and R. C. Jeffrey

Date: July 29, 1952

Abstract: Work on magnetic circuits for logical applications was
reviewed by H. Rising, R. Sims and G. Briggs.

Members
Present:

H. Anderson	R. Gerhardt	C. Morrison
I. Aronson	A. Guditz	W. Ogden
P. Baltzer	A. Heineck	K. Olsen
G. Briggs	W. Hosier	R. Pacl
D. Brown	J. Jacobs	L. Piecha
R. Callahan	R. Jeffrey	J. Raffel
J. Crane	R. Jenney	H. Rising
R. DiNolfo	N. Jones	C. Schultz
D. Eckl	A. Katz	R. Sims
R. Everett	C. Kirk	H. Smead
R. Farmer	W. Klein	N. Taylor
S. Fine	W. Linvill	S. Thompson
J. Forrester	R. Mayer	R. von Buelow
E. Gates	J. McCusker	B. Widrowitz
	J. Mitchell	

Rising: Flip-Flop.

A magnetic core operating on the steep portion of the
idealized B-H or φ-I loop looks like a resistance. A core operat-
ing on the flat portion looks like an inductance. These approxima-
tions are used in the analysis of magnetic circuits. For example,
the characteristics of a core which is switching are approximated by
an idealized transformer with a resistance shunting the primary.

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From the point of view of coupling:

Flat portion: Little coupling (much fringing).

Steep portion: Much coupling (low reluctance flux path).

The inductance of a winding is due to the number of turns, to the characteristics of the core, and to the air gap between the winding and the core.

Notation:

Current entering a dot sets core up. Current leaving a dot sets core down. ∴. When current flows into a dot on a primary, current flows out of dots on all secondaries (or the dot ends of all secondaries are positive).

A Magnetic Flip-Flop.

This flip-flop is analogous to the vacuum-tube flip-flop, which complements by moving to a neutral configuration, remembering which state it came from by the charge on the coupling capacitor between tubes.

"0" OUTPUT   1   3   "1" OUTPUT

SET   2   4   CLEAR

5

COMPLEMENT →

6

1	↓	↑
0	↑	↓
INTERMEDIATE STATE	↓	↓
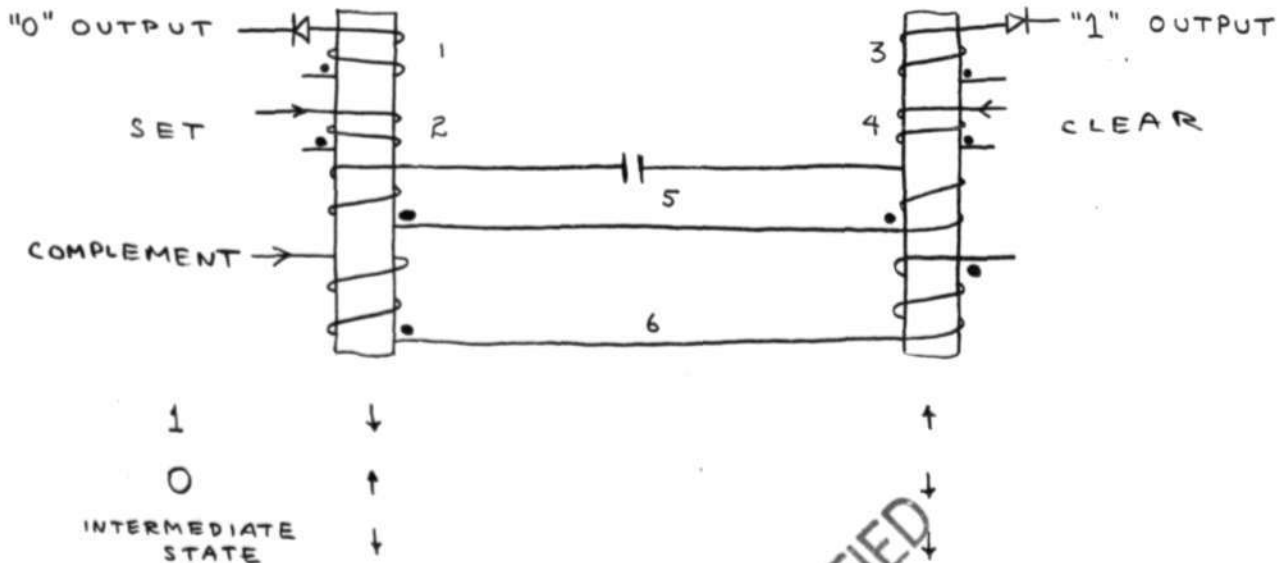
Rectifiers decouple the outputs while the capacitor is flipping the cores.

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Set Flip-Flop: I as shown in set winding sets left
core down. This induces a current in the left winding of 5
which charges the capacitor +⊣⊢ . When the capacitor dis-
charges, I flows into the dot at the right, setting the right
core up.

Clear Flip-Flop: Interchange right and left above.

Complement: Suppose the flip-flop is cleared: ↑↓ .
A pulse as shown in the complement winding sets cores ↓↓ and
charges the capacitor +⊣⊢ . When the capacitor discharges,
the left core is driven farther down, and the right core is set
up. Now the flip-flop is ↓↑ , the set configuration. Note
that, as in the vacuum-tube flip-flop, the complement winding at-
tempts to set and clear the flip-flop simultaneously.

The circuit is not bistable: if one of the cores is
not fully set, there is no tendency to go the rest of the way.
All power is supplied by the signal pulses. This flip-flop has
been built using Mo-Permalloy metallic cores and runs at a low
repetition rate.

Turnover speed: 2 microseconds.

It has been complemented at 5 kilocycles for 5 minutes
without deterioration of information.

Next step: Use ferramic cores to increase speed (this
will require 1-ampere pulses through 10 turns for set, clear and
complement). The present system uses 50 wraps of 1/8-inch tape
1/4 mil thick on a 1/4-inch ceramic bobbin.

Sims: Stepping register.

A magnetic stepping register was first developed at
Harvard ("Static Magnetic Delay Line") for storing digits in a
serial machine. A pattern of 1's and 0's in the various compart-
ments is shifted one place to the right on application of an ad-
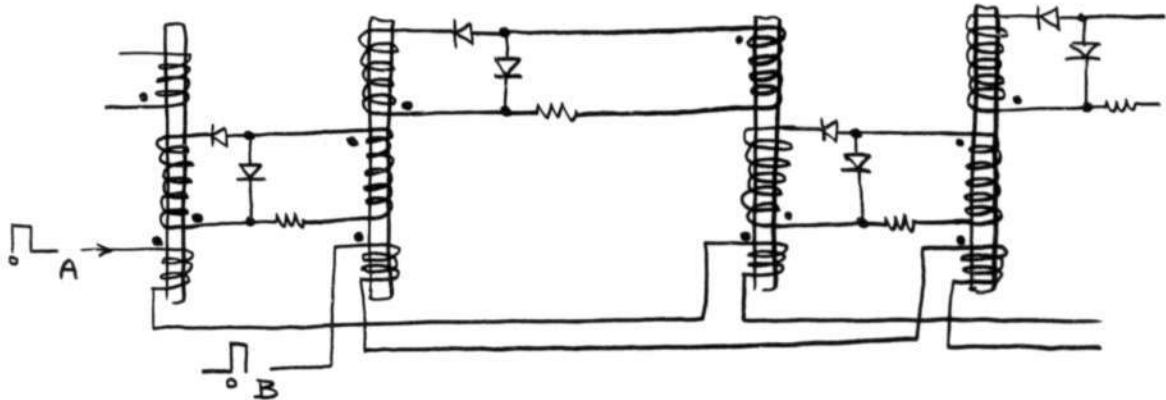vance pulse. In Sims' circuit, each compartment contains two cores;

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if adjacent cores were allowed to hold 1's, then the <u>advance</u>
pulse would be trying to <u>clear</u> the second core while the first
core was trying to <u>set</u> it.

Assume that initially every core is magnetized <u>up</u> (≈ 0).
Then current in the driving windings does nothing. Inject a "1"
into the first core by driving it <u>down</u>. At time t=o, pulse line
A. This clears the first core and reads its "1" into the second.
At time t=1, pulse line B. This advances the "1" into the next
compartment. Two pulses are required for a complete shift from
one compartment to the next. The second core in each compartment
is for temporary storage.
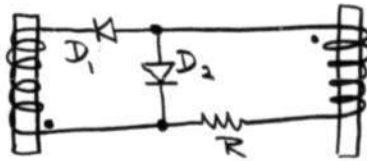
DETAILS OF COUPLING CIRCUIT

D_2 in series with R shunts undesired current when reading out of
core 2. Without R, D_2 would represent too high a load and tend to
prevent the switching of 2. D_1 prevents loading down 1 when read-
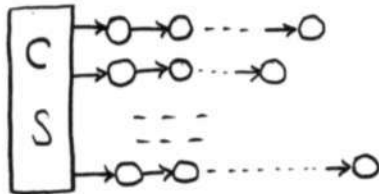ing a "1" from 1 to 2.

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Application to Control: In case we do not require
a general stepping register, but only require a single "1" to
be advanced down the line, the rest of the cores being "0",
we can use one core per stage instead of two.

One proposed method of central
control is to have one stepping
register per operation. The
control switch injects a "1" into the first core of the stepping
register representing the order to be performed; the "1" then
advances down the line. The pulse output at each step is used
to send commands to appropriate points in the machine. There
remain, even if the stepping register were perfected, problems
of mixing pulse outputs without back-up of information.

A stepping register of the type described has been
built. It gives a $\frac{1}{2}$-microsecond output pulse every 0.7 micro-
seconds. Cheerio-size ferrite cores (MF 1118) are used.

Briggs: Magnetic switch.

The stepping register described above, like other mag-
netic logical circuits, uses diodes to prevent back flow of in-
formation. These diodes must tolerate high forward I and back E,
with a consequent loss of reliability. A magnetic core switch
or "gate" has been developed for this application.
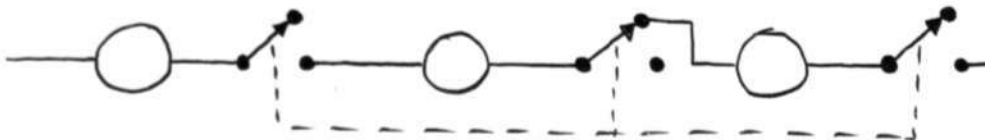
Two such switches operating in conjunction, one before and one
after each stage, can prevent back flow as shown. A rectangular
hysteresis loop is not necessary, but a saturation characteristic
is needed.

FIRST VERSION

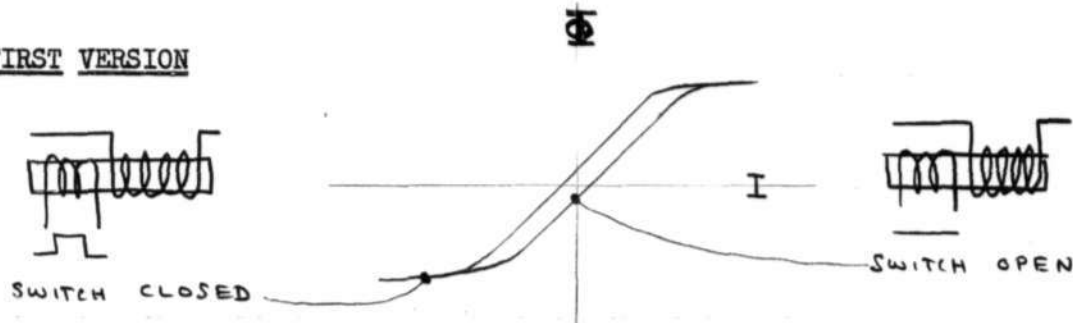SWITCH CLOSED   SWITCH OPEN

The gate core I is applied 0.5 microseconds before the pulse which transfers the information through the switch. This closes the switch. With no gate I, the switch is open.
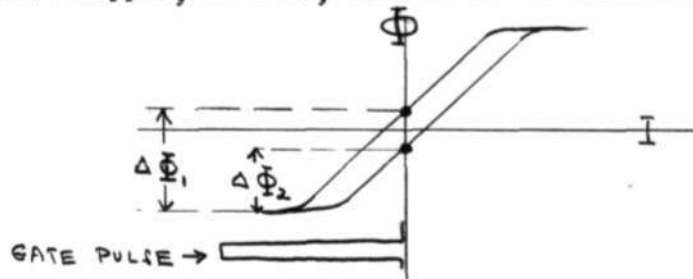
This scheme doesn't work because the gate current reads information out of the gate, and this appears as spurious information in the second core.

SECOND VERSION

Here the spurious outputs from the two gate cores are supposed to buck out.

This doesn't happen, however, because of the residual induction.

GATE PULSE →

The effect of the spurious output is to disturb the "1" just before readout, which progressively deteriorates the information. Solution: apply a MMF bias to both cores at all times.
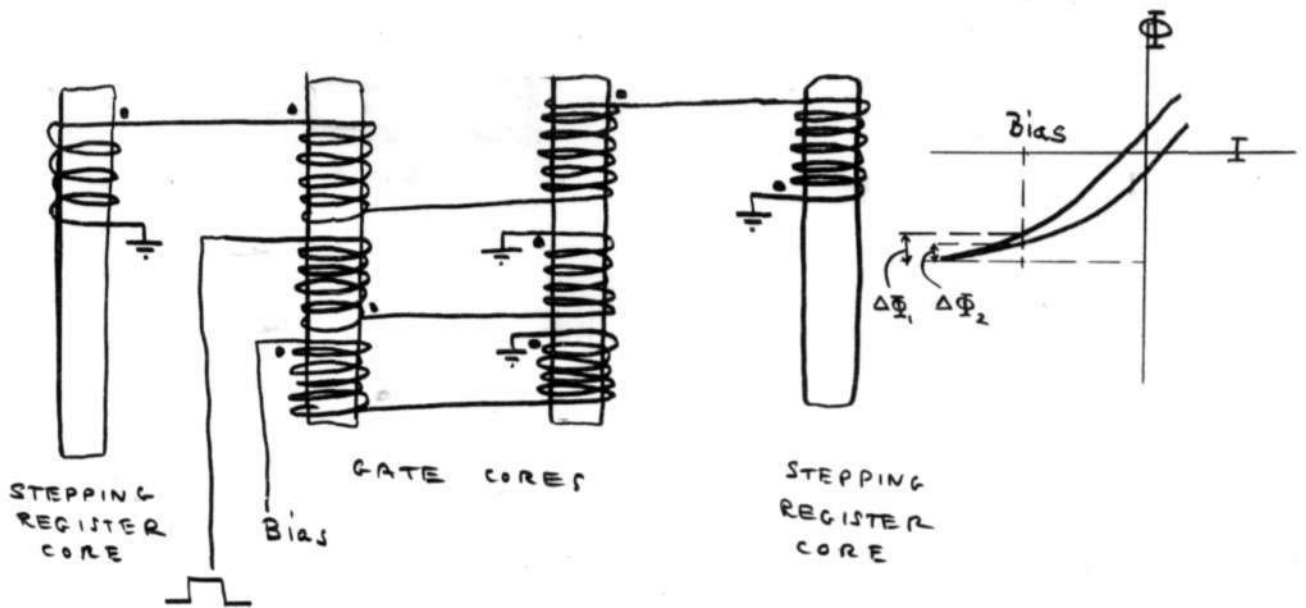
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FINAL VERSION

STEPPING
REGISTER
CORE

Bias

GATE CORES

STEPPING
REGISTER
CORE

Φ

Bias

I

$\Delta\Phi_1$ $\Delta\Phi_2$

The difference $\Delta\Phi_1 - \Delta\Phi_2$, due to the gating pulse above, is now practically negligible, and hence spurious introduction of information no longer is serious. However, with no gating pulse the switch still is open: <u>one</u> core still has a fairly large $\frac{d\Phi}{dI}$, since it is being swung <u>up</u> the Φ-I curve to the right. The other core looks like a short-circuit, since it is being swung out on the <u>saturation</u> leg to the left, but this doesn't affect the net open-switch effect.

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RCJ:NHT/bs

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