CONFIDENTIAL

UNCLASSIFIED

#1776

Library

Memorandum M-1466

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: <u>WWII BLOCK DIAGRAMS MEETINGS OF APRIL 16-17, 1952</u>

To: WWII Planning Group

From: W. A. Hosier

Date: April 28, 1952

CLASSIFICATION CHANGED TO:
DD 254
Auth:
By: R. R. Everett
Date: 2-1-60

Abstract: This note summarizes the discussion at the above meetings for
the benefit of those who may wish to trace the course of thought
on the subject.

Present: G. R. Briggs   H. R. J. Grosch   B. Fahnestock
          D. R. Brown   W. A. Hosier   R. P. Mayer
          R. R. Everett   R. C. Jeffrey   I. S. Reed
          J. W. Forrester   W. Ogden

LIN LAB DIV. 6
DOCUMENT ROOM
DO NOT REMOVE
THIS ROOM

    It was pointed out at the outset of this meeting, as has been
said before, that the control system of WWII is still in a "wide open"
state compared to memory and arithmetic elements, and that it would be
most helpful to have as concrete a proposal to look at under the control
heading as one has under the other two.

    J. Forrester proposed that there is perhaps a hierarchy of com-
ponents and decisions applicable to the machine - that is to say, an order
in which its aspects ought to be considered so that later decisions will
have a minimum of undesired retroactive effects on previous ones. He sug-
gested that if tentative systems are elaborated into enough detail, we may
have a better notion of what this order is, and be able to impose a pattern
of growth on WWII that fulfills itself somewhat more easily and consistently
than did that of WWI.

    A brief discussion of components ensued:

    (a) with regard to transistors, J. Forrester said that the quality
and quantity observed at GE the day previous was not encouraging; that for
our purposes, transistors are still too slow and subject to too much varia-
tion. R. Everett pointed out that this is particularly true of their operation
in pulsed circuits. I. Reed remarked that a tendency of transistor flip-flops
to oscillate, due presumably to low input impedance of the transistor, has
been inhibited in some cases by sufficient bias.

CONFIDENTIAL

UNCLASSIFIED

CONFIDENTIAL
UNCLASSIFIED

(b) with regard to magnetic cores, D. Brown observed that of 6 batches of ferrite cores recently made by General Ceramics and tested by us with our equipment at their plant, only the first batch was acceptable. Also, some of the Mo-permalloy cores have turned up with long switching times, up to 50 μs.

(c) the production of junction diodes at GE is not yet under adequate control, and their output is subject to considerable fluctuation.

I. Reed outlined briefly what might be called the "operation counter" of his 4-order computer proposed earlier. This 3-bit counter, capable of 8 states, was so constructed as to count through a cycle having 4 alternate branch loops, one for each of the 4 basic orders: "subtract", "transfer to control " (cp), "transfer back to memory and shift right", and "halt". This proposal has been written up in more detail by Reed and Jeffrey in an unnumbered note distributed at the meeting of April 24.

In response to J. Forrester's desire to have a more concrete display of how much "hardware" is implied by an abstract logical proposal like Reed's, and to be able to answer questions like how many levels of diodes are cascaded, driving and being driven by other diodes, circuits are suggested in the Reed-Jeffrey memo for realizing the logic in terms of (a) crystal diodes, (b) gate tubes, (c) magnetic cores.

A propos of Boolean methods, Mr. Forrester quoted a member of GE's engineering staff as saying that application of such analysis to television transmitter switching circuits enabled them to eliminate as much as 80% of the relays in some cases.

H. Grosch then outlined a means of instantaneous shifting similar to the system used in IBM's 604 (it has been suggested by various people that if WWII uses, say, a 32-bit word, then, since 7 bits would probably suffice for order and 16 for address, there would be at least 7 bits left to designate such other functions as the number of places to shift left or right). Briefly, this consisted of a rectangular matrix with 32-bit input lines y_0 to y_{31}, and similar output lines x_0 to x_{31}, with a core at each of the 1024 intersections. The 63 diagonals $x = y + n$ $(-31 \leq n \leq 31)$, are threaded through these same cores, so that a pulse of $I/2$ on input y_k and diagonal $\underline{n}$ will give a shifted output pulse on $x_{k + n}$.

R. Everett thought the total time saving so accomplished on the average program might come to 6%; he said that more time, perhaps 30%, could be saved by a similar condensing of the high-speed carry.

Such a possibility was shown by a proposal of G. Briggs - a flip-flop adder using parallel magnetic gates for carrying (see Fig. 1 attached). It uses $\frac{n}{2}(n + 1)$ cores in the carry matrix, but at most $\underline{n}$ of these are switched simultaneously.

CONFIDENTIAL
UNCLASSIFIED

CONFIDENTIAL

R. Everett cited W. Papian as saying that a series arrangement of cores for the high-speed carry would not necessarily have an operating time equal to the sum of the individual core-switching times, since the $d\phi/dt$ in a core would initiate switching of the core following before the first core had entirely switched.

R. Mayer carried further his study of the "single register" computer (E-459), detailing the "multiply" order. This was logically the same as the WWI order, with the minor exception that at the end of the operation <u>mh</u>, it is B_0 which will always hold a 0 rather than B_{15} as in WWI.

The total time needed for multiplying two 15-bit numbers is 301 μs. Mayer estimated that 4 μs of program timing could be saved by having an electronic program counter register; this could then also double as a step-counter, and would save 4 μs per multiplier digit.

In connection with the problem of saving time, Mr. Forrester asked Mr. Grosch to organize a survey of the available information on the percentage of operating time devoted to individual orders (see Grosch's note M-1464). Mr. Everett mentioned that he had more or less done such an analysis for the "2-register" computer.

Mr. Forrester suggested that it would be helpful to have from the components groups a proposal for control which is as concrete as the present ideas on a memory: for example, that W. Papian and N. Taylor propose a form of stepping register. Engineering problems that arise will probably include maintaining pulse shape under a variety of loads, and mixing of command pulses.

Under the heading of reducing variety of components by having one component perform more than one function, it was mentioned that building the control matrix as part of the memory might conflict with the notion of a high-power control matrix.

Closing discussion at Wednesday's meeting turned on the merits of iterative techniques for operations like <u>mr</u>, <u>dv</u>, square root, etc.; it was generally agreed that the slowness of iterative techniques made them impractical except for infrequent operations.

CONFIDENTIAL

CONFIDENTIAL

Thursday, April 17

Present: G. R. Briggs   J. W. Forrester   R. P. Mayer
          D. R. Brown   H.R.J. Grosch   H. Fahnestock
          R. R. Everett   R. C. Jeffrey
          S. H. Dodd   W. A. Hosier

        Thursday's meeting began with R. Mayer's sketch of a stepping
register to perform the order ad in his previously proposed computer. The
same sequence of commands also sufficed for su with the addition of a "com-
plement" pulse.

        The question arose, "Can these registers work without diodes?"
G. Briggs answered that Harvard has done this - but not reliably. The
shunt diode is easily left out of the circuit coupling two cores, but the
series diode, which decouples the driven core from its load, is not so
easily dispensed with, and its omission in the Harvard system had to be
compensated by a tricky leakage inductance. Briggs noted further that
drawing power out of such a register might slow it down.

        R. Mayer suggested that a possible means of hanging a more uniform
load on the stepping registers might be to have them set up other "command
cores" which would be pulsed out at a higher power level; or tubes might be
interposed in this buffer position. It was thought that the logical design
might have as one of its purposes to even up the loads on driver elements
as far as possible; further, to reduce the number of destinations of command
pulses.

        Of 23 command-pulse destinations in Mayer's 2-register machine,
he considered 10 to be constituted of cores, and the other 13 presumably of
tubes (R. Everett favors 7AK7's). It was thought that a reasonable top
speed figure (with unknown reliability) now realizable in a stepping register
with ferrite cores and germanium diodes, is 400 kc. It was proposed that
Mayer outline a stepping-register system using only 2 clock-pulse lines,
with a more detailed sketch of pulse origins and destinations.

        D. Brown proposed a simplified WWI control using ORDVAC techniques,
with cores instead of crystals; R. Mayer's control-matrix-in-memory scheme
was also brought up; but both these plans were shelved because they require
maintenance of switching voltages throughout the order sequence instead of
only to initiate it.

        One feature of R. Mayer's stepping-register control was an arrange-
ment of gate generator and gate tubes to short-circuit some of the program
timing in executing the order cp. R. Everett suggested that the relative
infrequency of the cp order would permit one to do it more slowly, simply
marking time during the unnecessary pulses of program timing and thereby
simplify the circuit.

CONFIDENTIAL

CONFIDENTIAL
UNCLASSIFIED

In the interests of simplicity and trouble-shooting, he expressed a distinct preference for having separate channels for separate orders, even if this means redundancy of equipment, pointing out that interconnections and time-sharing of channel components are what cause ambiguous symptoms and make diagnosis difficult. J. Forrester agrees to this, in general, as does S. Dodd. It was admitted, however, that this argument carries more weight in a large machine than a small one. Perhaps a distinction can be drawn by the question whether or not extra equipment (gate tubes, etc.) is needed to switch channels in and out of their common component - e.g., is the single electronic register proposed by Mayer, Forrester, Everett et al. inherently more difficult to diagnose than several separate simpler registers?

There was no objection to using a single register for all shift orders, since the selection switch can simply determine where to break into the chain.

S. Dodd thought it a drawback in stepping registers if they can not be stopped at a chosen pulse for pulse-by-pulse trouble-shooting (N. Taylor had previously doubted the importance of this). It was further agreed that diagnosis of errors would be rendered more difficult by the control switch's not holding the order after initiating it, thus necessitating a return to storage to find out what the order was.

In concluding the Thursday meeting, H. Grosch outlined a matrix proposal for instantaneous multiplication of integers up to 15, which would reduce the number of steps in a multiplication by a factor of 4 but would require a minimum of 1040 cores, plus 145 more if it were to add as well as multiply. There may of course be problems in driving these cores and in the time they take to effect switching.

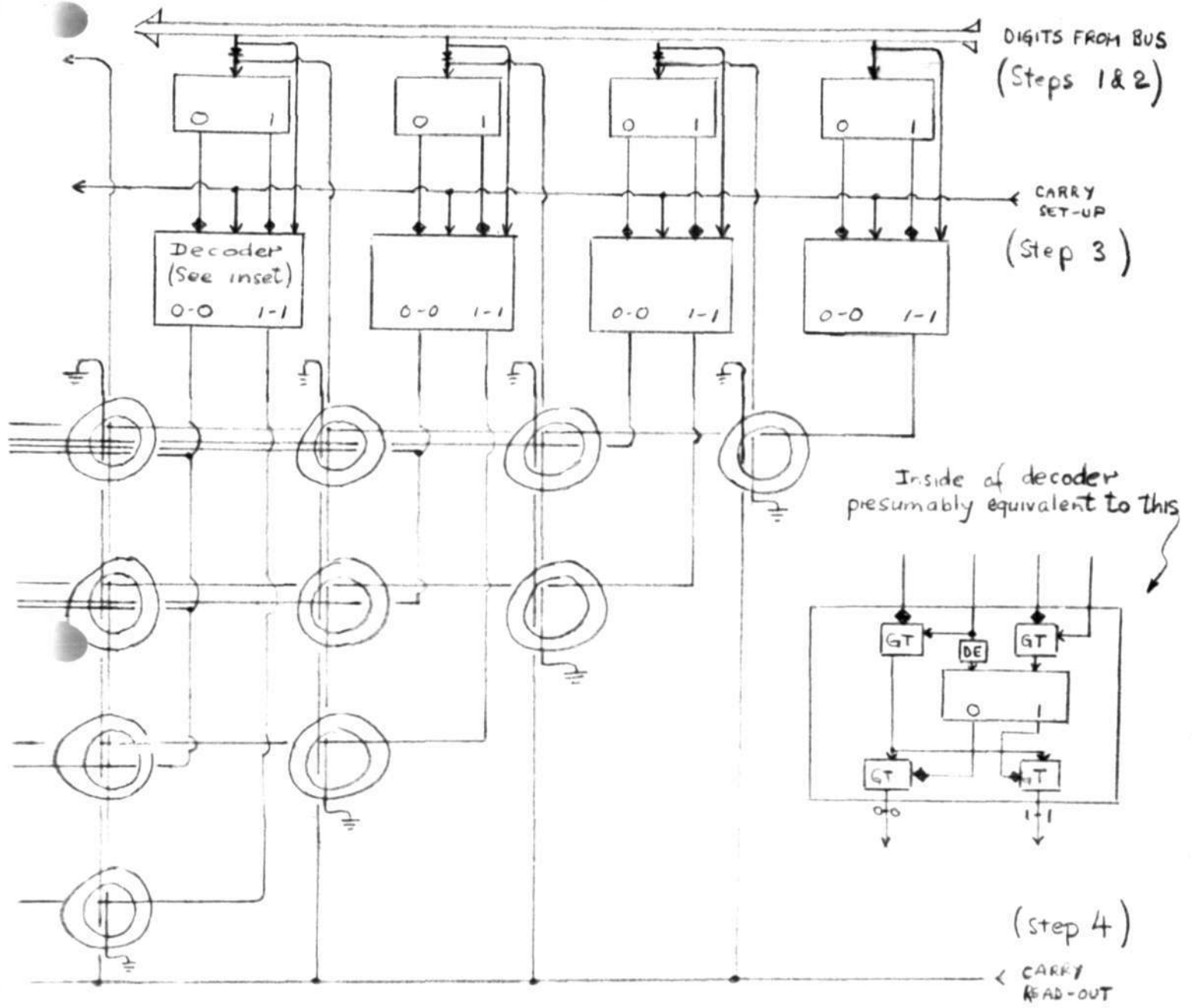SIGNED _W. A. Hosier_
W. A. Hosier

APPROVED _N. H. Taylor (by bs)_
N. H. Taylor

WAH/cp

UNCLASSIFIED

CONFIDENTIAL

G. BRIGGS'S PARALLEL CARRY ADDER

Carry set-up pulses originating at a 1-1 are propagated until bucked out by a 0-0.

Those cores which have been set up are then pulsed out to complement accumulator flip-flops on step 4.

Fig. 1

A-51420