Digital Computer Laboratory
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SUBJECT: MAGNETIC CORE ACTIVITY

To: N. H. Taylor

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Abstract: The 16 x 16 metallic array has been operated successfully. Only partial operation of the 16 x 16 ceramic-core switch-driven array has been accomplished. Some progress has also been made with pulse transformer investigations, ferroelectric storage, and new magnetic materials.

A verbal report on the status of the work being done with magnetic cores was given at a meeting held here on 4 January 1952. This memorandum is a post-facto attempt to put on record the information which came out during that meeting; it is organized according to each independent activity. A reasonable background knowledge about the activities is assumed; such information is available from the Bi-Weekly and Summary Reports.

1.0 THE METALLIC ARRAY

A fair demonstration of the practicability of the multi-dimensional magnetic-core memory scheme (see R-187 by J.W.F.) has been given by recent successful operation of our first 16 x 16 metallic array.

An arbitrary information pattern has been put into the array. The information in each successive core has been read and rewritten at a 4 kc rate, giving an array-scanning frequency of about 16 cycles, as limited by the surrounding test equipment. The switching time of each core was about 10 microseconds using a selecting-current ratio of 2:1. The worst ONE-ZERO ratio (taken on an amplitude basis at the sensing-time point) was about 4:1. A test of current-variation margins indicated that any one coordinate current could be varied by more than ±10% without interrupting operation. Partial operation of the array using 3:1 selecting-current ratios has also been accomplished and resulted in a reduction of core-switching time to roughly 5 microseconds.

The fact of error-free operation for periods as long as several hours is highly encouraging in view of the very large variation of characteristics among the 256 cores and the incomplete state of development of the logical test equipment surrounding the array. It is believed that two

major lines of future effort should be to construct new arrays out of cores with greater uniformity of characteristics, and to remodel or replace surrounding test equipment until the logical test setup performs with a high degree of reliability. A third line of effort is, of course, aimed at obtaining significant data from the test operation of the array for use in future design work and reliability estimates.

2.0 THE CERAMIC ARRAY AND SWITCH

This array has been progressing only slowly in the last few weeks. Two salient ways in which the ceramic array is different from the metallic one make the former a much tougher problem. One is the fact that it consists of two closely coupled new devices, the array and the driver switch, each of which has its own development problems; the resultant problem is greater than just the sum of the two because of the close coupling between them. The other difference is in the use of ceramic instead of metallic cores; this means cores with less desirable B-H characteristics and, also, a faster speed range where timing and circuitry details become more critical.

Nevertheless, partially successful operation has been achieved on a 2 x 4 portion of the array. Scanning was at a low rate, address-setup time of the order of 2 microseconds, and reading and rewriting took a little over 3 microseconds. ONE-ZERO ratios were of the order of 2:1 on an amplitude basis and 4:1 or so on an area basis.

Immediate development problems center largely around the driver switch and its coupling to the array. The big longer term problem is concerned with obtaining satisfactory core materials.

3.0 OTHER ACTIVITIES

Some work is being done in the areas of pulse transformers, ferroelectric storage, other computer components, and new materials. These are discussed below.

3.1 Pulse Transformers

The present effort in this area is to duplicate the performance of the present WWI pulse transformer using a small ferritic core. Some successes have been achieved experimentally.

Plans include testing a worthwhile new design in a few of the 5-Digit Multiplier circuits. Background and experience gained in the present work are expected to lead to a complete re-evaluation of our pulse-transformer designs and design methods, and the development

of any desirable new units for future applications. Should time allow, a short survey of the possibility of improving delay line designs by the use of ferrite rods will also be made.

3.2 Ferroelectric Storage

Some barium titanate slabs have been operated as memory units, but indications are that present materials will not yet work successfully as coincident-voltage memory units.

Switching times for these slabs have run around 2 microseconds, and undisturbed ONE-ZERO ratios were about 2 or 3.

3.3 Other Computer Components

Engineering Note E-438, by D. A. Buck, summarized the group's to-date thinking about the use of magnetic cores as flip-flops, gates, counters, etc.

A carrier type of magnetic-core flip-flop is being investigated, and work is expected to start soon on examining the possibilities of making a binary adder out of cores.

3.4 New Materials

Improved magnetic materials continue to arrive slowly, and a limited amount of measuring and evaluation goes on.

The responsibility for obtaining such improvements is being shifted over to D. R. Brown who also expects to start a complete and organized measuring, testing, and record-keeping program.

Equipment is being designed and constructed for acceptance testing and for life testing of ceramic cores. Liaison with other users and producers of our type of maghetic cores is good, particularly in the area of test techniques and standards.

An outline of the rectangular-loop core-testing problem is attached.

SIGNED _____
William N. Papian

APPROVED _____
N. H. Taylor

APPENDIX

Outline Notes on Rectangular-loop Core Testing

I. TWO BROAD TEST PURPOSES

A. Development Testing

B. Acceptance Testing

II. DEVELOPMENT TESTING; NEW MATERIALS; PUBLISHED CHARACTERISTICS

A. B-H Families

1. Quasi-static loops

a. Symmetrical

b. Biased

2. High frequency loops

B. Pulse Tests

1. Curves of switching time versus amplitude of applied step of H

a. Symmetrical excitation

b. Asymmetrical excitation

2. Specialized pulse tests

a. Ratio of switched output (ONE) to not-switched (ZERO) output

b. Coincident-current memory test (Disturbed signal ratios)

III. ACCEPTANCE TESTING - SOME COMBINATION OF II THAT IS SUFFICIENTLY SIGNIFICANT AND SUFFICIENTLY SIMPLE

A. B-H Families Not Satisfactory

1. Quasi-static ones ignore important time factors and are difficult to obtain on very small samples.

2. High frequency ones are valuable to user at given frequency only; they are difficult to obtain at worthwhile high frequencies because of dissipation and circuitry problems.

B. Pulse Tests

1. Switching time versus H too complicated to obtain.

2. Specialized pulse tests wrap up B-H characteristics and time factors in one convenient package.

a. Switched to not-switched outputs fine for most applications.

b. Coincident-current memory test a refinement of (a); needs small amount of additional equipment.

IV. A TECHNIQUE FOR PULSE ACCEPTANCE TESTING

A. Maker and User Determine Following

1. Desired sequence of current pulses

2. Resultant output-voltage limits (either certain points or complete waveshape)

3. A couple of "calibrating" cores corresponding to above limits

B. Engineer Sets Up Equipment Using the "Calibrating" Cores and Draws or Otherwise Indicates the Limit Points or Curves on Scope Screen.

C. Assistant Runs Tests

1. Cores are "mounted" on test jig a group at a time, including the two "calibrating" cores.

2. Core outputs are looked at singly.

3. Reference is made back to "calibrating" cores for each group of tested cores to assure that equipment adjustments are holding.