Digital Computer Laboratory
Massachusetts Institute of Technology
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SUBJECT: WWII BLOCK DIAGRAMS MEETING OF MAY 1, 1952

To: WWII Planning Group

From: W. A. Hosier

Date: May 8, 1952

Abstract: This note summarizes the discussion at the above meeting for the benefit of those who may wish to trace the course of thought on the subject.

Present: G. R. Briggs, R. C. Jeffrey, D. R. Brown, R. R. Mayer, H.R.J. Grosch, I. S. Reed, W. A. Hosier, N. H. Taylor

To begin with, there was discussion of J. Forrester's note of April 29, "Boundary Conditions for WWII Design" (M-1468). In view of the introductory remark that performance figures from columns more than two units apart should not be combined, it was somewhat puzzling that brief completion time should be linked with the more difficult designs. D. Israel explained later that the conclusion to be drawn from this arrangement is that if an optimum computer could be achieved in the longest time, a compromise of a near-optimum computer sooner would be better.

N. Taylor observed that reliability figures other than the "poorest acceptable" are difficult to foresee under present conditions; also that probably 36 months is a minimum completion time. Probable speed and storage capacity he thought might be 30 μs per order and 4000 registers, using Mo-permalloy cores and transistors. He mentioned that transistors give promise as gates, having a reliability comparable to germanium diodes and offering gain besides, with a conservative speed figure of 2 μs. The order code was left an open question; it was pointed out, however, that the size of the memory would affect such of it as relates to correlation programs and terminal equipment.

For the benefit of those present who did not know what a "B-box" was, R. Mayer explained that it is a separate register containing a constant which can be added to the address of certain specified orders. The B-box itself may or may not be capable of counting or adding.

It was suggested that the contents of the B-box might on occasion be substituted for the address instead of being added to it; also that more than one B-box might be useful. If numerous B-boxes were used, the practical effect would be one of a two-address order code; it was felt that a forthright two-address system would be preferable. (D. Israel says nobody has ever found any use for more than one B-box.)

H. Grosch suggested that a 3- or 4-address system might be more efficient than the contemplated single-address, but this was denied by N. Taylor and others, partly on the basis of D. Israel's report M-1325.

Mr. Grosch also outlined the "criss-cross" technique of multiplication: grouping together those pairs of factor digits which are multiplied in the product by a common power of the base (e.g., $132 \times 645 = 10^0(5 \times 2) + 10^1(5 \times 3 + 2 \times 4) + 10^2(5 \times 1 + 4 \times 3 + 6 \times 2) + 10^3(4 \times 1 + 6 \times 3) + 10^4(6 \times 1) = 10 + 230 + 2900 + 22{,}000 + 60{,}000 = 85{,}140$). While this may offer advantages in a decimal machine, particularly in a serial machine, it would appear to be cumbersome in a parallel binary one.

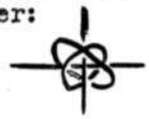
In a general discussion of whether simplicity and reliability are more easily achieved in a serial machine, I. S. Reed and N. Taylor observed that for comparable operating speeds, the serial machine offers little or no advantage, since its more complex control adds roughly the same amount of equipment as do the multiple channels of the parallel machine; and, further, makes it harder to understand.

N. Taylor made a rough "figure of merit" comparison of WWI and CADAC, as follows: (Germanium diodes being considered 10 times as reliable as vacuum tubes, 10 diodes are taken as equal to 1 tube)

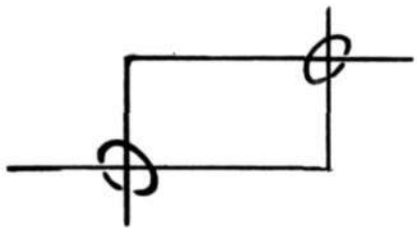
CADAC		WWI
2500	No. Diodes	11,000
250	÷ 10	1100
150	No. Tubes	5500
400	Effective "tubes"	6600
16	Operations per second	16,000
42	Word Length	16
$100,000	Est. Cost	$1,000,000

Using as a rough figure of merit the product (operations per second) x (word length) divided by the product ("tubes") x (cost), one has for CADAC a figure of 1.6×10^{-5}, and for WWI a figure of 4×10^{-5}.

A scheme for doubling the size of the memory without any change in the number of driving lines was outlined by D. Brown. This consisted of having two cores instead of one at the intersections of driving lines, so that the currents which add in the one core cancel in the other:



In practice, instead of the physically difficult situation of both cores at the same intersection, the driving lines are all simply made to cross twice, with one core at each of the two intersections:



All that the system then requires to switch the two cores independently is that it be possible for a driving current of I/2 to be put into one of the lines in either direction at will.

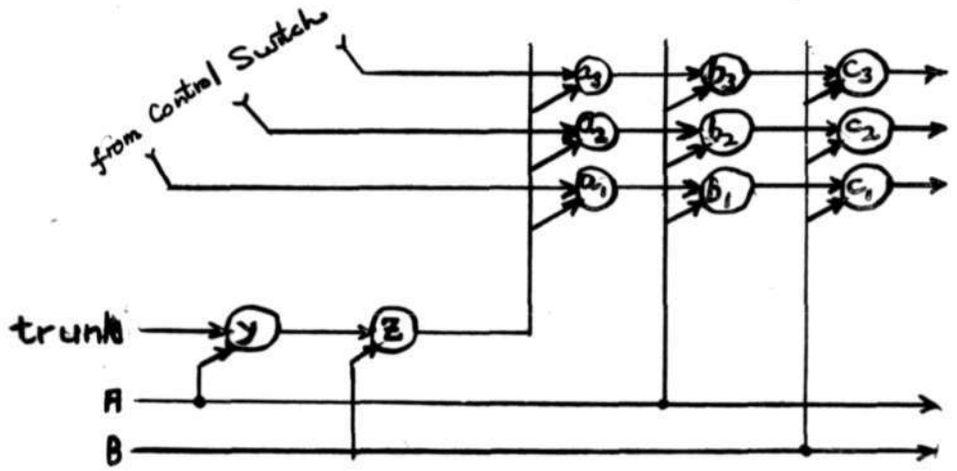
R. Jeffrey and I. Reed then launched a discussion of magnetic stepping registers, pointing out that such a register uses its cores inefficiently, assuming only n states out of the 2^n which are possible with n cores. However, it was generally agreed that this "linear" counter has simplicity of inputs and outputs that probably compensates for its excess of digits over the "logarithmic" (2^n) counter, and that the choice of one over the other for control purposes is probably a matter of which lends itself best to circuits at hand.

Possibly the linear register is better adapted to driving functions involving large amounts of power; however, whether or not any grouping of magnetic cores can be useful for such driving functions will depend on whether or not mixing of command pulses from several core channels is satisfactory. It was agreed that priority must be given to experimental effort on this mixing problem.

In this connection, G. Briggs brought up a device now under consideration for coupling magnetic cores at will by electrical means: a saturable reactor inductance in series with the two coupled cores, which presents in its unsaturated state an impedance high enough to prevent switching of the driven core, and in its saturated state an effective short-circuit. It is anticipated that a gate of this nature may be somewhat slower than desired; the saturating winding will probably have to be

energized somewhat prior to pulsing of the driving core. (It has been suggested in other quarters that the orthogonally-wound core proposed in D. Buck's note (E-454) on a Non-Destructive Read-Out may provide, by virtue of its acting as a one-way transformer, the desired means of mixing command pulses.)

In closing, Mayer and Jeffrey sketched a simple means of switching to one of any number of branch channels of a stepping register:



The driving lines A and B are alternately pulsed with 0's. This will propagate a 1 inserted at the beginning of the trunk line up to the core Z, where the propagated 1 will die if switch cores a_1, a_2, a_3.... all contain 0's. However, if previously the control switch has inserted a 1 in one of the switch cores, the 1 will continue to be propagated down the channel headed by that core, and no other.

SIGNED W. A. Hosier
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APPROVED N. H. Taylor
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WAH/cp