Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II MEETING OF MARCH 28, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and R. P. Mayer

Date: April 1, 1952

Members Present: C. Adams, G. Briggs, D. Buck, R. Callahan, D. Eckl, R. Everett, H. Fahnestock, J. Forrester, H. Grosch, W. Hosier, J. Hughes, R. Jeffrey, N. Jones, W. Linvill, R. Mayer, A. Moritz, J. O'Brien, W. Papian, R. Sims, N. Taylor, R. Wieser

Most of the meeting today was spent discussing D. Buck's non-destructive read-out, which is described in Engineering Note E-454. (Background information concerning square hysteresis loop material can be found in an E. E. Seminar paper, "Ferromagnetic Materials for Applications Requiring Rectangular Hysteresis Loops and Short Response Times", by W. Papian, written in January, 1950. This is available from the Barta Building library or from W. Papian.) This non-destructive read-out is interesting at this time because an experimental core has, within the past week, shown that the idea works quite well. Briefly, the read-out works by applying a magnetic pulse (by a "sensing winding") at 90° to the saturated flux (previously set up by a switching winding) in such a way as to obtain a read-out and yet not permanently disturb the saturated flux. The experimental core was made of Mo-Permalloy ribbon, and the ribbon itself was used for the "90° sensing winding".

This system allows us to build a flip-flop and gate combination which is rather similar to the electronic circuits of WWI, except that only one gate is connected to the flip-flop, and this gate gives a positive pulse representing "1" and a negative pulse representing "0". A destructive read-out is also possible. The output pulse from the gate is not a full sine wave because the flux lines are "driven up", and simply "fall back", so that the output wave form looks as shown in the sketch.

Note: (This wave form may require slower PRF.)

Pulsing the switching winding theoretically gives no output in the 90° winding because the two windings are not coupled. The 90° winding is effectively rotated when it is pulsed so that, according to D. Buck, any amount of power can be transferred to the output winding (which is closely coupled to the switching winding). Thus the core acts as a one-way transformer and might be used for isolation in place of crystals, as a buffer, etc.

If continuous AC is applied to the 90° winding, a phase detector is needed to tell whether a "0" or a "1" is stored. G. Briggs mentioned that it is possible to provide a direct feed-through to cancel the output for one phase, which will also provide a double-amplitude output for the other phase.

Since the output winding is closely coupled to the switching winding, a very large signal output occurs when reading-in. It is necessary to remember this in designing the circuits. One way of avoiding this unwanted signal is to make the read-in work so slowly that the signal is unobjectionably small. The experimental Mo-Permalloy ribbon core has an extremely fast read-out, but the slow read-in which is characteristic of metallic cores. Such a core may therefore be very useful for speed-change applications, such as read-in devices where information may arrive at a slow rate but is desired by the computer at a fast rate. J. Forrester pointed out that using the ribbon as a 90° winding may not be reliable because if the turns touch, the coil is shorted, but if the turns are separated too much, an undesirable air gap will result.

N. Taylor mentioned that specially-constructed ferrite cores with the 90° read-out may be worthwhile using in the arithmetic element (AE). It is worth expending special effort for this because only a few cores are required in AE, and AE must perform several functions at a high speed without disturbing the remaining number. However, since the core has effectively only one gate on each side of the flip-flop, we are faced with the problem of determining whether this is enough or whether there are ways of adding more gates. We must also solve the problem of suppressing the output when a core is switched fast.

The rest of the meeting was spent in discussing a single-time-pulse instruction system proposed by R. Mayer. In WWI several time pulses are used to accomplish program timing, which finds the next instruction and sets up the storage switch and the control switch. Program timing can be done with only two pulses if the storage selection matrix can be pulsed directly from the program counter (PC) so that it will immediately pulse the selected storage register, producing outputs from the storage. The first pulse, therefore, can obtain the instruction from storage and feed it to a temporary register, and the second pulse can send the instruction from there to the control switch and storage switch.

It is interesting to notice that this second pulse, in sending the address to the storage switch, can (by the above system) immediately read the number out of storage into the AE or vice versa, depending on the setting of the control switch. Thus, for many instructions, program timing occurs on one time pulse and operation-timing on the second time pulse.

This process can be reduced to one time pulse if two independent storage banks are used: The instruction coming from storage is not fed to a temporary register but is fed directly through a different selection matrix, immediately sending a number from storage to AE, or vice versa, depending on which instruction pulse occurs (at the same time). Thus, for many instructions, the entire operation works on one time pulse so that a pulse-generator, feeding single time pulses into the system, carries out the instructions.

If the pulse-generator is replaced by a completion pulse from the control switch, then the computer runs asynchronously (or with "no" time pulses). Presumably, the control switch could be set up to operate a step-register delay-line type of pulse distributor discussed last week, in which most of the instructions would produce an end-carry on the first step. It should be remembered that it may be necessary to operate several computers synchronously. The computers might be synchronized on each time pulse, or only when transfers between them occur. In any event, it may not be worthwhile to operate each computer asynchronously.

With the two independent storage banks required, instructions cannot refer to numbers in the same bank. The resultant programming difficulties can be avoided by taking instructions from the banks alternately, so that the programmer can get any number from storage either when he wants it or on the next instruction. This programming inconvenience can also be eliminated, by automatically using a second time pulse for any instructions referring to numbers in the same bank. Then the programmer can, if he wishes, make all instructions take one time pulse, but he does not have to worry about doing this.

This system is not supposed to solve all problems in making a fast computer, but simply to point out what appears to be a way of designing the logically-fastest computer. There is no logical necessity for any delays in this system, except between instructions. (Some operations - like multiply and shift - will, of course, require more than one time pulse if a WWI-type arithmetic element is used.) However, from an electronic point of view, certain delays are required to make sure that the simultaneous mixing in the selection matrices operates properly and to wait for the electronic and magnetic circuits to function. Also, it must not be assumed that the entire process can be carried on without any amplifiers.

J. Forrester pointed out that the number of time pulses used in an instruction may not be a valid criterion for determining how an instruction should be built. It may be better to use several time pulses to help with the electronic problems, and C. Adams pointed out that the speed of the equipment is a determining factor regardless of whether one or many time pulses are used in an instruction. N. Taylor pointed out that the problem is largely a question of whether a return-to-zero system is used or not, that is, whether an electronic condition will be established and then sensed or whether the establishing of the condition produces (by differentiation) the necessary "sensing". Most of the remaining discussion concerned the relative bandwidth required for the non-return-to-zero system. It was suggested that the ORDVAC-type computers make use of this system and should be investigated, but it was also pointed out that little information on their control system is available. The final conclusion was that the non-return-to-zero system used in the single-time-pulse instruction requires a smaller bandwidth and might, therefore, be allowed to operate more rapidly than other systems.

Rollin P. Mayer
Rollin P. Mayer

Norman H. Taylor
Norman H. Taylor

RPM/NHT:bs

Security Information