Memorandum M-1321

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Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: Fourth Meeting on Air Defense Computer

To: Jay W. Forrester

From: B. E. Morriss

Date: November 8, 1951

Those present were:

Forrester, Jay W.
Adams, C. W.
Brown, D. R.
Everett, R. R.
Israel, D. R.
Linvill, W.
Morriss, B. E.
Papian, W. N.
Taylor, N. H.
Walquist, R. L.

Mr. Israel began the meeting with a discussion of his investigation of multiple address order codes and concurrent operation of two banks of storage. Grouping the orders for three of the programs used by his group yielded the following divisions:

	% of program	average order
cp, sp	15%	Read + 1/2 restoration + 8μs
ca, cs, ad, su, cm, sa	45%	2 Reads + 1/2 restoration + 8μs
ao, qe, ts, td, ta	25%	2 Reads + write + 1/2 restorations + 8μs
mr, mh, dv	10%	2 Reads + 2 restorations + 20μs
sl, sr	5%	Read + 2 restorations +12μs

It is interesting to note that these times check closely with those found by R. P. Mayer for a large number of different types of programs.

The concurrent scheme was the use of two banks of storage, one for orders, the other for data and constants. While the data or constant for one order was being operated upon, the next order could be simultaneously withdrawn from the order storage bank. The use of the concurrent scheme was of major importance only if storage access time was high. For storage access times of 20µs, operations with this scheme would be about 1.45 times as fast as present operations. With multiple address order codes the results were similar. Because all possible combinations of single address orders cannot be made available, a sufficient number of orders are wasted to reduce the average speed to that of a single address order code. This would mean that storage space is being wasted in holding the longer orders. With access times of the magnitude discussed for Whirlwind II (2-3µs), there appears to be little or no virtue in either scheme. These two schemes are discussed in some detail in memorandum M-1325.

There does appear to be some virtue in placing more than one piece of information in a single register, i.e., x and y coordinates of an aircraft. With low storage access times the saving here results from less indexing in the programming. Mr. Walquist presented figures from one program in which 25% of the storage registers and 15% of the operating time were used for indexing data or program. Mr. Israel felt that in a program such as would be used with Air Defense system perhaps 50% of program could be indexing. Several possible solutions to the indexing problem were given: A block transfer within storage; the renumbering of storage registers by changes in selection system; the use of the "B" box technique used by Wilkes. At first glance the "B" box appeared to offer advantages over the other proposals. It probably would be as simple or simpler than the other approaches. It would offer a great deal more flexibility than the renumbering of storage, and should require less time than the block transfer within storage. None of these points were discussed sufficiently to draw definite conclusions. There did not appear to be any reason why the "B" box would not be applicable to the ideas presented earlier by Mr. Everett on a "single" register machine. While it was not a solution to the indexing problem, it was mentioned that as a programming technique it is sometimes better to index program orders referring to target data than registers of target information and vice versa. Mr. Everett said that it has been said that some techniques such as the "B" box are more difficult to accomplish with a parallel machine than with a serial machine. He did not believe that this was necessarily due to the parallel nature of the machines as much as to the great difference in speeds involved.

Mr. Adams, Mr. Walquist, and Mr. Israel were asked to investigate the question: Where does operating time go? What are the sorts of things on which long periods of time are being spent? This question was asked to find the answer to what sorts of special orders might be justified. Examples of such orders which have been mentioned in the past are a sin-cosine order, the inverse tangent order, the square root order, and the automatic correlation order. Mr. Adams suggested that an automatic conversion to x, y coordinates might be much more useful than the sin-cosine order. Mr. Israel said that with 1,000 aircraft, 5,000 conversions to x, y coordinates which now requires 40 orders, 1,000 inverse tangent solutions which now requires 40 orders, and 1,000 square root solutions which now require 20 orders would be necessary in the program for each scan of the radar. This would be 260,000 orders of which the x,y conversion is by far the largest part.

The next question discussed was that of balance between speed, simplicity, and cost. This question caused a great deal of disagreement within the group, although much of this disagreement appeared to be a question of semantics. It was asked: "The use of a single register computer is simple but slowed down by necessity of performing one step at a time. Is this good or bad?" With only this information, it is impossible to answer the question. With curves showing the relationships of cost, complexity, and usefulness an answer might be found, but the group did not seem able to agree to definitions of cost, speed, and usefulness, much less to the shapes of these curves and where the sharp changes in direction occurred. It seemed generally agreed that maintenance, which is a part of the cost, increases more rapidly than complexity, and that usefulness goes up faster than speed. It was said that marginal improvement is reached when doubling the complexity does not double the speed.

Some of the other statements which were made are listed here.

Reliability and complexity are not dependent on the amount of equipment alone, but also on components and techniques used.

Cost is not dollars or vacuum tubes alone, although vacuum tubes may be the better measure. It is intimately tied up in the question of ease of maintenance.

At present speed levels costs have not risen as fast as operating speeds.

A complex logic must make maintenance more difficult.

The fewer the number of different types of building blocks which are used, the simpler the logic and the better the job of development which can be done on each block. It is certainly nice to save components, but if this increases the number of different types of building blocks used and therefore complicates the logic, it may not be a good idea.

The increasing of the complexity of the logic by separation of functions or reducing components was discussed. Some of the group felt that WWI was quite simple because each box performed a single function, while others felt that not collecting all of control at one point made the logic more complex. The question of simple or complex logic may be due to the particular approach used by the individual and his ability or inability to explain the process easily. A quite simple event may be very difficult to explain or define. The point was well made that new things usually appear more complex than things with which we are familiar, and therefore new ideas should not be immediately discarded just because they appear somewhat more complex than the familiar. The dynamic flip-flop appears complex, but because it does not strain components and appears well suited for the transistor it may be a very good idea.

It was stated that much of the CRC computer's simplicity comes from the use of the drum rather than from the time sharing or combinations of circuits.

The following table was presented to show that increasing the number of vacuum tubes to increase speed may pay off materially.

	Operations per second	Vacuum Tubes	Vacuum tubes per Operation per second
CRC	100	200	2
WWI	20,000	4,000	0.2
Everett Core Computer	20,000	200	0.01

The first two lines show that more operations per tube have been achieved by increasing the number of tubes. Since up to a certain point tube life is largely measured in hours, an effort should be made to obtain as many operations as possible. With only one tenth of the number of tubes naturally less maintenance will be expected for the slower computer, but since 200 would be necessary to obtain the same number of operations per second, to say nothing of interchanges of information and coordination, would one-hundredth of the time be adequate? Some of the members did not feel that it was fair to compare two machines designed with completely different objectives in this manner, but that it was sufficient to say that the slower machine will not handle the problem at all. This in itself justifies the faster and more complex machine. Mr. Everett is writing a memorandum discussing this question of cost, complexity, and usefulness.

Mr. Forrester said it was not a question of whether to build a machine or not, but rather to build the best machine possible considering speed, cost, capacity, and complexity. For the problem under consideration all of the reasonable speed and capacity will be used and more will be desired by the users.

It is planned to continue with a general meeting a week which will be used largely for distributing information. The smaller groups working on transistors, magnetic cores, and other problems discussed but not answered, will present their work at these meetings. Mr. Taylor is supervising this group and will plan the meetings.

The suggestion was made that anyone who felt that particular questions or points had been discussed insufficiently or who did not agree with the conclusions which had been drawn should write a short report on the subject. These will be gathered together as they are written and printed.

Drum Storage Systems by R. L. Walquist

In considering any new computer, the storage system utilized must not be overlooked. In particular, the advantages of various types of storage elements need to be carefully weighed against each other with the result that a single type of storage system will probably not result. In this respect, each of the various types of storage should be used by taking advantage of their strong points, while using them under circumstances which place a minimum stress upon their weak points.

In line with this sort of thinking, it is not clear that it is either necessary or desirable to design a computer for Air Defense purposes which has all of its storage of the high-speed type. High speed storage becomes important only when the total time of carrying out operations is critically dependent upon the speed of storage access. It should be noted that if an information processing system uses a single arithmetic element as the processing link, the amount of high-speed storage need be no greater than two relatively small blocks, one of which is being filled from slower storage mediums while the other is being operated upon by the single arithmetic element. For the limiting case, there need be only two registers of high-speed access; the computer then extracts the information from one of these registers and proceeds to carry out some operation on the information for a period of X μsecs; at the same time, the second register is being supplied information from a slow-speed storage device which can have an access time up to the full X μsecs. (This is identical with a storage overlap scheme.)

A drum storage system appears to have several desirable features which might suggest it as the slow-speed storage device for use with such a system as the one above:

1. Information can be transferred in and out of drum storage at the relatively high-speed of 8 μsecs per transfer; this speed is higher than the average operation time of a WW I order, even assuming a zero access time to high speed storage;

2. A large amount of storage (about 1/4 million binary digits) is available on the drum in a relatively compact and cheap form;

3. The number of drum reading and writing circuits need not be any greater than the number of digits in a stored word; these circuits are switched by crystal gates or other means to various fields of the drum while a single comparison device can be used to locate a particular position around the periphery of the drum; selection and control equipment is thus held to a minimum;

4. By means of special heads on the drum, there is the possibility of simultaneously reading and writing in storage, although at different register positions;

5. A scanning action of storage is obtained for almost nothing (which is not true of other storage systems); this scanning action should prove very useful when a large amount of similar data is stored and pieces with identical characteristics are desired.

It should be noted that drum storage is not being stressed as the cure-all of the storage problem. By itself, drum storage would probably prove too slow for the Air Defense problem. However, in conjunction with a limited amount of high-speed storage, a drum storage system provides a large amount of storage capacity in a compact and reliable form. In evaluating such a hybrid storage system, consideration should be given to the possibility of an added complexity resulting from the use of two different storage mediums. Such consideration has been ignored in the above.

Signed B. E. Morriss
B. E. Morriss

Approved JWF
Jay W. Forrester

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