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SUBJECT: **DELTA$_{ns}$ IN CERAMIC ARRAY #1**

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Abstract: It is possible to obtain two values of output voltage from a half-selected memory core depending on whether it holds a ONE or a ZERO. This fact places a limit on the size of a memory plane or, more specifically, the number of cores on one sensing winding which may be half-selected during a read operation.

Consider the memory core hysteresis loop shown in Figure 1. I_m is the magnetizing current required to switch the core. $I_m/2$ is the magnetizing current to which the core is subjected while switching another memory core in its row or column. ϕ_1 and ϕ_0 are the flux states arbitrarily considered to be a disturbed ONE and a disturbed ZERO respectively. If a current of $I_m/2$ is applied to the core while it holds a ONE, a flux change of NS_1 (non-selected ONE) is produced. If, instead, the same current is applied while the core holds a ZERO, a different flux change, NS_0 (non-selected ZERO) is produced. The difference, $NS_1 - NS_0$, has been named δ_{ns}.

Figure 2 shows the sensing winding geometry for Ceramic Array #1. Note that the sensing winding links every core in the memory plane. Note, also, the plus and minus signs associated with each core. These refer to the polarity of output voltage induced in the sensing winding when a core is fully or partially switched by the application of coordinate driving currents in the directions indicated by the arrows at the ends of the driving lines. Since there are equal numbers of positive and negative outputs on each coordinate line almost complete cancellation of the half-selecting signals results. (One of the outputs is from the selected core).

Figure 3a shows two selected coordinate lines of memory cores in a 16 x 16 array. The plus and minus signs indicate the polarity of voltages induced in the sensing winding with the application of $I_m/2$ (Figure 1) in the positive direction in each coordinate driving line. Note that the selected core receives the full switching durrent while the other thirty cores receive but half switching current. However, since the sensing winding links all the cores, the thirty half-selected core outputs add to or subtract from the selected core output depending on their polarities. If all the half-selected outputs were equal in magnitude then two cases would result:

a. Selected core output positive

b. Selected core output negative

For (a) the net output becomes,

+ selected core output + 14NS - 16NS = + selected core output - 2NS.

For (b) the net output becomes,

- selected core output + 16NS - 14NS = - selected core output - 2NS.

The 2NS terms may be ignored temporarily as not significantly affecting array size. Since it has been shown that half-selecting a core which holds a ONE results in a larger output than half-selecting a core which holds a ZERO, it can be seen that there exists two "worst patterns" and two "best patterns" for a given pair of coordinate lines. Examples of these are shown in Figures 3a, 3b, 4a and 4b.

Suppose that the selected core in Figure 3a contains a ONE. Reading this core results in a negative output signal on the sensing winding. To construct a "worst pattern", the net half-selecting signal from the thirty half-selected cores must be positive in order to subtract from the negative ONE. This means that those cores which will contribute positive half-selecting signals must contain ONES and those cores which will contribute negative half-selecting signals must contain ZEROS. This condition will yield the largest net difference, the sum of all the δ_{ns}, which will be called Δ_{ns}.

Suppose again that the selected core in Figure 3b contained a ZERO. Reading this core would result in a negative output signal on the sensing winding. To construct a "worst case", the net half-selecting signal from the thirty half-selected cores must be negative in order to add to the negative ZERO. This means that those cores which contribute negative half-selecting signals must contain ONES and those cores which contribute positive half-selecting signals must contain ZEROS. Thus it is seen that a ONE can be made smaller and a ZERO larger by the contribution of Δ_{ns} to the net sensing winding output.

Conversely, Δ_{ns} can in some instances be of such value as to make the ONES larger and the ZEROS smaller resulting in a "best pattern" or one which gives the largest "ONE-ZERO" ratio. This situation results from patterns shown in Figures 4a and 4b.

For any array, the worst conditions exist for a ONE output signal when the net output is composed as follows:

$$\text{ONE} - (n - 2)\ \delta_{ns} - 2NS_1$$

where n = number of cores on a coordinate line.

The worst condition for a ZERO exists when the output consists of:

$$\text{ZERO} + (n - 2)\ \delta_{ns} - 2NS_0.$$

Furthermore, since the amplitude of an NS_1 is greatest on a core which holds an undisturbed ONE, and is lower and relatively constant after that, it is possible to get a large δ^1_{ns} which can be defined as:

$$\delta^1_{ns} \equiv NS_1 \text{ (undisturbed)} - NS_0.$$

For 2- to -1 selection in a memory plane, there may exist two undisturbed ONES ready to contribute to the above effect and the worst conditions may become:

$$\text{ONE} - 2\delta^1_{ns} - (n - 4)\ \delta\ -2NS_1$$

$$\text{ZERO} + 2\delta^1_{ns} + (n - 4)\ \delta\ -2NS_0$$

The NS signals from fourteen cores in Ceramic Array #1 were recorded photographically during normal operation while they held the "worst pattern". The results yielded an average δ_{ns} of two millivolts.

Measurement of δ_{ns} on seven individual cores by first half-selecting the core while it contained a ZERO and then while it contained a ONE gave an average δ_{ns} of about 2 1/2 millivolts.

Another measurement of delta was obtained by putting a "worst pattern" into the entire array. In this case all cores with outputs of positive polarity held ONES and all cores with outputs of negative polarity held ZEROS. With the pattern inserted, all excitation was removed except a half-selecting current on a winding which linked every core (Z-plane winding). The sensing winding output voltage then consisted solely of δ_{ns} from 128 pairs of cores. This value, therefore, is approximately the same as would be generated by a 128 x 128 array using 2:1 selection. This total Δ_{ns} was 130 millivolts or a δ_{ns} of approximately one millivolt.

These values may be compared to the following signal values:

Normal operation of the 16 x 16 Ceramic Array #1 gives peak-amplitude of ONE-ZERO ratios of 4:1 with ONES of approximately 250 millivolts and ZEROS of approximately 60 millivolts.

An average value for a disturbed NS_1 signal (over 30 cores) is 25 millivolts and for a disturbed NS_0 signal is 23 millivolts.

The "first NS_1 can be as much as ten times greater than a "second" or "third" NS_1 signal.

Documented photographic records of these data on the "delta problem" for Ceramic Array #1 are in Notebook #4 (3/28/52) on pp. 117-120, 125-136 and in Notebook #5 (6/30/52) on pp. 102-108, 123-124, of E. A. Guditz.

Signed Elio A. Guditz
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EAG:jmm

Drawing attached:
A-51628 Figure 2

$$NS_1 > NS_0$$

$$\delta_{ns} \equiv NS_1 - NS_0$$

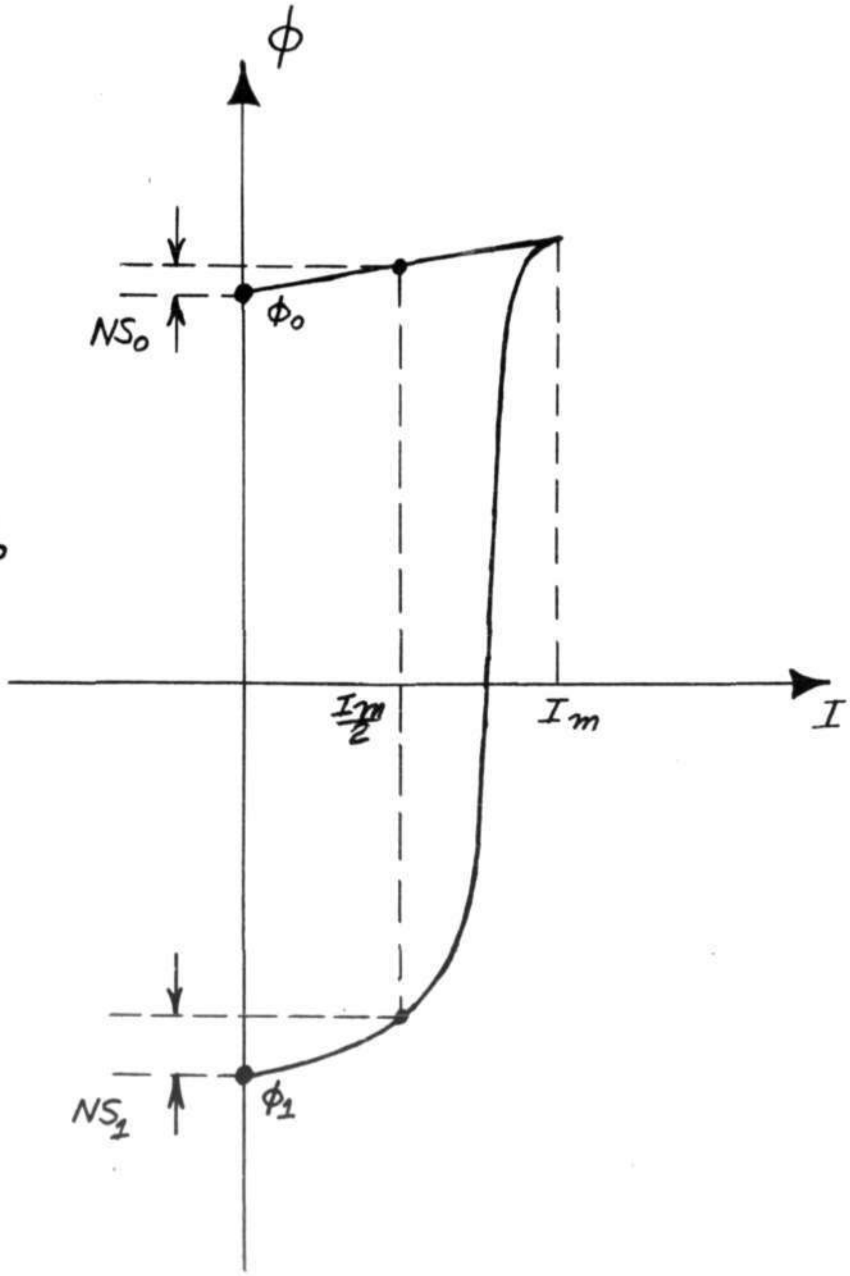

Fig. 1

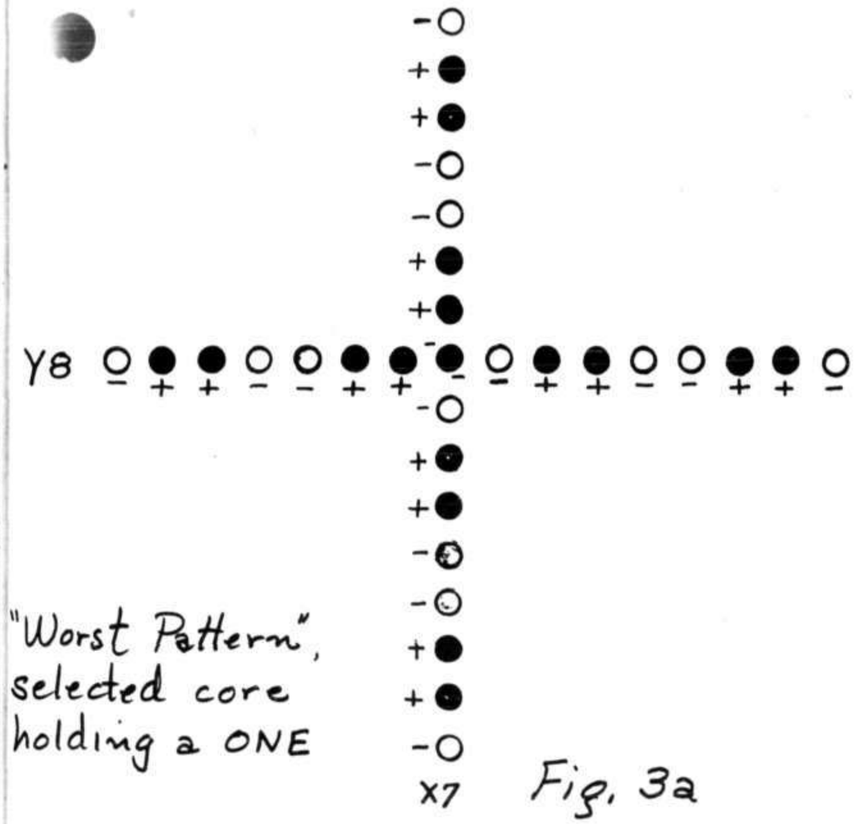

Fig. 3a

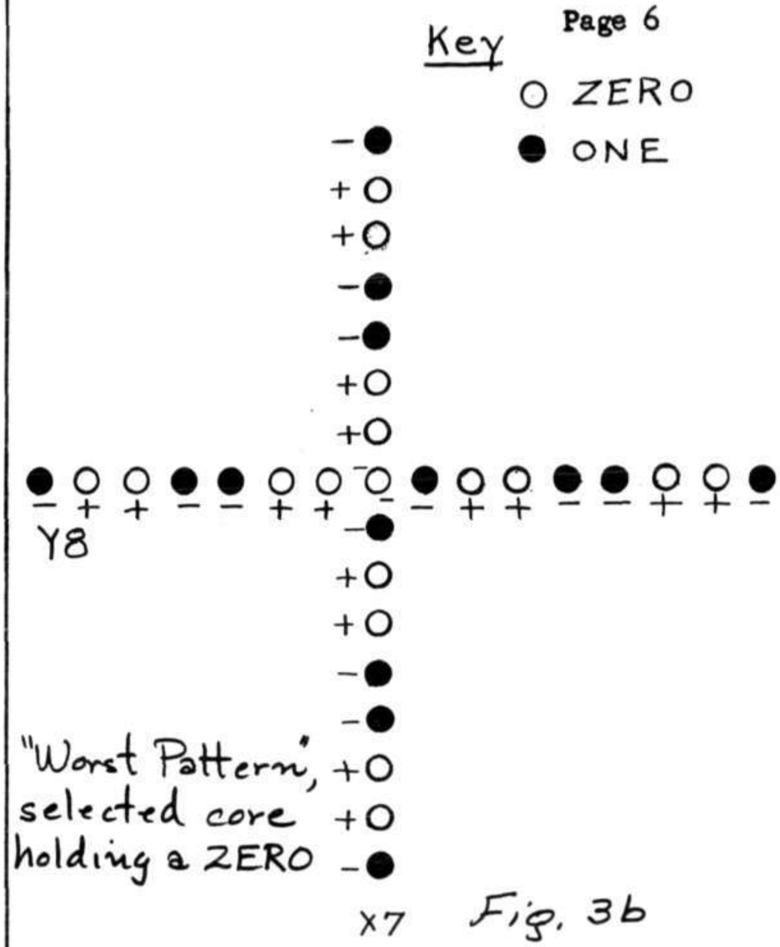

Fig. 3b

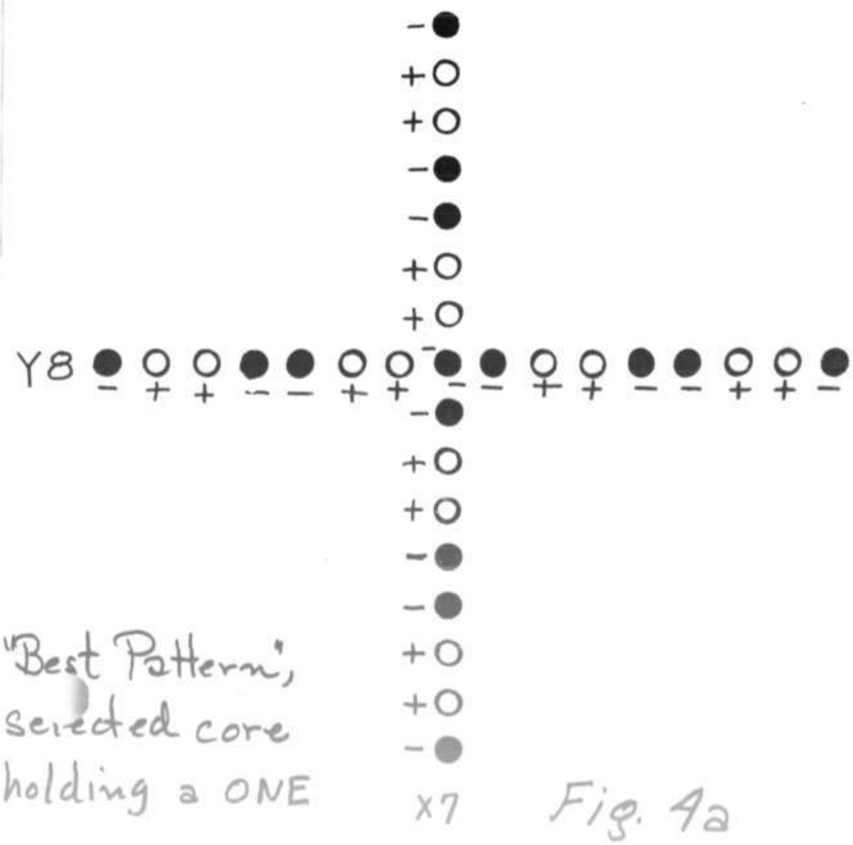

Fig. 4a

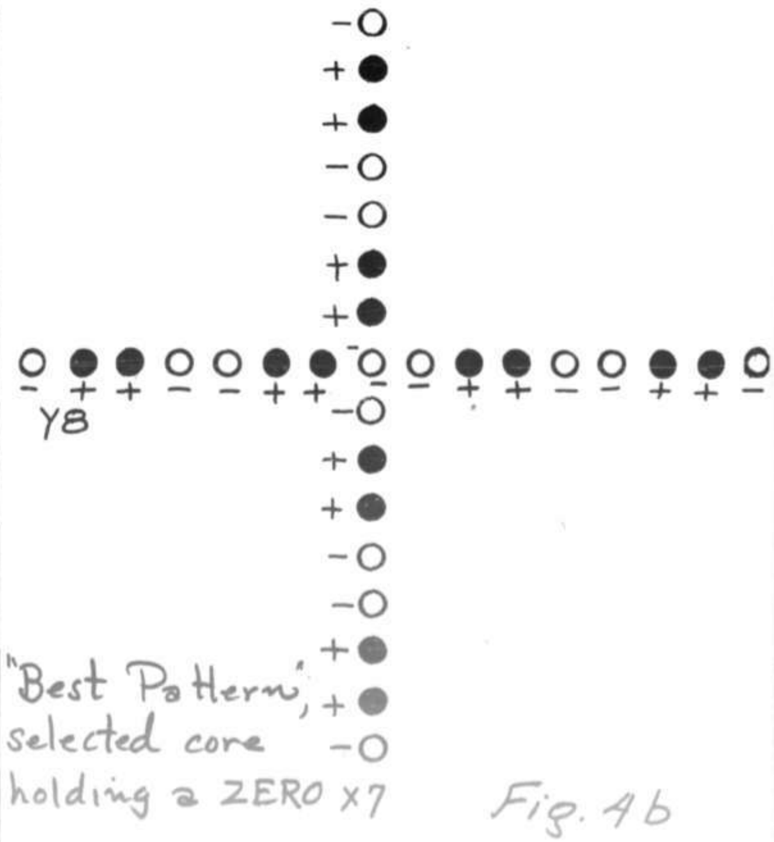

Fig. 4b

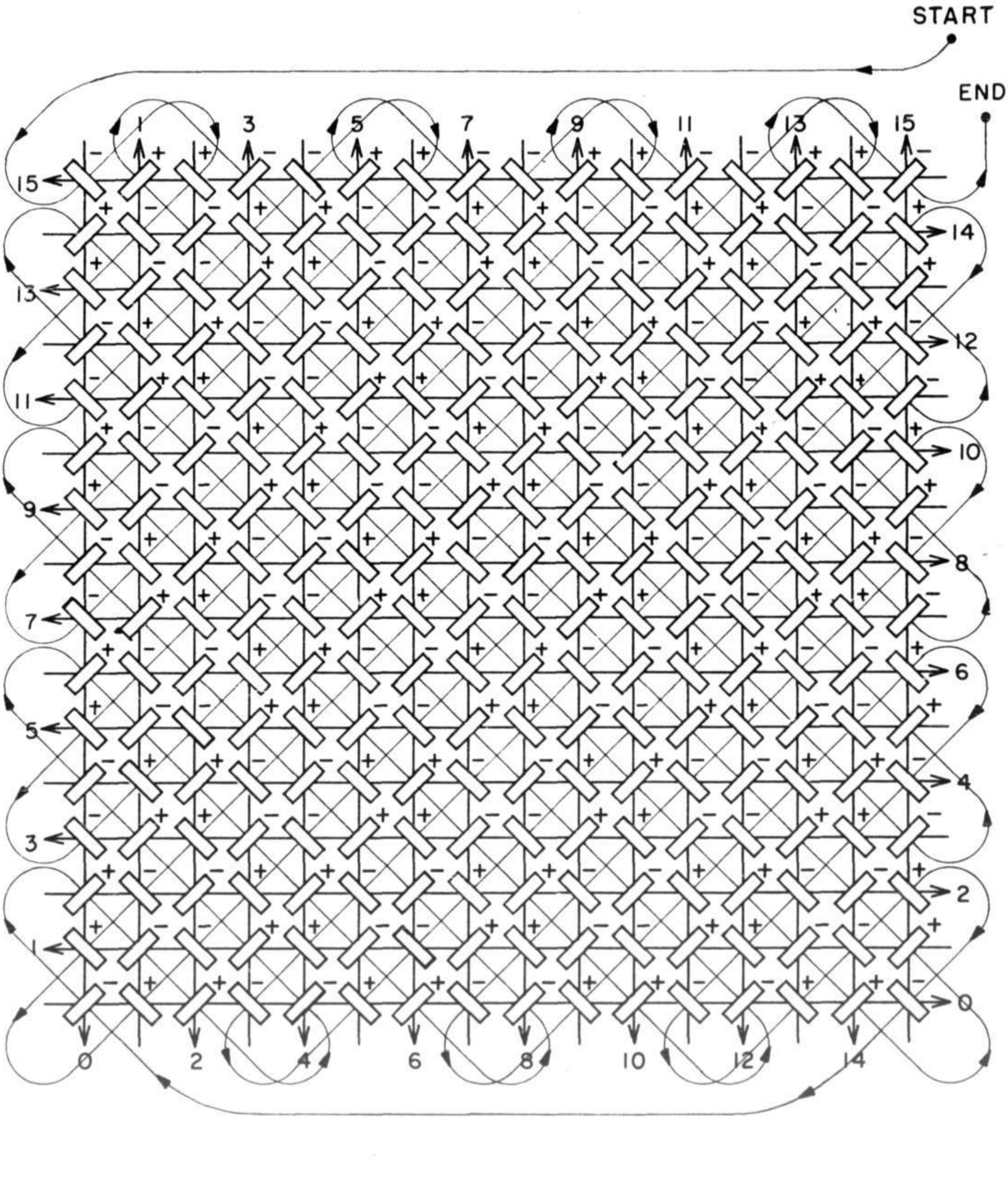

FIG. 2
WINDING GEOMETRY–CERAMIC ARRAY #1

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