

6345
Memorandum M-185

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Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BI-WEEKLY REPORT, PART I, DECEMBER 15, 1947
To: 6345 Engineers
From: Jay W. Forrester
Date: December 15, 1947

1.0 WHIRLWIND I COMPUTER ELEMENTS

1.1 Listed by Block Diagram Number

101 Master Clock

(H. Kenosian) Final specifications for the Master Clock are now being drawn up. Preliminary construction will begin as soon as final specifications are complete.

102 Program Counter

(D. R. Brown) Circuit schematic has been revised and can now be turned over to Sylvania to be redrawn for prototype construction. I don't know what has been done with the preliminary digit which was constructed by Sylvania.

103 Program Register

(D. R. Brown) The circuit schematic has been revised and delivered to Sylvania. Evidently they have redrawn the circuit schematic and made a prototype layout. We have a print of the layout but none of the circuit schematic.

104 Control Switch

(J. A. O'Brien) Tentative plans have been completed with Sylvania engineers for a proposal to build a model of the Control Switch for WWI. The data that is needed for a complete circuit is available and needs only to be put together and drawn. In line with this work, the present 32-position switch has been loaned to Sylvania to allow their engineers to become familiar with its operation. Slavin and Flaherty will design prototype.

105 Operation Matrix

(H. Fahnestock) Sylvania engineers Flaherty and Slavin are familiarizing themselves with J. A. O'Brien's preliminary work and proceeding to prototype design.

106 Time Pulse Distributor

(H. Fahnestock) A time pulse distributor has been built by Sylvania and is being rebuilt to better conform with the rest of WWI.

107 Operation Timing Matrix

(H. Fahnestock) Sylvania engineers Flaherty and Slavin are familiarizing themselves with J. A. O'Brien's preliminary work and proceeding to design of prototype.

108 Program Timing Matrix

(H. Fahnestock) Sylvania engineers Flaherty and Slavin are familiarizing themselves with J. A. O'Brien's preliminary work and proceeding to design of prototype.

201 Storage Switch

(H. Fahnestock) Much of the work being done under 104 can be applied to this. More details still to be worked out.

202 Toggle Switch Storage

(J. A. O'Brien) I have constructed two registers of toggle switch storage and have observed their operation using a 32-position switch. The principle difficulties in the way of perfection are the transmission and deshaping of switching transients that appear on the switch output.

Present tests indicate that these transients can be made unobjectionable and the storage set-up time be made less than one microsecond by using 6L6 amplifiers between the switching matrix and the storage digit tubes.

203 Flip-flop Storage

(D. R. Brown) The circuit schematics of flip-flop storage are being revised. They will be delivered to Sylvania next week. Sylvania will then make prototype layouts. The preliminary flip-flop storage rack constructed by Sylvania has been tested qualitatively. It can clear, read-in, and read-out at one-microsecond intervals. Sylvania has insufficient ability and test equipment to make quantitative measurements. J. A. O'Brien and I spent this morning working with Sylvania on this testing job. Much more time than this will be necessary before any measurements can be made.

300 Arithmetic Control

(G. C. Sumner) The arithmetic element control block schematic diagram has been completed except for recent changes in ACO made by the block diagram group. Schematic diagrams are underway for separate panels of arithmetic control. The past week has been spent in collecting problems involving the ACO carry register in arithmetic check and special add. This was found necessary for the design of ACO carry and special add memory, because time sequence is very critical. This work was carried on in connection with timing studies being made by the block diagram group. A problem was found that required farther propagation of carrier than problems being used in timing studies by block diagram group. A review of all functions of ACO carry will be issued in an E-series report.

301 A-Register

(C. W. Watt)

- A. An effort has been made to obtain correct and up-to-date schematics for the A-register, and to make preliminary layouts for the actual panels for WWI.
- B. A block schematic for the A-register has been completed, #B-31211.
A circuit schematic is nearly completed. This is #D-31276.
A preliminary layout has been made and submitted to us by Sylvania. Correction of this awaits completion of the schematic.
- C. As soon as the schematic is finished, the proposed layout will be checked and changed. When a satisfactory layout is achieved, Sylvania will make one preliminary model.
- D. Delays have been due to:
 - 1. Indecision on circuit component values.
 - 2. Indecision on bus driver methods.
 - 3. Other activities of mine, among which are drafting procedures, standard practice and methods reports, etc.(Nos. 1 and 3 are pretty well resolved now. No. 2 remains undecided.)

302 Accumulator

(J. J. O'Brien) Flip-flop Buffers to Drive the Accumulator Shift and Carry Matrix:

- A. Investigations of the type of buffer that could be used were made. Improvements in the operation of the present accumulator buffers were attempted.
- B. With a matrix switch the present type of buffer must be used. Some improvement in their operation has been gained.

- C. The question of drawing the matrix has been dropped to investigate a whiffle tree switch to replace the matrix.
- D. Because the buffer must be d-c coupled to the matrix, the dissipation ratings of the 1N34 crystals limits the design. This circuit has shown itself sensitive to tube characteristics in the multiplier.

Whiffle Tree Switch for Shift and Carry:

- A. The switch has been designed and constructed. Tests and improvements are being made on it.
- B. The switch works satisfactorily so far at low frequency inputs.
- C. The testing under all specifications will be made.
- D. --
- E. An E-series report will be issued.

(C. W. Watt)

- A. A complete layout of the accumulator for WWI is being made by Walter Cook in drafting. This has progressed well, but is now held up by lack of certain information (see below).
- B. A schematic for the accumulator is being made, #R-31275. A block schematic has been finished, D-31213.
- C. As soon as the schematic is finished, the layout will be changed to agree in detail, and an effort will be made to have a model built here that will be as excellent as it is possible to make. All detail mechanical specifications that we have set up will be followed to the letter, and the model will serve, it is hoped, as a definite prototype of the accumulator, and a model of construction for the other panels of WWI.
- D. Delays in the completion of this project are due to:
 1. Lack of a final decision on the use of the shifting matrix switch versus the whiffle tree switch.
 2. The incomplete schematic.

303 B-Register

(C. W. Watt)

- A. An effort is being made to obtain a correct and up-to-date schematic for the B-register, and to obtain a preliminary layout.
- B. A block schematic for the B-register has been completed, #B-31212. A circuit schematic is being drawn by Sylvania, based on a rough penciled schematic I gave them. It has not yet been received here. Its number will be D-31277. Two preliminary layouts have been made by Sylvania and submitted to us. They have not been approved because of lack of up-to-date circuit information.
- C. As soon as the schematic is finished completely, the layouts will be revised to agree, and Sylvania will build a preliminary model.

- C. Investigation of the implications of these new ideas is proceeding. Power studies remain to be done in detail and must soon be done, because rotary machinery must be ordered soon.

1.23 Video Cabling

(C. W. Watt)

- A. Decisions have recently been made on the types of video connectors to use in WWI cabling.
- B. It has been decided to use:
 - 1. The removable type of video tee connector, UG-274/U, for connecting branch circuits to main cables. This permits complicated cables to be made up in small sections and assembled into larger combinations at installation.
 - 2. A modification of the present method of shield braid clamping in all of the RNC type connectors. A supply of the extra parts needed to modify connectors on hand has been ordered. John Ely has been doing this work.
- C. Sample connectors have been obtained from Industrial Products Corp. and from Waltham Horological Co., both unmodified.
- C. Modified samples of connectors will be obtained from the above companies.
- D. No detailed work can be done on specific cables for some time, but must await panel design, rack arrangement decisions, etc.

1.3 Auxiliary Equipment

1.31 Power Supplies

(H. Fahnestock) Received "Preliminary Power Consumption Estimate, December 8" by Anderson of Sylvania. Desirable for him to carry this further by summarizing current required at various voltages and write specs for generators based on equipment available. Close cooperation must be maintained with C. W. Watt (see 1.21 above).

1.32 Air Conditioning

(H. Fahnestock) Conference December 12, Forrester, Fahnestock, Watt, Boyd, Wainwright. Duct location along ends of racks on top instead of under floor should be investigated. Dumping air needs further consideration to save return ducts. Proposal received from Carrier.

(H. R. Boyd) Discussed airconditioning with Bohm and Wainwright. Suggest that a 5000 pound unit can be placed on an angle-frame resting on the floor with the unit about 10 feet above in the front of the boiler room.

(W. C. Bohm) Based on the results of conferences which were held to discuss this subject, the Carrier Corp. has now submitted a proposal for air conditioning WWI. Although their present specification is for a total dissipation of 49.5 K.W., it appears that a relatively minor change in the size of one of the compressor units will permit the capacity to be raised to approximately 60 K.W. An M-series memo giving further details on this subject as a whole, has just been written and is entitled, "Air Conditioning for WWI," dated December 12, 1947.

1.4 Unclassified.

Test Specifications.

(N. Taylor) Soon after circuits are "frozen" Sylvania will need "Test Specification" on each of the units 101 to 601. These specifications are being formulated along the lines used to test and specify "Multiplier test Specs" but will be much more complete. It is planned that the test specs in the ACC, A & B Rg. be established by February 1, 1948. The others will follow shortly thereafter.

Standard Circuits

(J. A. O'Brien) A system is being set up to standardize all of the basic circuits in the computer. This is treated in detail in engineering note E-80. The principle difficulties are that some proposed circuits have not yet been developed. For this reason some of the circuits have not been published as yet.

Mechanical and Other Specifications for WWI.

(C. W. Watt)

A. A proposal for mechanical and wiring specifications has been written, and will be issued by Fahnestock as E-79.

A proposal for standard circuits has been made and will be issued by J. A. O'Brien as E-80.

B. The need for such specs has been established; and the work done, while preliminary, will serve as a good beginning to a complete set of mechanical and electrical specs for WWI.

C. New specs, as needed, will be written and issued. Brown and Taylor will write video specs.

D. Delays and difficulties are merely those of getting time to do writing of specs, and obtaining general agreement from all concerned. The new policy coordination between M.I.T. and Sylvania should help things greatly.

2.0 WHIRLWIND I RESEARCH

2.1 Circuits

(N. Taylor) Several Circuits are being studied in order to "freeze" circuit schematics at the earliest possible date.

These are:

1. "Waffle Tree" gate chain for use in the Accumulator.
2. Multiple mixing of pulses in a single channel for use in "Acc."
3. Multiple mixing of signals for resetting a flip-flop.
4. Multiple mixing of signals for the new bus driver method.
5. Work on the ac coupled flip-flop will continue on an expanded scale to aid in the decision of using it in WWI.
6. A special transformer to give both a positive and negative pulse simultaneously is under consideration by transformer group. If it is possible to do this, it will save tubes in arithmetic control and in several other panels.

2.11 Flip-Flop Design and Stability

(H. Fahnstock) AC coupled flip-flop looks promising for WWI. It is less affected by component tolerances than DC coupled FF. Necessary to test into actual loads and to have various people build and use AC coupled FF to gain experience.

(A. B. Horton, Jr.)

A. Nature of Present Work:

Work is at present in progress on the analysis and design of a capacitively-coupled (a-c) flip-flop, results of which are to be submitted to M.I.T. as a master's thesis report.

A breadboard model has been constructed and set into operation in the laboratory. At present, extensive work is being done on a mathematical analysis of the operation of the circuit. This mathematical analysis has been broken into two major portions, the first being an analysis of the switching transient and the second an analysis of the circuit behavior between switches. As this analysis progresses, correlation of day-by-day results is being made with experimental results obtained on the breadboard model. The analysis includes the effect of all circuit parameters, including interelectrode and wiring capacitances.

B. Results of Greatest Interest:

Experimental

Switching time, Unloaded:

Off-going	≈	0.14 μsec
On-going	≈	0.08 μsec

Switching Time, Loaded on each plate with 33 muf to ground:

Off-going \approx 0.15 μ sec.

On-going \approx 0.1 μ sec.

Minimum required trigger amplitude - 16 volts.

Parameter tolerances not critical.

Natural free-running half-period greater than 30 μ sec.

Analytical

Results obtained so far check well with experimental results.

C. Future Plans:

The present breadboard model, being the first, is by no means to be considered as optimum. When the analytical work is completed, a study will be made of the results with the view of determining those parameters and characteristics which have a major influence on the switching and interswitching behavior of the circuit. In this way, it is hoped that the flip-flop operation will be improved. A design procedure will be devised. An improved method of triggering the circuit should be studied. Finally, extensive testing of the circuit under actual operating conditions should be carried out.

D. Difficulties and Delays:

The procedure of carrying out numerical calculations from the mathematical analysis is long and tedious, especially in the switching analysis because of the complexity of the equations. In addition, the analysis of the circuit behavior in the interval between switches must be done on a point-by-point basis, thereby increasing the time required to obtain numerical results.

E. More Detailed Write-Ups.

Master's Thesis Proposal

Thesis Progress Reports 1 and 2.

Progress Report 3 will be issued soon.

2.12 Clamping Methods

(N. L. Daggett) Present work concerns reduction of undesired pip on flip-flop waveform in order to reduce clamping difficulties. Work is discussed in E-81.

(D. R. Brown) It is desired to increase the interval between pairs of restorer pulses so that long operations such as division can be performed without interruption. This could be done by increasing the coupling capacitor but might distort waveforms. It has been shown that it can be increased to .001 MFD or even .01 MFD without any harmful effects. A decision will be made on the basis of available capacitors and computer requirements.

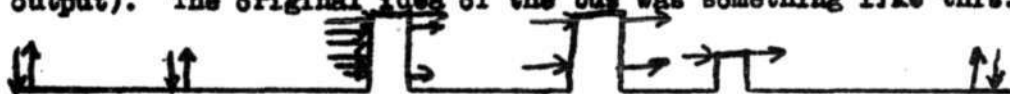
(J. A. O'Brien) Some concern has been expressed about the load added to a flip-flop by the condenser in the flip-flop AC coupling circuits. D.R. Brown and I arrived at the conclusion that the charge that the flip-flop must replace on the coupling condenser during the restorer operation is $q = EC(1 - e^{-\frac{t}{RC}})$ where t is the time between restorer operations, and E is the net voltage forcing the discharge. The effect of varying the size of the coupling capacitors is negligible if $\frac{t}{RC}$ remains less than 0.1.

2.13 Bus Drivers

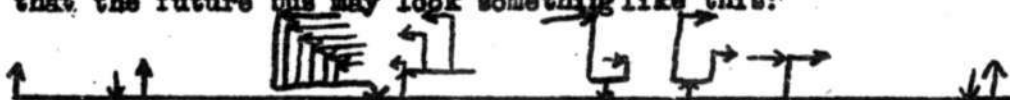
(C. A. Rowland)

At present I am working on the digital transfer bus and line driver for the bus.

Using one continuous bus of about 80 feet in length, voltages in the range of 15 to 18 volts were obtained on the bus using a 6Y6 driven by an SR 1030. Reflections at worst were on the order of 3 or 4 volts. (It takes a 4 or 5 volt signal into the SR 1030's biased at -15 before any signal appears on the output). The original idea of the bus was something like this:



The present plan is to mix several signals into one buffer so that the future bus may look something like this:



This will reduce the number of drivers that are needed and will shorten the bus. Results so far indicate that six signals can be mixed into one grid. It seems that the measured plate dissipation of a 6Y6 is about 75% greater than expected from the characteristic charts. This may mean another buffer between the SR-1030 and the 6Y6.

2.15 Restorer Operation without Trigger Tube.

(J.J.O'Brien)

- A. The flip-flop life test rack was operated for 163 hours without trigger tubes. Noise was introduced on the common cathode line by setting and resetting three flip-flops at one megacycle prf.
- B. No recorded error occurred in the 163 hour period.
- C. Move the rack to Barta Building as soon as possible.
- D. The present equipment for photographing waveforms is unsatisfactory.
- E. M-138. A Memorandum, "Flip-flop Life Test Rack, Run No. 3" which is in preparation.

2.16 Gate Generator

(J. A. O'Brien)

A gate generator made up of a flip-flop and a delay line and followed by a 6Y6 cathode follower has been constructed.

It will put out a $\frac{1}{2}$ microsecond gate with 0.2 microsecond rise time and an amplitude of 14 volts into a 100 ohm terminated line.

It is planned to modify the circuit by putting a transformer in the plate circuit of the 6Y6 making it an amplifier. This may increase the output voltage, but will most likely increase the rise time.

One difficulty with the flip-flop type gate generator is that it has to be cleared in order to insure its being in the proper position; for this reason a gate generator using a blocking oscillator will be built and tested. It is expected that some difficulty may be encountered in reducing the resolution time of the blocking oscillator.

2.2 Components

2.22 Pulse Transformers

(G. G. Hoberg)

1. From estimates by J. A. O'Brien, D. Brown, and C. Watt, it was concluded that about 1600 pulse transformers would be required for WWI.
2. Since only about 400 hypersil transformer cores are currently in stock, it is suggested that 1500 more be ordered from Westinghouse as soon as the Navy approves the order.
3. Specifications for these hypersil cores were written up and submitted to H. Morley.
4. Two pulse transformer types, NE362(1:1) and NE363(3:1), are appropriate for most WWI applications. They have been proved satisfactory; no design changes are foreseen. Formal specifications were written up and submitted to H. Morley.
5. I am aware of only two WWI applications which may require transformer types other than the two mentioned.
 - a. A higher turns ratio may have to be used for the control-line-driver circuit.
 - b. Longer windings may be required if transformers are used in circuits which handle long gate pulses. A transformer suitable for (a.) has already been designed. Difficulty with (b.) will be encountered only if gate-pulse lengths are greater than 0.5 microseconds. Circuits in both cases are still tentative.

2.23 SR-1030 Tests and Specifications

(D. R. Brown) On December 2, Emporium telephoned us average data on results of control run of 100 SR-1030's. This included two types: C-5104, C-5245. We selected C-5245 on the basis of the data. Since that time Emporium has done nothing because of a misunderstanding between Boston and Emporium. We did receive fifty C-5245's, but no specs. Rochester called Emporium December 9 and got the ball rolling again. We are to receive specs on which we can order this week.

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2.4 Unclassified

Crystal Rectifiers

(D. R. Brown) A meeting with the Sylvania crystal-rectifier group to discuss crystal reliability was held November 21. Data indicate that crystal-rectifiers do deteriorate, but it is difficult to ascertain just how rapidly. Heins said they have as good life as vacuum tube, maybe better. A meeting between BuStandards, Sylvania and Whirlwind will be held in the near future to review all crystal-rectifier-life data.

High-Conductivity Crystal Rectifiers

(D. R. Brown) Sylvania is making thirty high-conductivity crystal rectifiers (Sylvania No. D344) for laboratory work on bus system. The laboratory work will be done here by Mr. Rowland. The crystals will be delivered early next week.

Life tests of high-conductivity crystals at elevated temperatures continue. New life tests at 35-40° C. have been started recently.

(E. W. Sard) The relative amounts of power in periodic pulses of the following shapes were computed.

- a. Rectangular
- b. Half-sinusoidal.
- c. Top of a sinusoid (less than half)
- d. Triangular
- e. Parabolic

One result was that less than 7% error is made if the power is computed on the basis of the shape of the pulse being half-sinusoidal, when in fact it may be the top of a sinusoid.

3.0 SPECIAL CIRCUITS

3.1 Five-Digit Multiplier

(N. H. Taylor) A memorandum will soon be issued covering the "Present Achievement and Future Plans of the Five-Digit Multiplier." It covers the following points:

1. Present Achievement
 - a. Successful operation at 2 MC pxf for 500 hours.
2. Future Plans
 - a. New power supply
 - b. Repetitive solution of problems
 - c. Crystal clock
 - d. Control to "add" as well as "multiply."
 - e. Life test (methods, aims, procedures)

(H. L. Ziegler) At the present time, the multiplier is being kept in continuous operation on a 24-hour basis in order to obtain data on component life and variation in the characteristics of the component during its lifetime.

When the filament power alone was kept on overnight as was done at the beginning of these tests, the flip-flops, in the morning showed a tendency to "stick" in one position when the plate and grid voltages were applied. Though the flip-flops in all cases were being restored and could be set to either position, they would automatically return to the "sticking" position. In general, these flip-flops were restored to normal operation by being triggered at a two megacycle rate for a period of a few minutes.

With all voltages on continuously, this "sticking" was much less common and those that did stick were more easily cleared.

Investigation has shown that the "sticking" tendency is reversed if the positions of the two flip-flop tubes are reversed. Testing of the tubes in question usually shows considerable difference in their characteristics, particularly in plate currents. The "sticking" is probably due to failure of one tube to cutoff completely and work is being done to make the present flip-flop circuit less critical of tube unbalance.

The effect of triggering at a high rate has not as yet been explained and is being investigated at the present time.

3.2 Test Equipment

(J. W. Forrester) All persons interested in test equipment are urged to comment on proposed standard test equipment program. No units can be considered standard test equipment until specifications have been agreed upon.

(W. Taylor) Several new panels are under development principally to be used with the "five-stage multiplier" but basically intended to expand our line of Standard Test Equipment.

1. Variable Frequency Pulse Distributor.
This unit will provide pulses at variable frequency from 1 to 5 MC (lower if desired) and on an adjacent line restorer pulses. The latter will occur at fixed time intervals and will not vary in frequency, that is one microsecond between pulse will be maintained. In addition, the variable frequency pulses will be gated out during the restoring period. This panel should prove of wide use as a test unit. Perhaps Sylvania should have a few to test panels at higher prf's than end use requirements.
2. Crystal Clock for use in Multiplier is being tested in breadboard stage.
3. Frequency Divider to replace the G.E. counter is being constructed. NOTE: The G.E. counters are subject to jitter and are unstable after long runs.
4. A pulse distributor to run the multiplier repetitively is under construction.

3.21 Standard Test Equipment

(J. O. Ely)

- A. Present Work — attempting to design:
 1. Pulse-shaping amplifier for 0.1 μ sec. pulses at 30-50 v amplitude on 93 ohm line.
 2. Calibrated delay multivibrator for delay range 0.5 - 5000 μ sec.
- B. Results:
 1. First blocking-oscillator type pulse-shaper unsuccessful. Will not work at all well below 0.3 μ sec.
 2. First model delay m-v not yet breadboarded.
- C. Will revise proposal for standard test equipment system as soon as replies to E-78 are in.
- D. No replies on E-78.
- E. E-78, M-173, M-177.

3.22 Special Test Equipment

(D. J. Crawford) Model 2 Crystal Tester. Except for the receipt of the modified meter, the Model 2 Crystal Tester has been completed. This new tester operates on the same principle as the previous model, but contains an improved voltmeter circuit with a stabilized power supply and has an additional voltage range suitable for testing type IN38 crystal diodes. A complete description will be contained in E-84 which will be published soon.

(J. J. O'Brien)

Low Frequency Five-Stage Binary Counter with Trigger Phase Control
(Work in association with H. Kenosian)

- A. The design, construction and test of the five-binary stages has been completed. A slight adjustment of one stage is being made. The trigger phasing circuits are under construction.
- B. --
- C. The unit will be given final testing, packaged and installed in the Demonstration Multiplier.
- D. --
- E. An E-series report will describe the unit.

Life Data of the Demonstration Multiplier:

- A. A system of recording the life data of the Demonstration Multiplier is being set up.
- B. --
- C. --
- D. --
- E. E-83, covering this subject will be published shortly.

(R. H. Murch)

I am designing and constructing a rock power control unit, which can be used to control the D.C. and A.C. power to a test rack.

This unit will include:

- 1. D.C. control circuit for standard D.C. voltages.
 - a. Master switch.
 - b. Pilot light for each voltage.
 - c. Fuse for each voltage (any value of fuse up to 3 amps may be used).
 - d. Four 12-pin Jones Plugs outputs.
 - e. Two Jones strip outputs.
- 2. A. C. control circuit:
 - a. Twelve amp circuit breaker
 - b. Ten amp variac.
 - c. Meter to measure line and variac voltage
 - d. Two 40 amp filament transformers controlled by variac. One will feed the Jones plugs and the other the Jones strips.
 - e. Six A.C. outlets, three on variac and three direct from line.

The prototype is under construction now.

(H. Kenosian) Further details on the test equipment program and detailed specifications of equipment to be described will appear in a memorandum now being typed in rough draft form.

I. Master Clock for Demonstration Multiplier:

The master crystal controlled unit to be installed permanently in the Demonstration Multiplier is now being tested in breadboard form. The final model will be constructed as soon as breadboard tests have been completed.

II. Binary Frequency Divider 2:1 - 4:1.

The prototype and all drawings have been completed. Parts lists are being drawn up and photographs are to be made. The unit will be used for general laboratory testing for frequencies up to 6.2 M.C. The standard flip-flop used in the first divider circuit will trigger above 6 M.C. Three more will be built and an E-series note is now being typed in rough draft form.

III. Variable Delay Pulse and Gate Generator:

Breadboard testing has been completed and prototype is under construction. Unit will be used to test the resolving power and amplitude sensitivity of basic sections of WWI.

IV. Single Pulse Synchronizer:

Will be used to obtain standard $0.1 \mu s$ low frequency pulses. Will replace the Gas Tube Pulse Generator and will be used to adjust push-button phasing on the control panel of the Demonstration Multiplier and Restorer Pulse Generator. The prototype has been completed and three more models are very nearly finished.

V. Variable Frequency Clock-Restorer Pulse Distributor:

This unit will be used to test the effect of prf variation on and to determine the upper frequency limit of the Demonstration Multiplier and WWI.

VI. Low Frequency Five-Stage Binary Counter with Trigger Phase Control:

This unit is being developed in conjunction with J. J. O'Brien. The design and construction and testing of the five binary stages have been completed. The trigger phasing circuit is now being added. The unit will be given final testing, packaging, etc., and drawings will be submitted to Sylvania for their use. The circuit will be built into the master clock for the Demonstration Multiplier to replace G.E. counters.

VII. Cathode Follower Probe:

A standard prototype of the probe which has been in use in

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the laboratory for some time is now completed and awaiting drawings to enable construction of eleven more units.

(R. L. Best) A pulse amplitude monitor has been constructed which turns on a light when noise (either positive or negative) gets above a certain minimum level, or when a pulse falls above or below a given range of amplitudes. All of these warning levels are adjustable. The above unit is in breadboard form; a final unit is now being constructed by one of the technicians under Bob Murch.

A large panel is being constructed to simulate the horizontal line driving problem. This will have provision for driving seven tubes at sixteen different points.

A frequency divider is being developed that has an output of 4 K.C. regardless of input pulse repetition rate, and whose output pulse is synchronized with one of the synchronizing pulses.

(R. L. Massard) Video Amplifier, Model 5 Synchroscope.

Present work consists of adjusting the high frequency compensating circuits of separate stages. The overall gain is approximately 140 and the output stage bandwidth is about 23 M.C. Compensation of each stage is made separately to get a smooth frequency characteristic for that stage. Difficulties arise from the fact that there is interaction between the shunt and series components in the four terminal circuits used, and also because the shunt capacities of the output of one stage and the input to the next vary relatively. Reference: Memo M-125.

(E. W. Sard) A periodic program control for multiplier is under construction. The construction should be finished by December 15 or 16, and the unit itself should be in operation by December 19.

4.0 BLOCK DIAGRAMS

(R. R. Everett)

Work is proceeding on a modified set of block diagrams for WWI. These modifications will include the additions mentioned in M-111 as well as changes in existing drawings. The new set of block diagrams should be ready in about one month or about January 15.

The block diagram group has also been engaged in the study of timing problems and checking. These activities are reported separately in Sections 4.1 and 5.0.

Coding for one attack on the coulomb friction problem for the control force loaders has been carried out and is described in Section 9.14.

4.1 Timing Studies

(E. Blumenthal)

A timing study of WWI has been completed based upon the information available in R-127. At present an R-series report is being prepared which will completely describe the results obtained from the study, as well as the background information necessary to substantiate these results.

The greatest limitation to computer operating speed is the switching time of a flip-flop. It was discovered that high speed carry could possibly require greater than 1 microsecond. R.R. Everett therefore has redesigned the ACC section of the accumulator to correct this difficulty. (This is also discussed in the report under preparation.)

A study will be made subsequent to the issuance of this report concerning the design of check problems, with the goal of eventually designing a trouble location system for WWI.

(G. G. Hoberg)

A complete check of the timing scheme outlined in R-127 has been made with E. Blumenthal. See E. Blumenthal's Bi-Weekly Report.

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