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Memorandum 11-752

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Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, MassachusettsSUBJECT: BI-WEEKLY REPORT, PART I, JANUARY 7, 1949

To: 6345 Engineers

From: Jay W. Forrester

1.0 WHIRLWIND I COMPUTER ELEMENTS1.01 Production Report

(H. F. Mercer)

The following WWI panels (production units) have been received from Sylvania to date:

Arithmetic Element (complete)
 Bus Driver, Arithmetic Element (complete)
 Program Register (complete)
 Fixed Voltage Switching Panels (complete)
 Fuse Indication Panels (complete)
 Restorer Pulse Generator (complete)
 Time Pulse Distributor Output
 7 Bus Driver, Flip-Flop Storage
 32 Control Pulse Output Units
 2 Digit Interlock Panels
 3 Register Driver, Type 1

1.02 WWI System Tests

(G. C. Sumner)

During the previous two-week period, system testing has been interrupted, December 27 to December 29, and January 5 to January 8, for further installation of the power system and video cables. A test oscilloscope with amplifier and test probe was obtained January 3. In spite of these delays, system testing of the arithmetic element is well underway.

In testing the shifting channels of the B-register it was necessary to provide a means to read-in arbitrary numbers. Since equipment to do this is not yet installed, a temporary method had to be devised. To do this a short jumper cable was attached at each digit where the digit 1 was desired and

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UNCLASSIFIED1.02 WWI System Tests (Continued)

a pulse thereby applied to both grids of the read-in gate tube. This method has been found very successful and will probably be used for certain other registers.

It was found that the signals received from adjacent digits on the shift channels were not equal for the 0 and 1 sides of the flip flops, because of unsymmetrical loading of the inputs. Even though the amplitude of the 1-digit is apparently ample, a modification has been proposed to equalize the loading, because shifting must be done at a 2 megacycle rate.

System testing of the accumulator will begin 11 January. Work is being slowed somewhat for lack of another test synchroscope with or without amplifier and probe.

1.1 Listed by Block Diagram Number111 Synchronizer
(A. Susskind)

Tests of a push-button-pulse synchronizing unit consisting of five channels have been completed. All specifications have been met and sufficient overdesign incorporated to insure reliable operation. Remote control of the unit, simulating WWI conditions where the pushbuttons will be located in the console, has been tried and found to be satisfactory. The unit has been installed in the temporary console where its use will also serve as a life test.

The design of the WWI synchronizer has been drawn up with the exception of the restart channel. This channel will be different from all the others and its design must depend on the alarm clearing scheme used. Work on the alarm indicators has been started and upon its completion the WWI synchronizer will also be completed.

302 Accumulator.

(W. Papian)

Digit 0. This panel was received from Sylvania as a regular accumulator panel slated to be modified here; consequently, their testing consisted only of resistance checks. Modification having been completed, full testing is now in process.

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UNCLASSIFIED700 Operators Console.

(R. H. Gould)

The experimental breadboard model of the time pulse distributor has been discarded and replaced with standard test equipment. Three register panels and four gate panels are used, a wiffletree circuit replacing the crystal matrix of the time pulse distributor.

Operation of all parts of the temporary console available was found satisfactory with some minor changes and the permanent video cables for the temporary console were installed as completely as possible. Some cables are too short to be run behind the racks as desired and others must be changed because of changes in the console equipment.

The equipment now used for testing the arithmetic element will probably be dispensed with next week and the temporary console used for further tests.

The necessary test equipment to complete the temporary console should be available shortly.

(A. K. Susskind)

A breadboard construction of the alarm indicator design has been received. Preliminary tests have revealed poor operation of the restart synchronizer, which is part of the design, due to switch chatter when clearing the alarm indicators. Alternate clearing schemes are being considered to provide satisfactory restart operation.

1.2 System Engineering

(G. W. Watt)

Installation. Power was shut down for four days, December 24, 27, 28 and 29, and for three days, January 6, 7 and 8, during which periods a crew of about 10 men installed equipment and wiring impossible to put in with power on. All temporary video cabling is in place. Racks AX7, AX8, C14 and C15 have been wired into the system, the power meters have been installed and connected, and room lighting and utility power switches have been installed. The dovetailing of installation and testing has been smooth so far. Considerable installation work can continue after the power is again turned on.

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UNCLASSIFIED1.21 Power Control and Distribution

(R. E. Hunt)

Power Supply Control Drawings. These are well along and should be complete in another week.

Power Supply Control Panel. This panel is now in the shop for construction. It should be complete in 2 or 3 days.

Filament Power Control Panel. This panel is now being checked in the drafting room. All components are on hand.

Marginal Checking Supply and Control. A finished schematic for this section of Whirlwind I is now being worked out. This will probably require one or two more weeks work before it can be turned over to the drafting room.

1.22 Power Cabling.

(H. S. Lee)

The installation of power cables in the arithmetic control racks AX7, AX8, CL4 and CL5 is progressing satisfactorily and should be completed by Tuesday, January 13. A temporary installation of overhead feeder cables has been made and will tie these racks in with the arithmetic element racks.

Design and detailing of the power cables for the flip-flop storage racks is approximately 60% completed. It is expected that the fabrication order and the necessary material will be forwarded to Gavitt Manufacturing Company on or about Thursday, January 15. Gavitt has indicated that the completion date of 1 February will not be impossible to meet.

There is also being installed in Rack CL4 a temporary power setup (a-c and d-c) to provide power for the restorer pulse generator which is being temporarily installed in CL4 at the request of G. Hoberg.

1.23 Video Cabling.

(R. March)

The arithmetic control video cables have been received from Sylvania. About 50% of these cables will be installed by Monday, January 10. Another day with the power off will be required to complete their installation.

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1.23 Video Cabling (Continued)

Accumulator horizontal video cables have been received from Sylvania and will be installed by Monday, January 10.

The two video cables for restorer pulses to the program registers have also been received.

Installation of all A-register and B-register horizontal video cables has been completed.

1.25 Time Schedules

(R. A. Osborne)

All time schedules have been posted through December and prints are now being made. Copies will be distributed to interested persons early next week.

1.3 Auxiliary Equipment

1.31 Power Supplies

(C. R. Wieser)

Test Power for Arithmetic Element. The Power Equipment Company plus 48-volt supply has been installed and is in operation. Test work on the high frequency transients occurring at the output of the supplies has been hampered by use of the supplies to test equipment in the computer room. However, it has been determined that the transients occur in the overlap period when two tubes are conducting simultaneously. RF chokes in the anodes help to reduce the transients. The computer decoupling filters effectively keep these transients from disturbing computing circuits.

Whirlwind I Filament Power. The filament alternator field has been reconnected for 125-volt excitation, and an exciter has been ordered. The alternator and drive motor are on the bed plate awaiting final alignment by shop personnel from Building 32. Wiring of both machines is in progress.

(J. J. Gano)

Synchronous Motor Regulator. The G. E. induction disk-type under and overvoltage relay has been delivered. The protective circuit has been redesigned to incorporate this relay along with another high quality G. E. relay that arrived. Design of a new panel to replace the present temporary one will get underway soon.

Test Power for Arithmetic Element. The temporary -15 volt regulator which occasionally failed to regulate sufficiently close has been removed while the arithmetic element has been down. An additional output tube has been added to increase the capacity to about 1 ampere. At the same time its operation will be checked.

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<u>WVI Drawing List</u>	<u>Block Diagram</u>	<u>Block Schematic</u>	<u>Circuit Schematic</u>
System	B-37071-5		
Control	B-37098-4		
Master Clock	B-37159-1		
101 Pulse Generator	B-37155-2	B-32385	E-32333-3
102 Program Counter	B-37062-4	B-32213-1	D-31516-4
103 Program Register	B-37067-2	B-39289-1	D-31276-8
104 Control Switch	B-37066-3	T60CS00-4-C	Z60CS00-A W60CS00-1-A Z60CS00-2-A
105 Operation Matrix		S600M00	Z600M00-1-C
Control-Pulse Output		R60CP00	S60CP00-1-B
106 Time-Pulse Distributor	B-37068-3	T60PD00-8-B	
106 Time-Pulse Distributor Counter		T60PD00-3-A	Y60PD00-C
106 Time-Pulse Distributor Output		T60PD00-4-B	Z60PD00-1-B
109 Clock-Pulse Control	B-39817-1	C-32642-2	R-31916-3
110 Frequency Divider	B-37154-2	B-32261-1	R-31729-1
111 Synchronizer	- -	- -	- -
112 Restorer-Pulse Generator	B-37160-1	B-32209-4	D-31909-7
200 Storage	C-37156-1		
201 Storage Switch	B-37121-1	B-32855 T60CS00-4-C	Z60CS00-A Z60CS00-2-A E-32830-1 R-32722-1
202 Toggle-Switch Storage	B-37122-3		E-32711
202 Toggle-Switch Storage Output		C32080	E-32721-2
203 Flip-Flop Storage Output	B-37060-5	B-32269-1	E-31635-4
203 Flip-Flop Storage Register	B-37057-4	B-32268-1	E-31621-4
203 Flip-Flop Storage Control	B-37061-7	D-32106-2	
301 A-Register, Digits 1-15	B-37056-2	B-31211-3	D-31276-8

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<u>WVI Drawing List (continued)</u>	<u>Block Diagram</u>	<u>Block Schematic</u>	<u>Circuit Schematic</u>
301 A-Register, Digit 0	B-37056-2 B-37072-7	B-31574-1	D-31573-3
302 Accumulator, Digits 1-14	B-37063-5	D-31213-3	R-31275-5
302 Accumulator, Digit 0	B-37096-5	D-32851	R-32850
302 Accumulator, Digit 0, Aux. Panel	B-37096-5	B-32492-2	D-32602-1
303 B-Register	B-37097-3	B-31212-4	D-31277-5
304 Sign Control & 308 Divide-Error Control	B-37072-7	C-31576-3	E-31619-2
305 Step Counter 305 Step Counter Output	B-37074-5	D-31828-1 A-32723-1	D-39764-1 D-32735-2
306 Multiply & 307 Shift Control	B-37072-7	C-31532-3	E-31588-5
308 Divide Control	B-37072-7	C-31552-3	R-31718-5
309 Special Add Memory & ACO Carry	B-37072-7	C-31575-4	E-31632-2
310 Point-Off Control	B-37072-7	C-31600-6	E-31717-6
403 In-Out Register	B-37119-2	B-32434-1	D-31277-5
404 Comparison Register	B-37120-2	B-32578-1	E-32576-2
601 Check Register	B-39816-2	B-32577-1	E-32576-2
601 Check Register Check		B-32018	E-32023-1
Bus Connections	C-37124-3	C-37123-3	
Bus Driver, Arithmetic Element		A-32297-1	D-31727-6
Bus Driver, Flip-Flop Storage		A-32296-1	D-31726-6
Register Driver, Type I		B-32207-1	R-32261-4
Register Driver, Type II		A-32691-2	D-32690-2
Fuse Indication Panel			W60P00-7-D
Voltage Variation Panel			W60P00-6-B
WVI Power-Connector Pin Connections			B-31955-5

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2.0 WHIRLWIND I RESEARCH2.1 Circuits2.1.1 Flip-Flop Design and Stability

(M. H. Hayes, Jr.)

Experimental investigations have been completed on the dual-triode a-c flip-flop. All aspects of its operation are satisfactory. With a 20 volt output signal, the circuit will operate at 10 megacycles. This was not tried with a chain of pulses however, because of the difficulty in obtaining such a chain. However, the circuit will operate continuously at 10 megacycles.

All that remains to be done on the thesis now is to obtain data and photographs of the operation of the circuit with various parameter values, and to actually write the thesis.

(J. M. Hunt)

A low-speed analogue (see M-709) of the WWI basic flip-flop has been constructed and tested. Time is scaled by a factor of 10^6 on the model tested (i.e., one microsecond of time on the actual flip-flop corresponds to one second of time on the analogue). Voltages and currents of the analogue have been recorded with a Brush oscillograph, which provides an inked-tape record of the flip-flop currents and voltages during a switching cycle. The analogue is triggered by 0.1-second half-sine waves, either cathode or grid triggering being possible. The height, shape, and width of the trigger pulses can be varied if desired.

Preliminary tests indicate that the recorded plate-voltage wave form of the analogue closely duplicates the plate wave form of the original circuit, as observed on a synchroscope. The effects of various circuit capacitances have been observed; these effects were found to correspond closely to the effects predicted by theory and by experience with the high-speed circuits.

A permanent test set-up is now being constructed to facilitate measurements on the analogue.

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2.12 Coupling Methods

(K. E. McVicar)

Two different d-c coupled flip-flop circuits have been investigated. One, utilizing electron coupling, has been temporarily abandoned in view of the extensive program which would be necessary to perfect it. The other, using cathode-follower coupling, is under experimentation. Such circuits are needed in the input-output control.

2.2 Components2.23 Vacuum Tube Studies

(R. L. Ellis)

Fifteen hundred 7AD7 tubes were received recently as well as 400 7AK7's. This gives us 2500 untested 7AD7's and about 800 7AK7's.

The distribution curves for 600 7AD7's have been completed. They will probably be issued in memorandum form.

Tube complements for 7 coder panels have been completed. An adapter for the tube tester to test ion gas current has been completed and works satisfactorily.

(H. B. Frost)

A new pulse tester with design improvements is now under construction. This equipment will pulse 7AD7 and 7AK7 grids to 15 volts using half-microsecond pulses at repetition frequencies determined by a clock-pulse generator. The purpose is to investigate tube characteristics in the usual pulse amplifier operating range.

Tests made on a sample lot of 7AD7 tubes recently produced to L7P mechanical and electrical specifications indicate that they are quite similar to the original L7P production. These tubes will be placed on life test.

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2.3 Systems2.31 Five-Digit Multiplier

(E. S. Rich)

Considerable time has been spent during the past two weeks checking the validity of data obtained in marginal-checking of gate tubes and buffer amplifiers, particularly those associated with the Whiffletree circuits. It has been observed that the output amplitude of the Whiffletree circuits in the Five-Digit Multiplier depends both on the number of pulses passed and on the position of the accumulator flip-flops in the interval during problem solutions. These effects, therefore, have to be taken into account in order to set up a satisfactory marginal checking procedure. It appears that a compromise method will have to be accepted which still will indicate the safe margin of operation, but which will not isolate the Whiffletree from other gate tubes on a panel.

A week ago Read was assigned to work on the Multiplier to replace Frost, who is starting tube investigations.

More work has to be done to improve the margin of operation of the test equipment so that a life test can be started.

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3.0 SPECIAL CIRCUITS

3.2 Test Equipment

3.21 Standard Test Equipment

(R. L. Best)

A prototype is being made of the new scope synchronizer to be called "Multivibrator Frequency Divider." More flexibility of control and wider frequency coverage is being provided.

(R. L. Massard)

Video Amplifier. The second model 3-B amplifier has been lined up and is now being used. The third is ready for lining up. This model amplifier was tested finally by putting through restorer pulses of widths 0.07 and 0.15 microseconds, and exactly the same amplitudes. The pulses out of the amplifier were neither changed in widths nor in relative amplitudes due to original difference in widths.

A complete detailed report has been written on this type of video amplifier.

(C. Rowland & H. Kenosian)

D-C Coupled Register Panel. The prototype of the d-c coupled register panel is undergoing final tests. This unit is similar to the a-c coupled register panel except that d-c coupling is used between the flip-flop and gate tube.

Gate Panel. The gate panels will be modified to accommodate the d-c register panels or the a-c register panels. The gate circuits will also be changed to improve reliability.

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4.0 Block Diagrams

(L. M. Salzer)
(R. P. Mayer)

The block diagrams of the A-Register and B-Register have been revised and brought up to date. One diagram was found to be superfluous (B-37069 for BR) and was eliminated so that there is now only one block diagram each for the A-Register and the B-Register (Nos. B-37056-3 and B-37097-4).

The revision of the accumulator continues. As a result of this work it was found that the dv (divide) operation might have to be modified to prevent interference with any of the algebraic operations which succeed division. This is because after division the AC Carry FF's are not cleared. The addition of a video cable from the control matrix (revised) to the accumulator will be required to clear the AC Carry FF's at the end of a dv operation. For the present there seems to be no other satisfactory solution.

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