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PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 10

JULY 1948

Submitted to the
SPECIAL DEVICES CENTER, OFFICE OF NAVAL RESEARCH
under Contract N5ori60
Project NR-720-003

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts
Project DIC 6345

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TABLE OF CONTENTS

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FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Special Devices Center of the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to The Special Devices Center, Office of Naval Research, Port Washington, Long Island, New York; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

GENERAL STATUS

The semi-annual revision of detailed time schedules has been completed and included in this report. Changes in plans since the first of the year have altered the emphasis on different phases of the computer project, resulting in much scattering of the relative status of computer assemblies.

Actual progress has been made at about three-quarters of the rate as expected in January. The new schedule extends the work by 30% in recognition of this fact.

The original schedule indicated when delivery of computer assemblies was expected, but did not recognize the order in which sub-assemblies would be necessary and useful in putting together the computer. The new schedules show delivery of these units at times corresponding to the installation program.

Those parts necessary for installing the arithmetic element will be ready first. These will be followed by the arithmetic and central control of the machine and by test storage. At that time the entire machine can be operated and many trouble location procedures will be worked out before electrostatic storage is installed. The schedule shown for electrostatic storage is that permitted in relation to other parts of the computer and permits time for design and construction of storage control circuits.

Both the original and the revised time schedules are shown in this report for comparison purposes. In the future only the revised schedules will be posted. The August Summary Report will contain an over-all time schedule for a two or three year period to show the relationship of these detailed activities to longer range objectives.

Accomplishments of the past year have clarified a number of minor details in design which were not well defined when the block diagrams for WWI systems were compiled and issued in Report R-127 (September, 1947). These drawings have been brought up to date and now conform with practical circuit designs and the latest information on coding techniques. During the next month additional effort will be put into checking the logic, drafting accuracy, and consistency in nomenclature of all WWI block diagrams. After completion of this final editing these diagrams will represent the finished version of the logical design of WWI.

As WWI progresses toward completion, the need for further work on the mathematical aspects of high-speed digital computation becomes more pressing. During the summer months the Project mathematics group has taken advantage of the temporary availability of qualified personnel to enlarge its staff. Both the basic principles of digital mathematics and specific methods for applying WWI to the solution of problems are being investigated so that the computer may be put into useful operation as soon as possible after completion. The number of staff available for these application studies is still not sufficient to carry this research at the necessary level.

VISITORS

During July the Laboratory had among its visitors the following:

Mr. Martin Grabau, Executive Director of the Committee on Physical Sciences of the Research and Development Board in Washington, whose organization will coordinate computer research activities.

Mr. Paul G. Bohlke of the Kew Gardens, Long Island, laboratories of Sylvania Electric Products, Inc., to discuss problems of storage tube development and production.

Mr. Charles L. Wright, Jr., of the Stability Section of the Bureau of Ships, who is interested in the application of Whirlwind I to ship design problems.

Dr. R. F. Nicholson of the Cambridge Field Station of Watson Laboratories, who visited the Laboratory to discuss the problem of air traffic control.

Captain W. H. Leahy, Assistant Chief of Research of ONR; Dr. T. J. Killian, Science Director of ONR; and Cmdr. W. L. Thompson, Dr. Roy G. Hoskins, and Prof. Edwin Wilson of the Boston Branch, ONR.

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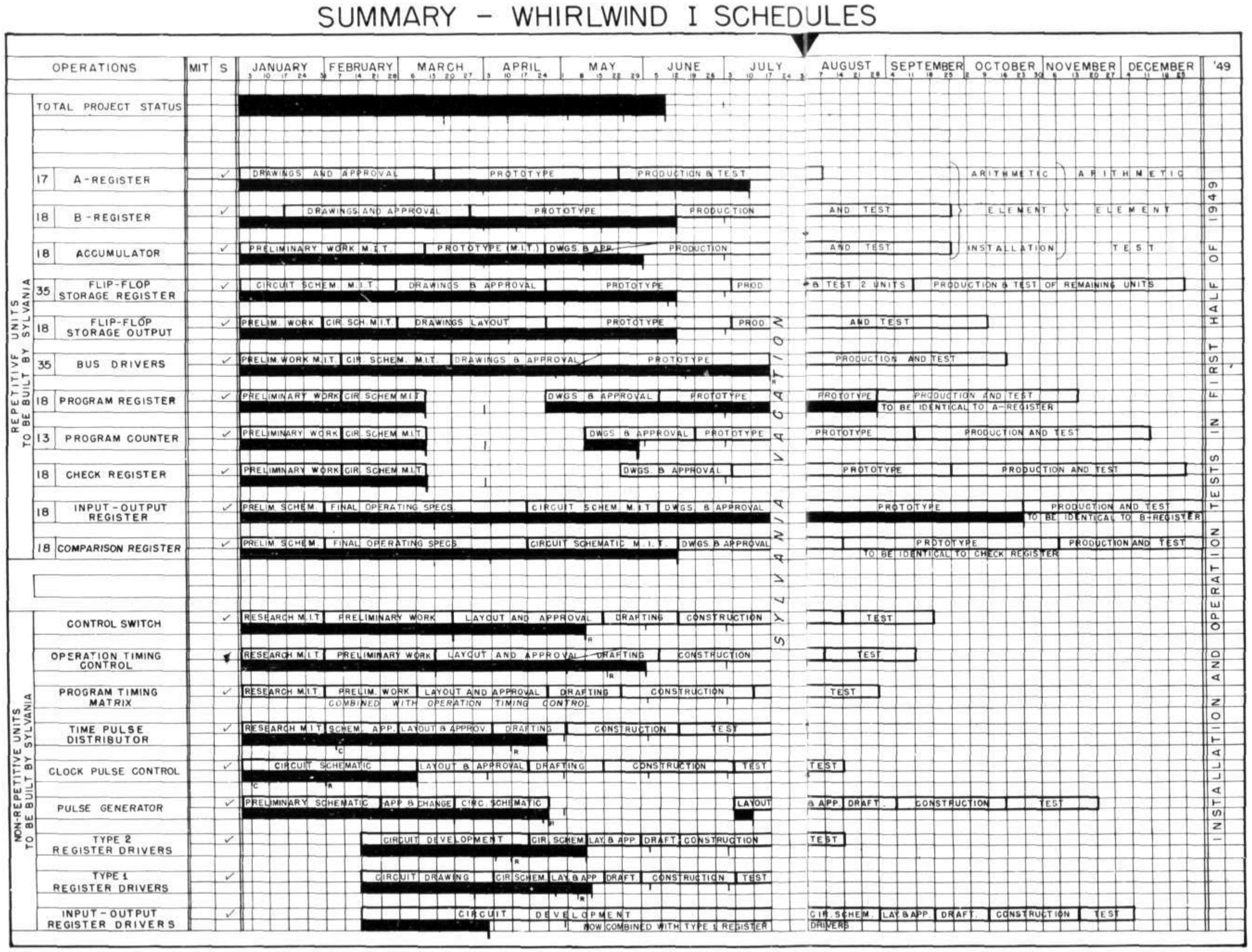
SUMMARY - WHIRLWIND I SCHEDULES



LEGEND

JANUARY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and estimated time allotted for its completion. Estimates made in January 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

Diagonal line indicates overlapping of two operations.

MIT	S
	✓

Column showing whether M.I.T. or Sylvania will do major portion of the job.

NOTES

C Changes in specifications have delayed this item.

S Studies and specifications still incomplete, due principally to lack of staff time.

R Revised schedule does not call for same completion date as originally planned.

T Temporary arrangements can be made to meet required schedule.

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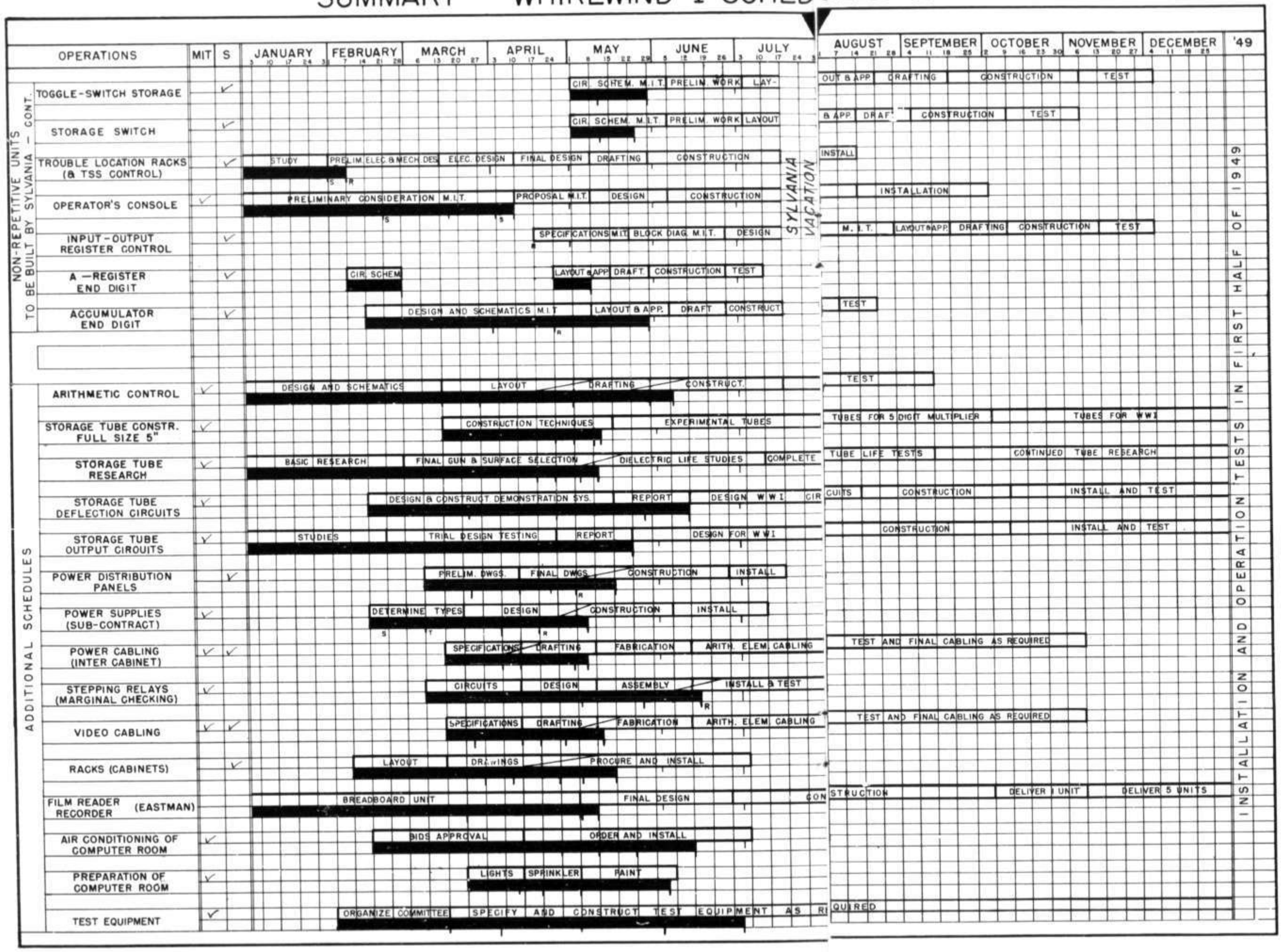

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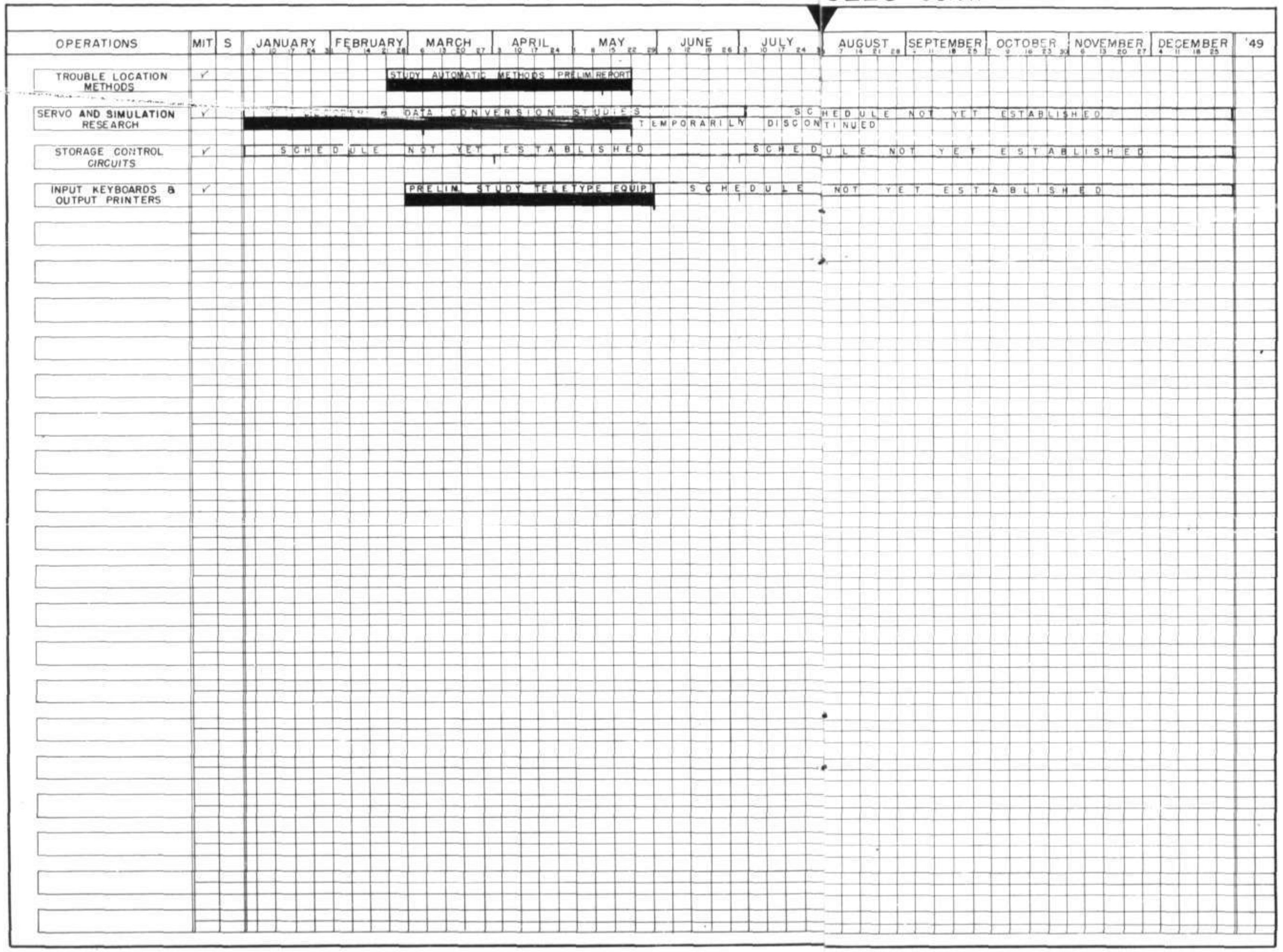

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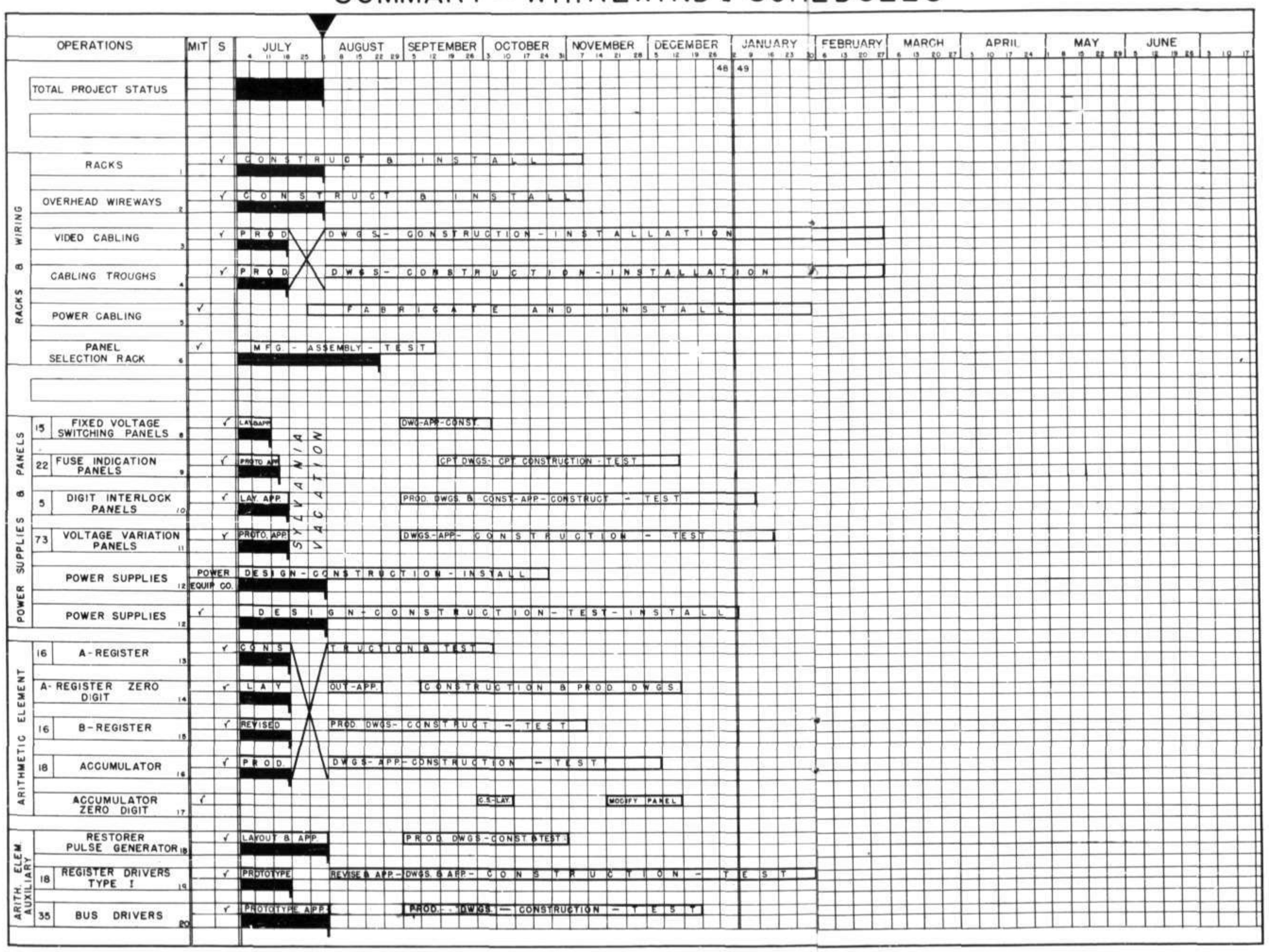

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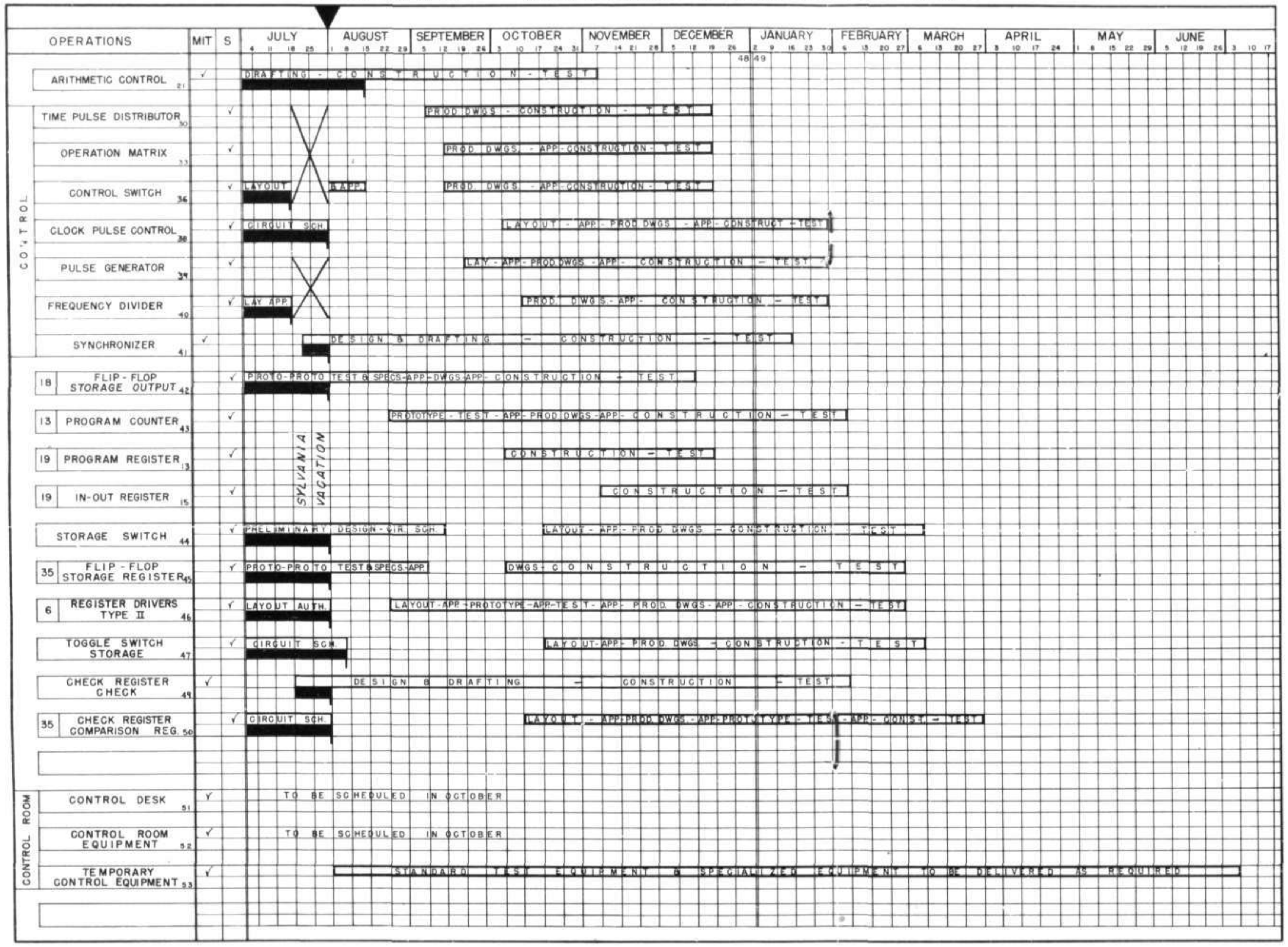

LEGEND

JULY

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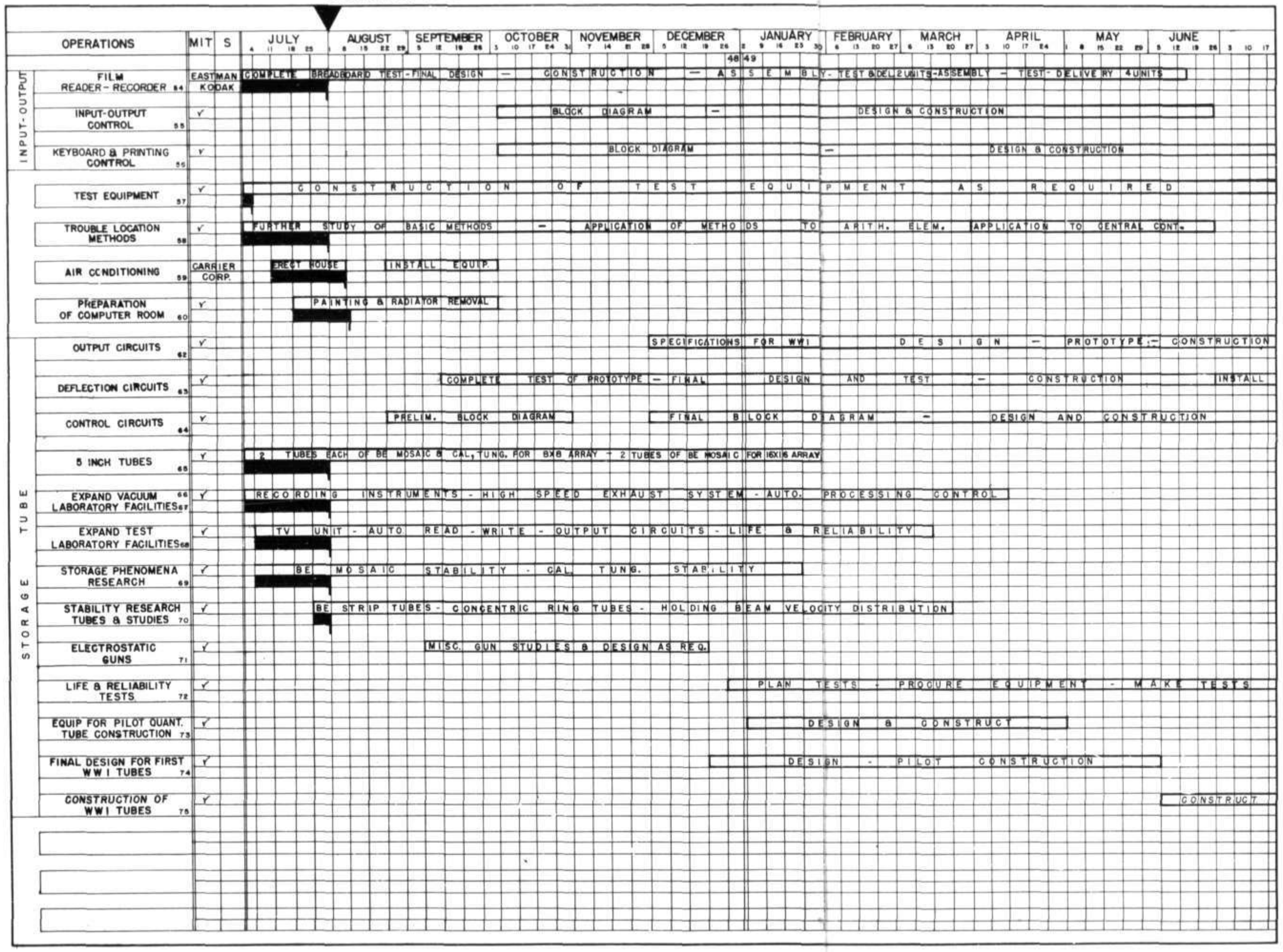
SUMMARY - WHIRLWIND I SCHEDULES -CONT.



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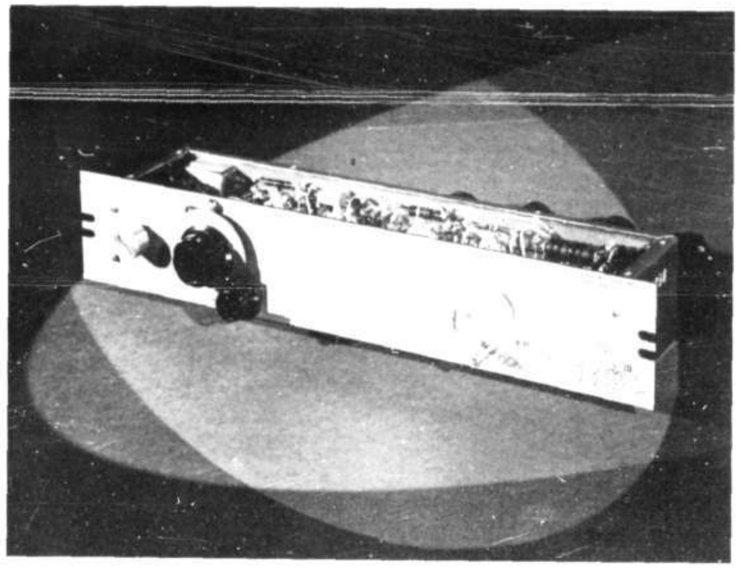

FIG. 1. VARIABLE-FREQUENCY CLOCK-PULSE GENERATOR.

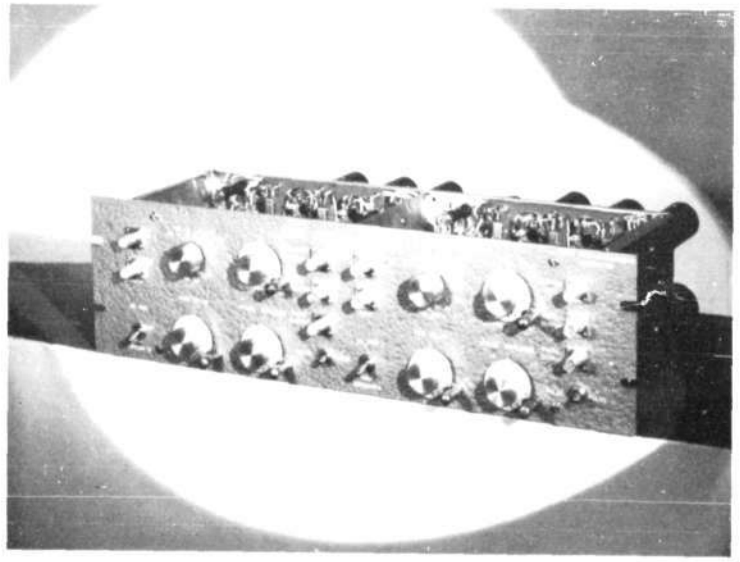

FIG. 2. GATE AND DELAY UNIT.

STANDARD TEST EQUIPMENT

Summary Report No. 6, March 1948, described the establishment of a Test Equipment Committee composed of members of the Project staff. A primary concern of this group was to eliminate the task of assembling test setups each time an engineer wished to experiment with design. The result was a plan to provide standard test equipment units which could be used as building blocks for all types of laboratory investigation.

In order that any sequence of pulses or arrangement of gates could be obtained quickly in each laboratory, the blocks had to include not only standard commercial measuring devices, but also units much broader in nature, adaptable to specific Project needs. It was agreed, therefore, that standard test equipment should operate from the central laboratory power source, should fit a regulation panel rack, should be readily interconnectable by plug-in cables, and should be uniform in appearance. Output pulses would be of "standard" length (0.1 microsecond) at a 93-ohm impedance level.

Most of the equipment necessary for such a plan was not commercially available and had to be designed by staff engineers. The committee recently approved the production of certain test units which it feels will adequately answer present and future needs and which have undergone sufficient laboratory experimentation to establish reliability. To date, the following units have been put in production as standard Project test equipment:

Variable-Frequency Clock-Pulse Generator - a primary pulse source for test setups of gate tubes, flip-flops, matrices, bus drivers, control-line drivers, and other components as well as complete systems and special tests. Model 2, shown in Fig. 1, supplies 0.1-microsecond half-sine-wave pulses at a 93-ohm impedance level with a range of pulse repetition frequencies from 0.2 to 4.9 megacycles.

Gate and Delay Unit - a unit which generates an output pulse at an adjustable time (from 0.5 to 2500 microseconds) after receiving an input pulse. The equipment will also generate a gate whose duration is the same as the delay time of the output pulse and whose amplitude is 40 volts at an output impedance level of 93 ohms. If used in sufficient numbers, these units will produce any desired number and sequence of pulses and gates for controlling WWI elements during design and test. See Fig. 2, which is a double unit containing two independent circuits.

Register Panel - an element consisting of a flip-flop with trigger tube and indicator lights, and two gate tubes with output buffers. Multiple input jacks are provided. The register panel is used for system mock-up in addition to counting, synchronizing, and pulse distribution.

Scope Synchronizer - a frequency divider usable with most commercial synchroscopes. Since the computer circuits employ high pulse repetition frequency, the scope synchronizer provides a sub-multiple frequency needed to operate the synchroscope.

Cathode-Follower Probe - when used as a probe from a synchroscope, this device possesses sufficient input impedance to permit the observation of waveforms without affecting the circuit under test. Fig. 3 illustrates this cathode-follower probe in cross section.

Other test equipment units now in the prototype stage are expected to be in production within a few months. These include a pulse mixer, a coder, a video amplifier, and an amplifier calibrator. To assist in the standardization of Project test equipment, instruction booklets are now being written for each unit beyond the prototype stage. These booklets will be made available to anyone having occasion to use the equipment.

FIG. 3. CATHODE FOLLOWER PROBE.

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DECIMAL - TO - BINARY CONVERSION

Information to be supplied to digital computers will usually occur in one of two entirely different forms, either in decimal digits and English letters or in some measurable physical quantity. In either case, this information must be converted to binary digital form when used by WWI. Most of the information appearing in decimal digits and English letters will arise in the setting up of a problem (i.e., in the actual program which is used to direct the calculations which the machine is to perform) and in the numerical constants supplied at the beginning of the problem. Consequently, there will be little need for extremely high rates of conversion from decimal to binary form.

When the computer is used for simulation and control where large amounts of data must be fed into the computer during a calculation, the data will occur in terms of shaft positions, electrical signals, and similar measurable (analog) quantities. This information must be interpreted into digital form at a high speed. The analog-to-digital conversion has been studied briefly at this laboratory and in more detail by other projects. In analog-to-digital conversion there is, of course, no problem of decimal-to-binary conversion, since the quantities are converted directly to binary form.

There is a close connection between the problems of input conversion and output conversion; in fact the considerations just mentioned concerning the difference in the requirements of analog-to-binary and of decimal-to-binary conversion are valid for output as well as input. A discussion of output conversion, including a detailed description of binary numbers and of binary-decimal numbers, in which each decimal digit is represented by four binary digits, will be found in Summary Report No. 7, April 1948, pp 13-14.

The input plan for conversion of alphabetic and numerical information proposed for WWI will make use of the computer itself to carry out the decimal-to-binary conversion, thereby avoiding the complication of designing and building special conversion devices. The loss of time caused by this use of the computer is negligible, and the gain in simplifying input equipment is great.

According to the present proposal, decimal information will be typed on a standard teletypewriter in columns as it would normally appear on paper. The teletypewriter will provide a typewritten copy for checking and reference and will simultaneously cut a paper tape with one row of punched holes representing each character. These are essentially a set of five-digit binary numbers (pentads) in which the presence or absence of a punched hole in each of the five positions means a one or a zero in ordinary binary representation. Each alphabetic character and decimal digit is represented by a pentad. When the key corresponding to the letter A is struck, an A is typed and the tape cutter cuts holes in the first and second spaces of the row on the tape, but not in the third, fourth, or fifth. The B key will cause holes to be punched in the first, fourth, and fifth spaces only. Thus the letters A and B would be represented by the binary pentads 11000 and 10011, respectively, while the numbers 1 and 2 would become 11101 and 11001. (Certain numbers have the same representation as certain letters and are distinguished only by the shifted position of the teletypewriter carriage. This ambiguity can be taken care of in the WWI conversion program mentioned below.)

The teletypewriter has thus provided a conversion from decimal form to a teletype-coded binary form. The teletype code is quite arbitrary and the coded form is useless to the computer as it stands, but by proper programming the Whirlwind computer can be instructed to translate from the teletype-coded form into binary-decimal form and then arithmetically into the binary form used by the computer (i.e., numbers are translated into ordinary binary numbers, and two-letter combinations into the five-digit order code used by WWI). The teletype tape as taken from the teletypewriter will be handled by a device already designed and under test in which the punched holes of the tape control the settings of flip-flops in a flip-flop register. Information from this flip-flop register can be read into the film reader-recorder being developed by Eastman Kodak. The film thus obtained can then be used to read into WWI at the rate of about three thousand characters per second. The film is used as an intermediate device because it provides a buffer between the slow speed of the teletype tape (about six characters per second) and the high speed of WWI.

A program for the conversion to be carried out by the computer has been written, and it appears likely that the conversion can be accomplished faster than information can be read in from film, so that there is no loss of time resulting from use of the computer to do conversion, at least in the setting up of the calculation. Double-length numbers and numbers with scale factors, as well as ordinary orders and numbers, can be handled in the same fashion without loss of time.

Use of teletype equipment is desirable not only because it is standard equipment already available, but also because it allows information for the computer to be transmitted from remote points direct to the computer by ordinary teletype without requiring any human interference or unnecessary rehandling at the computer.

THE TWO-REGISTER CODING METHOD

The WWI computer is a fixed-decimal-point machine. All numbers upon which operations are to be performed must be fifteen-digit binary fractions of absolute value less than one. Future machines would have a longer register but still of limited capacity.

In the computation and solution of any problem where values will fall outside of this range (between 1×2^{-15} and 1.0), some means of computation of scale-factor, or power-of-two involved, must be provided. With such a method, any problem can be solved regardless of the size of the numbers.

For this purpose, the "two-register" or "multi-register" method of coding has been devised. One register carries the scale-factor, the other the number itself. Multiplications are accomplished by multiplying numbers and adding their scale factors, division by dividing the numbers and subtracting scale factors. For addition and subtraction, scale factors must be made the same and the numbers shifted accordingly before the operation can be carried out.

The task of coding an ordinary problem using a fixed decimal point and investigating scale factors at arbitrary time intervals is a difficult one. It is difficult to prevent the machine from overflowing (that is, to keep the absolute values of the numbers used from exceeding one). The two-register method takes care of this automatically: the problem is coded without regard to scale factor or overflow; then two orders are substituted for each one order, and the two-register code is ready for operation. The second of these two orders calls for a sub-program which carries out the desired operation, and eliminates overflow by adjusting the scale factor in the second register. Two storage registers will also be necessary for each one under a single-register system.

Extension of this method to more than two registers automatically provides a means of single programming of other such complicated operations as those on complex numbers, vectors, matrices, etc. A program could be coded considering vector manipulations as simple algebraic manipulations of real numbers, and then recoded using two orders for each original order.

The limitations of this method are:

1. The requirement of longer computing time. This method averages about sixteen times as long per order as single-length operations.
2. Requirements of more storage. The two-register method for scale factor would require about 250 registers for stored subprograms and twice as many order registers as before. A vector program would require even more storage.

Its advantages are:

1. Ease and simplicity of coding. A purely formal process may be easily followed.
2. Prevention of machine overflows. The two-register method automatically takes care of this time-consuming waste of machine time.
3. Easy means of obtaining bounds on magnitudes of numbers involved. Any problems can be solved in this manner and later solved by more direct methods once maximum and minimum values of numbers involved are known.

A complete library of subprogrammed orders could be stored on film or tape, to be fed into the machine for the proper problems. Thus separate consideration of problems in real numbers, complex numbers, vectors, or any other algebraic fields would be unnecessary.

STORAGE TUBES

General Status

During June and July two storage tubes were built and tested which showed much improvement in performance over earlier models. These tubes used the small research-size storage surface on which a beryllium rectangular mosaic had been formed under more careful control than previously. Earlier tubes have shown an undesirably narrow range of voltages over which the holding gun would provide stability of both positive and negative charges. The new tubes showed stability over a range of several hundred volts.

The laboratory has thus far been unsuccessful

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in constructing a large storage surface using this metallic beryllium mosaic. Failure has been due to the lack of suitable laboratory equipment and to the necessity for further study of processing techniques. In order that more rapid progress may be made in the future, several staff members are now devoting their time to improving the storage tube laboratory equipment and instrumentation. For the evaporation work on large surfaces, a high-speed vacuum pumping system may be required. In order that processing may be better controlled, automatic recording equipment will be installed to register pressures and temperatures in the vacuum processing systems. In the past, evaporation has been accomplished by heating the material in the tube by high-frequency fields from the r-f bomber. As a result, temperatures and pressures cannot be closely controlled. Methods for resistance heating and thermocouple indication of temperature will be installed. Further work on five-inch tubes with a mosaic surface will be postponed until this equipment is available, and studies will continue on the small size targets where difficulty is not encountered.

Several staff members were transferred to the storage tube work from the aircraft simulation project, which is being postponed.

Storage Tube Holding Gun Design

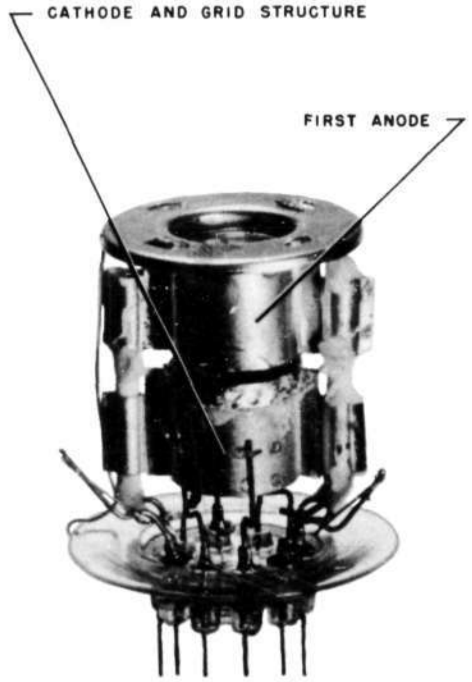
Digits are stored in the Project Whirlwind electrostatic storage tube as spots on the storage surface positively or negatively charged by a high-velocity beam from the writing gun. To prevent growing or shrinking of the stored spots, the surface is continuously sprayed by a diffuse beam of low-velocity electrons from the holding gun.

The design of the holding gun is centered around the requirement of uniform illumination of a 5-inch diameter flat surface by electrons of a uniform and low speed. Optically, this requirement relates the holding gun system to a projector rather than a headlight arrangement. In other words, the electrons emerging from the cathode are first concentrated into a narrow "crossover" that corresponds to the optical focus; then, by means of a second, weaker convex system, a large image of the crossover is formed on the storage surface.

Electron optical studies have shown that the emission from a barium oxide cathode emerges from more or less discrete places, surrounded by areas of poor emission. Furthermore, this distribution picture varies with temperature and age. Ordinarily the images of such emitting centers are "washed out" by the space charge in front of them. The guns of cathode ray tubes, however, run close to temperature-limited emission because of the low amplification factor and relatively high first-anode voltage necessary to get high emission. Therefore, the image of a crossover, where the electrons are arranged according to their initial thermal velocity, will give a more uniformly illuminated disk on the storage surface than the image of the cathode.

In the practical design this requirement of a crossover image can be only partially fulfilled because other specifications - low-voltage operation, low grid cut-off voltage, low current loss to the beam-forming electrodes - demand a design of low amplification factor (large grid aperture close to cathode) and thereby tend to move the image-forming plane toward the cathode.

The present holding gun is a compromise between these requirements. With a maximum of 500 volts at the electrode system and an electron velocity of 100 to 200 volts at the storage surface, a 5-inch fluorescent disk is uniformly illuminated,



STORAGE TUBE HOLDING GUN

as far as can be told by visual inspection; the grid cut-off voltage is -35 volts, and the beam current arriving at the storage surface is a little more than 0.5 ma. This results in a current density of 5μa per sq cm on the 5-inch disk. At 1000 volts maximum, the beam current is between 2 and 3 ma, while the illumination still is uniform; at 1500 volts the current is considerably higher, but the uniformity is impaired.

The holding gun makes use of parts taken from standard 5 UP cathode ray tube guns. The cathode is kept without change; the grid aperture is opened up from 0.031 to 0.047 inch diameter. The first anode is a cylinder 0.437 inch high with an inner aperture of 0.100 inch and an outer one of 0.250 inch. Second and third anodes consist of aquadag coatings at the inside of the storage tube glass envelope, biased to meet the requirements of the high-velocity writing gun.

The loss of beam current to the beam-forming electrodes is predominantly carried by the first anode, which is at the highest potential. This loss is confined to about 30 percent of the cathode emission at 500 volts and to about 5 to 10 percent at 1000 volts maximum. Since secondaries such as those liberated here originate near the point of most positive potential of the beam course, they are not expected to contribute appreciably to non-uniformity of speed in the beam at the storage surface. However, the collector screen mesh in front of the storage surface may cause difficulty; this is to be investigated.

The holding gun is designed to cover an area 5 inches in diameter at a distance of about 12 inches from the gun. This area can be reduced to 1 inch in diameter by reducing the third-anode potential to values of the order of 15 volts positive with respect to the cathode. This makes the holding gun applicable for use in research tubes with 1-inch storage surfaces.

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APPENDIX

REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were among those issued during July.

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
SR-7	Summary Report No. 7	17	-	4-48	
SR-8	Summary Report No. 8	17	-	5-48	
R-137	Life-Testing of Surfaces Suitable for Electrostatic Storage Tubes (Abstract in E-116)	73	24	5- 7-48	H. L. Heydt
R-138	Glossary of Computer Terms	12	-	5-48	(J. N. Ulman (G. G. Hoberg
E-114	Characteristics of Standard Flip-Flop Basic Circuit FF1	8	4	5-21-48	J. M. Hunt
E-121	Gate and Delay Unit	2	1	5-14-48	H. Kenosian
E-129	Tube Life in the Deflection-Voltage Generators	3	-	6-30-48	D. R. Brown
E-132	Gate-Tube Investigations	4	3	7- 8-48	M. H. Hayes
E-135	Life Data of 7AD7 Tubes of Five-Digit Multiplier	2	-	7-20-48	J. J. O'Brien
M-395	Distillation in Vacuo from a Right Cylindrical Toroid	15	2	6- 9-48	M. Daniloff
M-479	Production Drawings for WWI Units Constructed at MIT	4	1	6-28-48	A. M. Falcione
M-488	Life Tests on Beryllium Storage Surfaces	6	7	6-17-48	H. L. Heydt
M-489	Secondary Emission Measurements on Beryllium Storage Surfaces	5	2	6-17-48	H. L. Heydt
M-501	Holding Gun Stability Tests on Storage Tube 28-1	7	23	6-16-48	J. S. Rochefort
M-505	Revision in Program Timing	1	-	6-24-48	E. Blumenthal
M-508	Bi-Weekly Report, Part I, June 25, 1948	19	-	6-25-48	
M-509	Bi-Weekly Report, Part II, June 25, 1948	22	-	6-25-48	
M-510	Eastman Conference, June 24th	5	-	6-28-48	H. R. Boyd
M-511	6AG7 Life Tests	1	-	6-25-48	H. Fahnestock
M-512	Trouble Location in a Large-Scale Electronic Digital Computer	4	-	7- 6-48	G. C. Sumner
M-513	Power Feed to the Control Elements of WWI	2	-	6-28-48	E. Blumenthal
M-516	WWI Meters	2	-	7- 1-48	W. S. Rogers
M-517	Design of a Holding Gun for Use in Storage Tubes	6	8	7- 2-48	H. Klemperer
M-518	Storage Tube Testing	7	-	7- 2-48	S. H. Dodd
M-519	Program of Mathematical Objectives	1	-	7- 7-48	P. Franklin
M-520	Rack Ground Bus	1	-	7- 7-48	H. S. Lee
M-527	Calibration of a 15E EIMAC as an Ionization Gauge	3	6	7- 7-48	J. H. McCusker
M-529	Instruction Booklets for Test Equipment	2	-	7- 8-48	R. Rathbone
M-530	Bi-Weekly Report, Part I, July 9, 1948	18	-	7- 9-48	
M-531	Bi-Weekly Report, Part II, July 9, 1948	17	-	7- 9-48	
M-532	Parts List Distribution	1	-	7-12-48	C. W. Watt
M-533	Decimal to Binary Conversion for WWI Input	13	2	7-15-48	C. W. Adams
M-534	Fuse Indication Panel Prototype Approval	2	-	7-13-48	C. W. Watt
M-535	Symposium on Numerical Methods of Analysis in Engineering - Illinois Institute of Technology, Chicago, May 7, 1948	4	-	7-13-48	E. Reich
M-541	Standard Test Specifications for WWI	1	-	7-20-48	C. W. Watt
M-544	Conference on Installation Problems, WWI	2	-	7-21-48	H. S. Lee
M-546	Synchronizer Design Proposal	2	-	7-21-48	J. A. O'Brien
M-552	Bi-Weekly Report, Part I, July 23, 1948	16	-	7-23-48	
M-553	Bi-Weekly Report, Part II, July 23, 1948	17	-	7-23-48	
C-54	WWI Seminar No. 28: Runge-Kutta Method of Numerical Integration	4	-	5-17-48	P. Franklin
C-55	WWI Seminar No. 29: Runge-Kutta, etc.	3	1	5-19-48	P. Franklin
C-56	WWI Seminar No. 30: Runge-Kutta, etc.	5	-	5-24-48	P. Franklin
C-57	WWI Seminar No. 31: Runge-Kutta, etc.	5	-	5-26-48	P. Franklin

Translation

M-524	The Application of Newton's Method to Functional Equations - (REPORTS OF THE ACADEMY OF SCIENCES OF U.S.S.R., by L. V. Kantorovich)	9	-	7- 7-48	M. Daniloff