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Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Lexington 73, Massachusetts

Subject:    TRIP TO NSA, WASHINGTON, D. C.

To:         J. W. Forrester

From:       D. J. Eckl

Date:       30 March 1955

Approved:   _DRB_____
            D. R. Brown

Abstract:    NSA in Washington has submitted to Philco a purchase
             description for a computer, SOLO, to be built with an
             SBT control and arithmetic unit and a 4096 register
             ferrite core memory.  NSA and Group 63 have agreed to
             maintain close contact regarding their respective
             transistor computer projects.

On 15 March 1955 D. R. Brown and I visited NSA in Washington,
D. C., to discuss the Philco surface-barrier transistor with J. J. Eachus,
Assistant Director for Development.  Present at the discussion were the
following people from NSA:  Joseph J. Eachus, Howard Campaigne, Roger
Moulton, C. R. Blair, Douglas Hogan, and A. E. Slade.

NSA has submitted to Philco a purchase description for a
digital computer called SOLO which is to use a surface-barrier control
and arithmetic unit and a ferrite-core memory.  It has been suggested
that Philco call on MIT as a consultant for writing the memory specifica-
tions and for choosing the subcontractor to do the memory work.  NSA
requested that they be kept informed of the transistor work at Lincoln
and we agreed.  Copies of the Philco Subcontract No. 49 reports will be
sent to NSA.

A brief description of some of the principal requirements for
the SOLO computer follow.  These aspects will be stressed in the order
given:

1. Reliability.
2. Compactness.
3. Design for convenience and minimum distraction.
4. Low power consumption and heat dissipation.
5. Complexity of order code.
6. Speed of operation.

The control and arithmetic element are to be constructed of surface-barrier transistors. The memory is to consist of ferrite magnetic-core elements.

Three versions of successively reduced complexity have been proposed. It is desired that the most complex version consistent with compactness, reliability, and power consumption be constructed. All three have a 4096-word memory. The word length is 36, 28, and 24 bits for versions one to three, respectively. The order code is correspondingly reduced in complexity.

The reliability criterion requires that the probability of a detected error in 50 hours of scheduled operation be less than 20 percent. Preventative maintenance procedures should not be scheduled more often than once every 40 hours of operation.

Exclusive of terminal equipment but including the core memory SOLO must fit within a floor space of 40 x 60 inches with a maximum height of 72 inches. A working area 20 x 40 inches must be available at the 30-inch level. The weight must not exceed 1500 pounds. The unit should be portable.

Power consumption should not exceed 25 amperes of 80 percent power factor at 125 volts, 60 cycles. Cooling is to be by air, entering room at $75^{\circ}$F, with exhaust air limited to a maximum rise of $15^{\circ}$F. Input air temperature variations of $\pm 15^{\circ}$F and relative humidity values up to 60 percent should be tolerated.

Signed: *Donald J. Eckl*
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DJE/md


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