Division 6 - Lincoln Laboratory
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SUBJECT: MEETING TO DECIDE MTC MEMORY SELECTION SCHEME, SEPTEMBER 16, 1953

To: N. H. Taylor

From: W. A. Hosier, P. R. Bagley

Date: September 18, 1953

Abstract: To help settle some of the questions raised by the prospect of having a 4096-register magnetic memory in MTC (See Memorandum M-2361), this meeting of MTC personnel and programmers was arranged. Opinion was heavily in favor of a bank-switching instruction which could include drum fields as banks. Certain other features desirable from a programming standpoint were also brought up.

Persons attending:

Group 6345:	C.W. Adams	J.M. Frankovitch
	D.N. Arden	F.C. Helwig
	D. Combelic	E.S. Kopley
	M.S. Demurjian	J.D. Porter
	H.H. Denman	A. Siegel
Group 61:	W.A. Clark	
Group 62:	P.R. Bagley	
	W.A. Hosier	
	R.P. Mayer	

Memorandum M-2361 outlined four principal proposals for addressing a 64 x 64 memory in MTC; of these, the last, adding a 17th digit to the computer throughout, was abandoned because of time and manpower limitations. Of the other three, a variation of proposal I (use of a special bank-switch instruction) was unanimously supported, since it of all the proposals implied the possibility of addressing the drum, treating drum fields in exactly the same way (from the programming standpoint) as the two 2048-word banks of the magnetic-core memory.

Under this plan, there would be two four-bit registers controlling bank selection: first, the "Program Timing Bank Selector", effectively an extension of the program counter, indicating from which bank instructions are to be taken; second, the "Operation Timing Bank Selector", effectively an implicit extension of the addresses of instructions, indicating from which bank to take the numbers, etc., manipulated by the instructions.

Within the 2048 registers of a bank, addressing would of course be done with the usual 11 address bits; the 64 registers of Panel Storage (toggle-switch and plugboard) would be treated as a distinct bank in themselves.

Making allowance for a possible 12 drum fields, then, this scheme leads to 15 "banks" in all, addressed in the following manner: (octal addresses)

Address	Refers to Memory Section	Bank Selector Setting
0 - 3777	Panel Storage (repeats modulo 64)	0000
4000 - 13777	Magnetic Core Memory	0001 - 0010
14000 - 73777	Magnetic Drum	0011 - 1110 incl.

An alternative addressing scheme, slightly less favored as being a bit more complex to implement and as requiring sacrifice of 64 registers of core memory, is the following:

0 - 77	Panel Storage	0000
100 - 3777	Magnetic Cores, Bank A	0000
4000 - 7777	Magnetic Cores, Bank B	0001
10000 - 67777	Magnetic Drum	0010 - 1101 incl.

The principal question raised by this plan is the exact manner of effecting a "transfer of control" (i.e., reset the program counter, MTC tr and tn, corresponding to WWI sp and cp). Usually the new instruction location will be in the same bank where the program is, but occasionally one will want to transfer out of the bank, and this requires 15 bits of address. Further, it is highly desirable to accomplish the transfer in one instruction, especially if it is a conditional transfer: this means having a preset bank indication available when the tr or tn is executed. The technique of transferring to the address indicated in the register whose address is given by the transfer instruction was rejected as being clumsy both from a programming and electronics point of view; it was agreed that the best solution would be a transfer instruction which resets the program counter to agree with the (previously set) operation timing bank selector. To avoid the necessity of resetting the latter when transferring inside a bank in a program whose addresses are largely outside the bank, it was thought that a special "inside transfer" instruction would be helpful, which would always leave the bank-selection digits of the program counter undisturbed. For this purpose one could make use of the positions now occupied in the MTC instruction code by the instructions tp and np.

Thus, in sum, to take care of the 64 x 64 memory and, as a by-product, to address the magnetic drum in like manner, three instructions will be added:

1. a "bank-select" instruction (bk?)
2. a "transfer-inside" instruction (ti?)
3. a conditional or "negative transfer inside" instruction (ni?)

It was not contemplated, at least for the present, to install block transfer instructions or to group all in-out operations under a general

instruction like WWI's si. Block transfers between drum and core memory, if made in MTC, will thus be a succession of single-word transfers, and necessarily somewhat slower than the WWI type.

Some minor aspects of the system discussed were there:

1. It might be a help to be able to read out of the bank selector.

2. For using floating-address routines, it would be desirable to have the program counter carry from the end of one bank to the beginning of the next.

Aside from the question of memory bank selection, Prof. Adams and his group brought up several features they would like to see incorporated into MTC, principally to facilitate extra-precision arithmetic and floating-binary-point routines:

1. Changes in the overflow alarm system. Instead of sensing the overflow-storing flip-flop at the end of the instruction which has generated the overflow, they suggest sensing it at the beginning of the next instruction, with consequences varying according to the nature of the next instruction. Thus "shift right" would merely shift contents of the overflow FF into AC0 and clear the former; a "transfer on overflow" would be possible; most other instructions, not intended to make specific use of an overflow, would ignore it or cause an alarm. Probably can be done with very little trouble.

2. A "scale-factor" instruction. This implies the ability to shift left in AC and BR. Might be added when MTC is moved, especially if new FF's with bufferless gates are put into AC and BR, thus freeing space where buffers were on shift-gate panels.

3. Alteration of paper-tape reading setup to use 7th hole as a parity indicator. They say read-in errors have been frequent on WWI. Perhaps the Ferranti reader may improve reliability to the point of making this unnecessary; at any rate it should be considered.

4. Possible use of a 2's complement representation for negative numbers instead of the present 1's complement. This would be much neater for adding modulo 2, ignoring overflow, but is unlikely for now.

Not mentioned, but possibly of interest, are instructions of the absolute value sort (WWI's cm, am, dm).

Prof. Adams said his group would give thought to delegating someone to act as liaison with MTC; he was assured that a desk would be made available in the MTC area any time he should need it.

Signed: W. A. Hosier
W. A. Hosier

WAH/rb

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