Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: MTC MEETING OF JULY 25, 1952

To: MTC Planning Group

From: R. R. Everett and W. A. Hosier

Date: July 28, 1952

Abstract: Decisions and progress relevant to the proposed Memory Test Computer (MTC) are summarized for distribution to those interested, and to trace development of the computer.

Present:

R. R. Everett	W. N. Papian
W. A. Hosier	L. L. Sutro
R. P. Mayer	N. H. Taylor
W. Ogden	H. Smead
K. H. Olsen	R. von Buelow

N. Taylor expressed concern lest MTC circuits, through faulty liaison within the Laboratory, should fail to take full advantage of the latest WWI ideas and experience in this regard. He suggested, therefore, that before any circuit design is frozen or definitive policy laid down, a committee of qualified people (e. g., R. Best, N. Daggett, C. Corderman) pass upon it and make sure it is as up-to-date as possible with current thought and practice.

In this connection, it was pointed out that a meeting is to be held Wednesday, July 30, to examine plug-in circuits, which will probably constitute at least the arithmetic element of the MTC.

Circuits directly concerned with the magnetic memory will of course derive less benefit from WWI experience.

N. Taylor also thought it would be important to know the peak duty factor for the memory drivers (over, say, a minute's operation) - mainly on account of heat dissipation, since overheated screens tend to give off gas and poison cathodes. This figure, under the most extreme conditions, can not exceed 50%, since read and write pulses must alternate in the memory, and are taken from separate drivers. If necessary, programming or insertion of arbitrary delays in order cycles could reduce the duty factors; but this would seem inadvisable in a memory testing device since it would in like degree limit the memory core duty cycle. The problem is not thought to pose difficulties in the MTC, with its metallic cores, but could be more serious in WWII, with the higher currents demanded by ferrite cores and more stringent demand for reliability.

R. Everett expressed a desire to see the MTC group draw up an honest-to-God time schedule, showing just what is supposed to be done by when, and clearly stating what cooperation they will need from other sources in order to stick to it. This should serve the two-fold purpose of exposing bottlenecks as they occur and of forcing the group to make detailed plans that might otherwise be neglected. Such a schedule is important especially to the MTC, the usefulness of which will be almost completely vitiated if it is not ready soon enough. As an example of a comparable design and construction effort, Everett cited the first bank of WWI electrostatic storage.

It was agreed that in about a week, tentative schedules of this sort would be submitted by W. Papian, D. Brown, and L. Sutro.

Construction of the memory hinges considerably on the delivery date of 20,000 satisfactory cores (the 300 sample cores recently received and tested were slow - 20 microseconds switching time, though all right in other respects); nevertheless, such problems as can be anticipated will be worked on, cores or no cores - even to the extent of constructing "arrays" out of ceramic bobbins if necessary. *

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* (Magnetics, Inc. has said that the ceramic bobbins are the critical item slowing down core production.)(!)

The question of cannibalizing one of the two ferrite test arrays for test equipment was raised but not decided (presumably pending L. Sutro's forthcoming schedule). The value of the equipment and manpower thus released would have to be weighed against the usefulness of the array in furthering work on ferrites and in training new men.

It was agreed that MTC block diagrams and most other drawings should be graded, starting now, to assure better liaison. Although many changes are likely to be forthcoming in the block diagrams, particularly with regard to control, still some parts of the arithmetic element, such as the accumulator, can profitably be got under construction as soon as some of the above-mentioned circuit decisions have been reached.

W. A. Hosier

R. R. Everett

WAH/RRE:bs