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PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 15
DECEMBER 1948

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SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Cambridge 39, Massachusetts
Project DIC 6345

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FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to the Office of Naval Research, Navy Department, Washington 25, D. C.; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

GENERAL STATUS

The entire arithmetic element of the Whirlwind computer has now been delivered. All panels have passed detailed individual tests including video operation to simulate use in the computer. Preliminary tests on the entire arithmetic element show favorable results. All panels of arithmetic control have likewise passed individual tests. The arithmetic element and arithmetic control (see Summary Report 14), along with the equipment in the temporary console (see Summary Report 13), are capable of all arithmetic and shifting operations of the complete computer. Tests on these individual functions will begin in January.

Schedules posted to the end of December show a delay of about one month behind the plan of last July; this represents closer estimating than for the previous six months. Since again there is considerable scattering in the status of individual equipments due to changed plans and priorities, a new set of schedules will be made to take effect in January. Because almost all research problems of Whirlwind I have been solved, these new schedules will represent almost entirely design, construction, and installation. The possible accuracy should therefore be greater and estimates can be extended further into the future. The new schedules will extend through the assembly of WWI.

Four storage tubes were constructed during December. Three were satisfactory and will be used in tests of storage tube circuits and for life tests on the tubes themselves. One had a glass defect resulting in poor vacuum. The reliability tester for storage tubes, described briefly last month and to be treated more fully in January, was in preliminary operation. Such early tests as were attempted on storage tubes gave satisfactory results. These tests included the cyclic reading of a 16-by-16 stored pattern and the indexing of this pattern one point at a time through the tube so that the tube was subjected to a changing progression of stored signals.

Preliminary tests on marginal checking in the five-digit multiplier show the anticipated detection of weak circuit components, and verify that we can expect to detect deteriorating components before

they cause computer errors.

INSTALLATION AND TESTING OF WWI

During the month of December installation of power wiring to the arithmetic element was completed, associated indication and alarm systems were connected, and two complete 16-digit registers, the A-register and the B-register, were installed. Preliminary wiring checks showed no wiring errors in the d-c system, and only a few minor mistakes in the a-c and indication wiring. Errors were corrected before power was turned on, and on December 14 the d-c voltages were put on the system for the first time, with the registers not connected. No trouble was experienced, and on December 15 the panels were connected and power applied for the first time to the system. Restorer pulses were applied the same day to the A-register, and its flip-flops were made to restore satisfactorily.

System testing proceeded for the next few days. With a small array of test equipment providing restorer pulses and high-frequency clock pulses, the allowable amplitude limits of register-driver operation were studied. Also the optimum terminations for lines feeding all digits of registers were determined. Restorer pulses are fed from a central register-driver stage for each register. The sample curves on page 10, showing voltages at the flip-flop cathodes, indicate that the attenuation along the line is smooth and not excessive. This information, coupled with the observation on a test synchroscope that no spurious reflections or distortion occur at any point, shows that the lines are well terminated at both the sending and receiving ends.

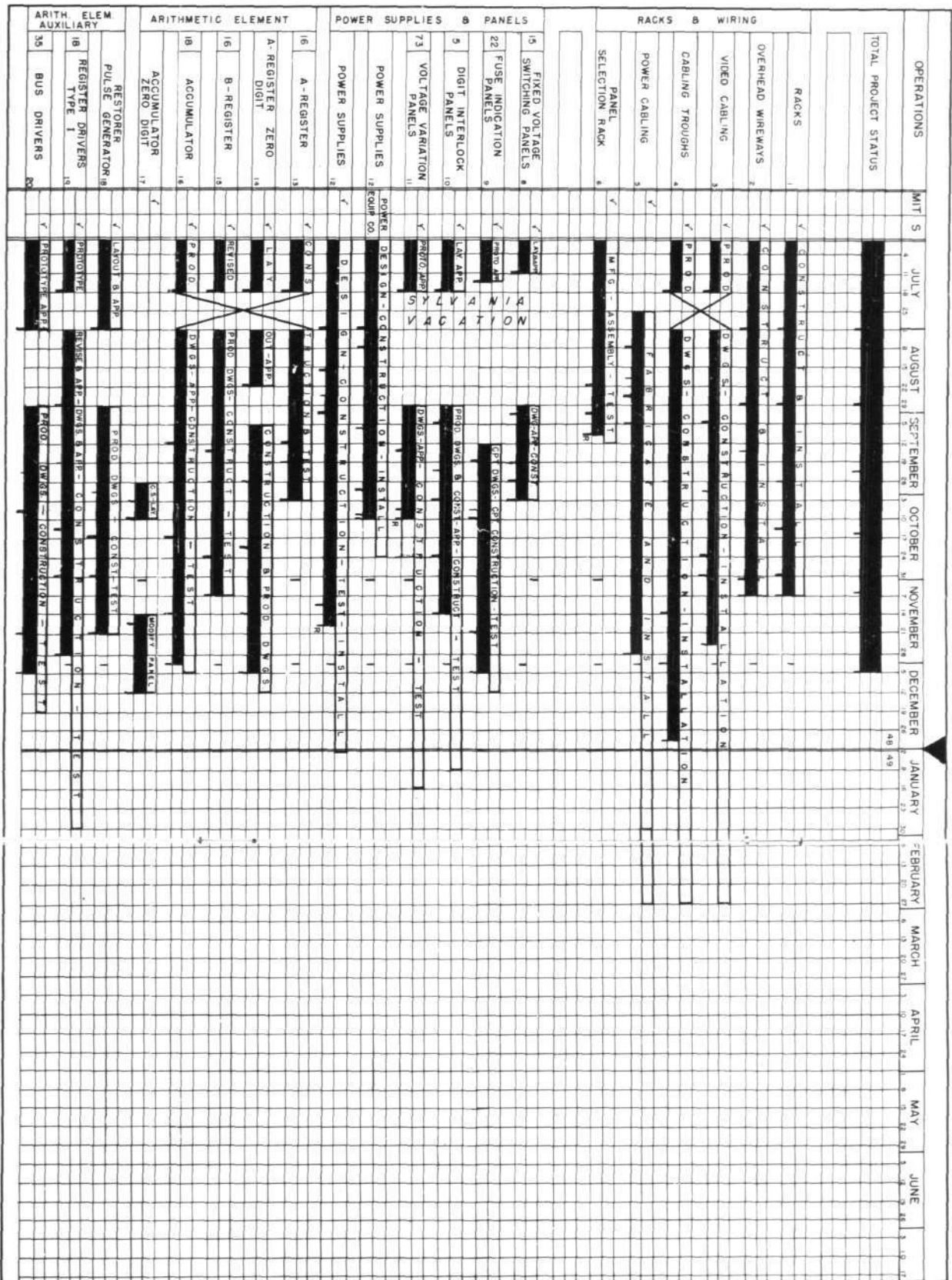
Power was shut down for four days near the end of the month to permit the installation of more wiring.

Wiring for neon light flip-flop indication and blown fuse indication is now complete for the arithmetic element, including arithmetic control; lumiline room lighting is complete and operating; and all power failure interlocks are operative, although some switch and relay panels are not in their final form. Five of the permanent power supplies are installed and operating. Bias voltages are presently being obtained from laboratory sources. As the month ended, system testing had begun again.

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SUMMARY - WHIRLWIND I SCHEDULES



Legend: JULY, PROTOTYPE

Period of one month, comprising the total number of days in the month.

Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

Column showing whether M.I.T. or Sylvania will do major portion of the job.

NOTES

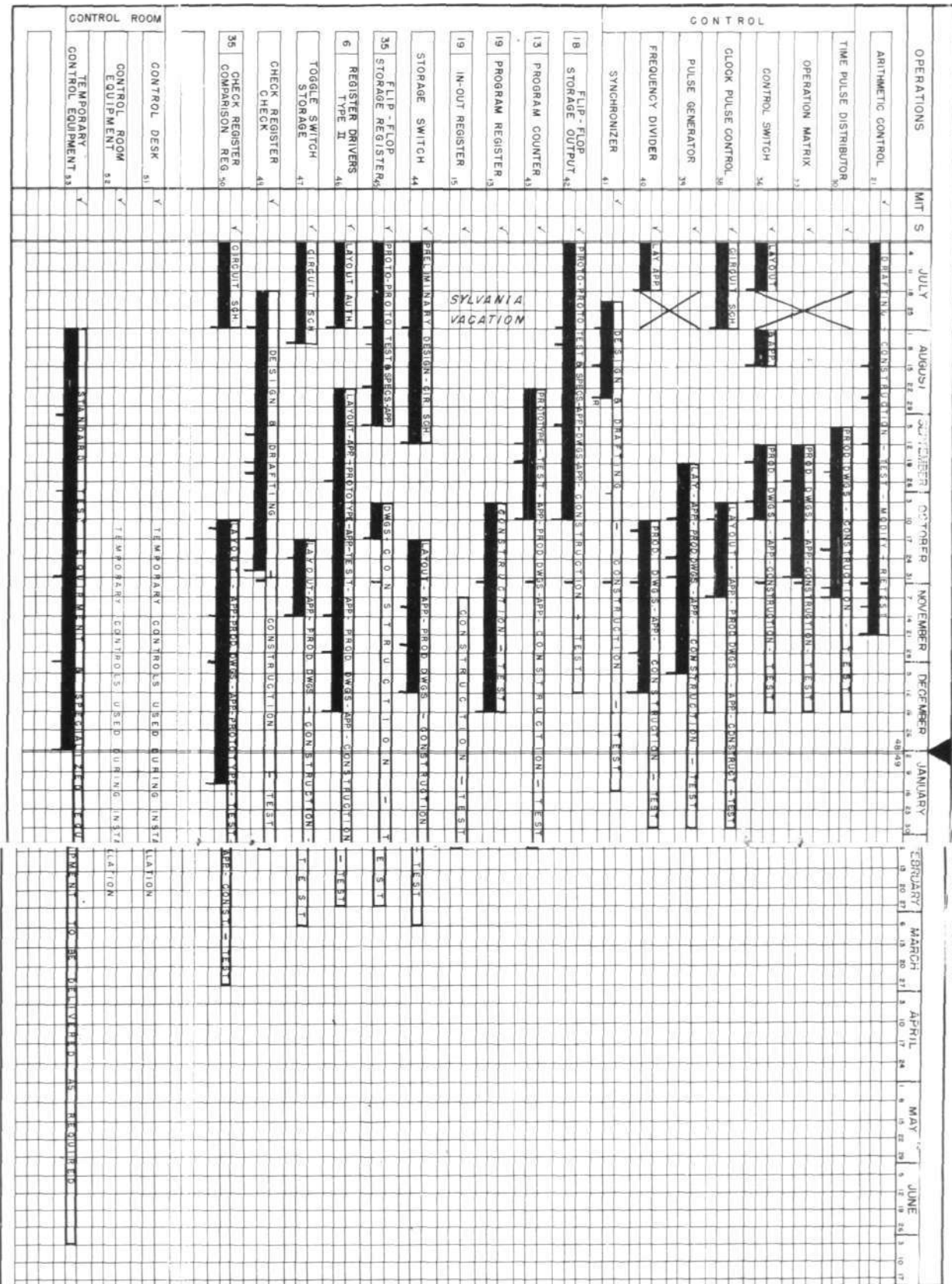
R Revised schedule does not call for same completion date as originally planned.

For a long-range plan from 1944 to 1952 showing the relation of this detailed schedule to past and future work, see Summary Report No. 11, August 1948.

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SUMMARY - WHIRLWIND I SCHEDULES CONT.



LEGEND

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1946.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

MIT

S

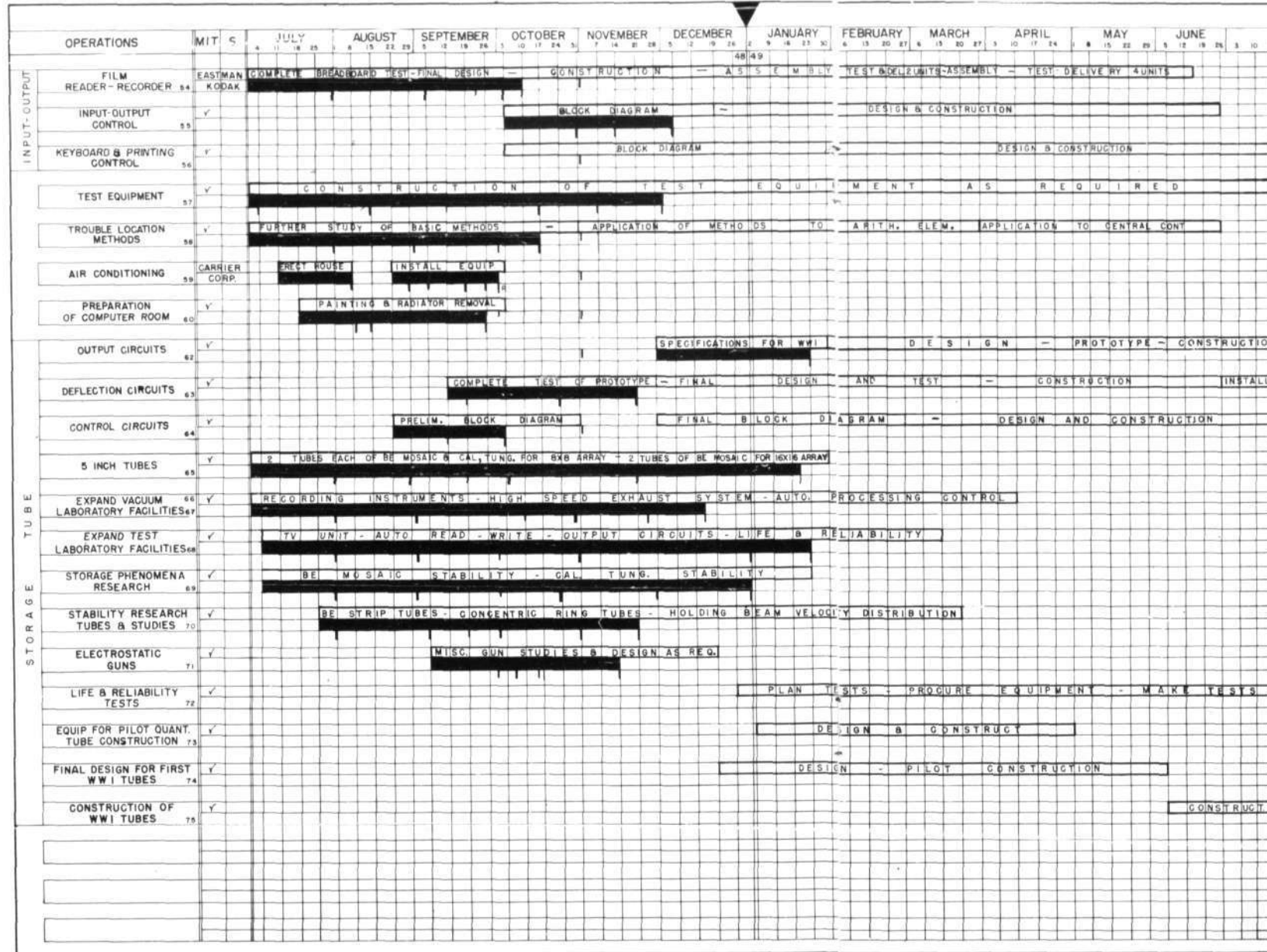
Column showing whether MIT, or Sylvania will do major portion of the job.

NOTES

R Revised schedule does not call for same completion date as originally planned.

For a long range plan from 1944 to 1955 showing the relationship of the various projects, see Summary Report No. 11, August 1946.

SUMMARY - WHIRLWIND I SCHEDULES -CONT



LEGEND



Period of one month, comprising the total number of days in the month.



Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.



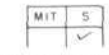
Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.



Date of latest posting.



Summary line. Shows overall status of the project.

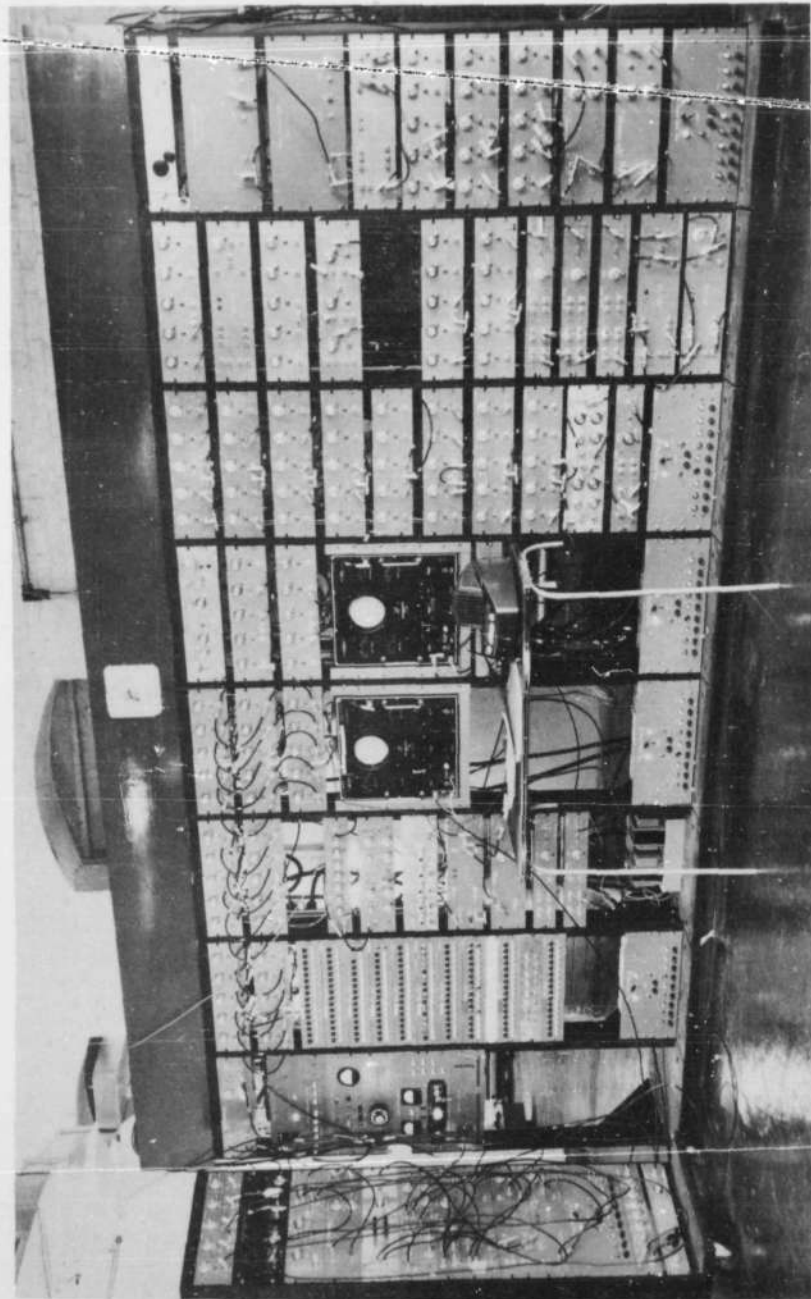


Column showing whether M.I.T. or Sylvania will do major portion of the job.

NOTES

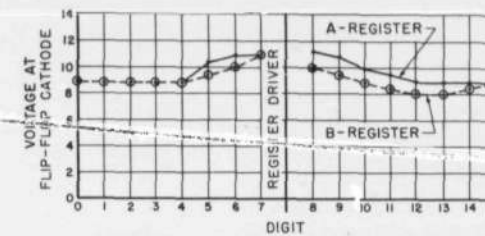
Revised schedule does not call for same completion date as originally planned.

For a long-range plan from 1944 to 1952 showing the relation of this detailed schedule to past and future work, see Summary Report No. 11, August 1948.



TEMPORARY CONSOLE AND CONTROL

Shown above are racks of standard test equipment to be used as a temporary operator's console from which WWI apparatus can be controlled manually by means of toggle switches and pushbuttons. These test-equipment units, all of which (except for the synchroscopes) were designed and built by the Project, provide sufficient high-speed control and number-storage facilities to permit repetitive performance of single arithmetic operations at standard WWI pulse-repetition frequencies. See Summary Report 13 (October, 1948) for a block diagram and description of the system.



ATTENUATION OF RESTORER PULSES

STORAGE TUBE RADIO-FREQUENCY OUTPUT SYSTEM

The Need for an R-F Output System

Operation of the electrostatic storage tube requires an output system that is able to separate switching transients from output signals. The tube has a holding gun to provide a low-velocity diffuse beam of electrons which spray the storage surface, establishing two stable potentials and maintaining a charge distribution despite leakage, crosstalk between spots, and other disturbing influences. A high-velocity well-focused electron beam is used to switch spots on the storage surface between the two stable potentials and thus store the digit "one" and "zero". A wire mesh screen held closely in front of the storage surface acts as a collector of secondary electrons. A metal backing plate, or signal plate, picks up signal output current by capacitive coupling to the storage surface and also acts as a switching electrode for controlling the surface potential during the writing and reading operations.

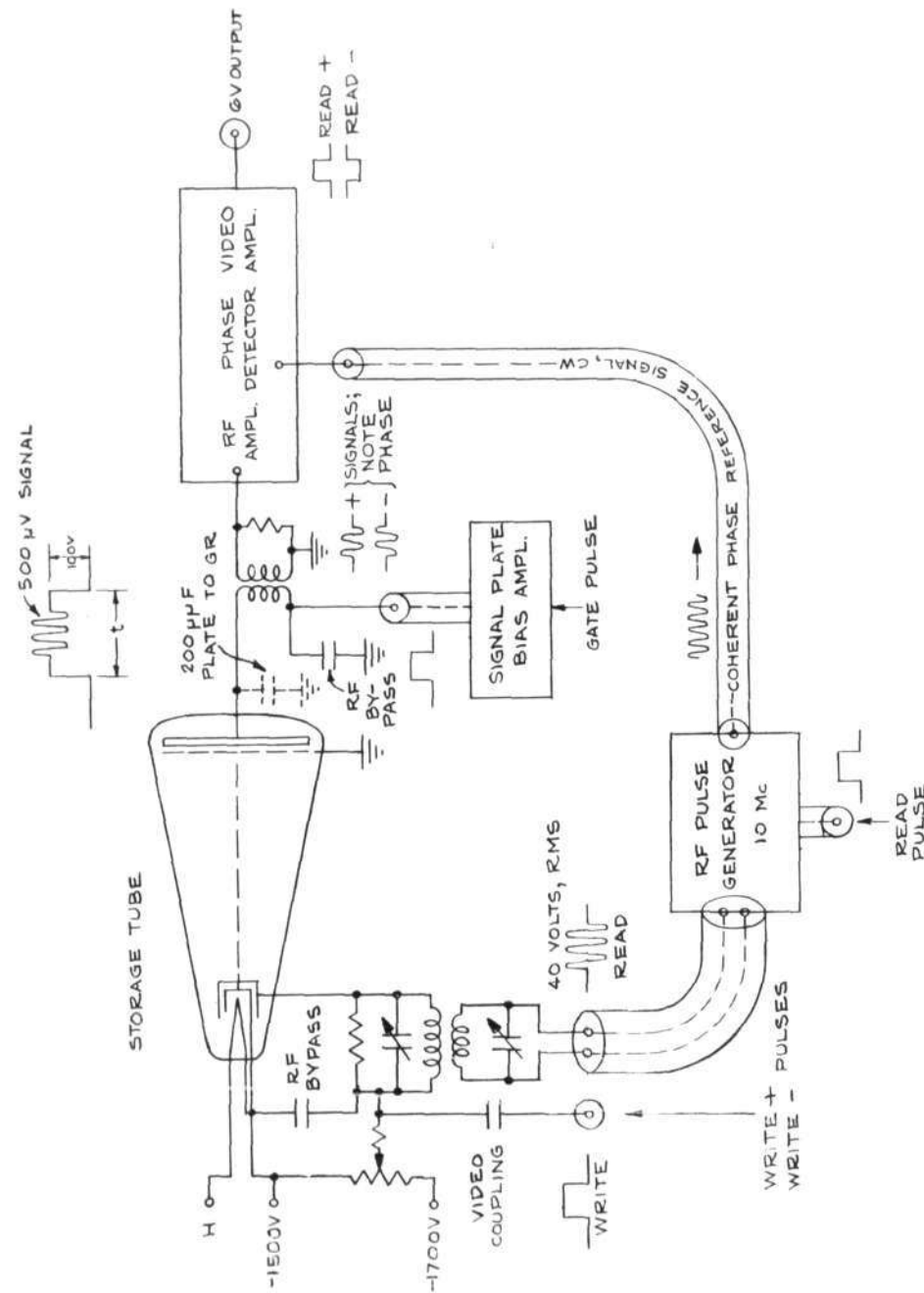
Requirements on speed, voltage and noise levels, and impedance levels are determined by the choice of operating cycle during writing and reading. Let us consider first the basic method of operation and then several possible cycles.

The holding gun charges any spot on the storage surface to either the wire screen potential (positive stable potential) or the holding-gun cathode potential (negative stable potential). The write-read gun always charges a spot to collector potential, but has small effect on the potentials of adjacent areas. Thus, to write a positive spot, the write-read gun de-

flexion voltages are adjusted to choose the required spot and then the current is gated on until writing has been accomplished. The current density of the write-read gun is large enough to over-ride the holding-gun action during this writing process, so that it is unnecessary to cut off the holding-gun current. A negative spot is written by switching the signal plate positive before the write-read gun current is gated on and returning the signal plate to its neutral potential after writing has been completed. The signal-plate switching pulse thus carries the surface positive by capacitive coupling, the writing current pulse charges the spot to collector potential, and the end of the switching pulse carries the spot negative. The pulses are adjusted so that the spot is charged to holding-gun cathode potential. Potentials of adjacent areas are not appreciably affected by the writing operation, and the holding gun now perpetuates the new potential configuration. During the signal-plate switching pulse the holding beam is cut off to prevent discharge of other stored signals.

Reading is accomplished by either partial or complete discharge of spots and a detecting of discharge current flow to the signal plate. The spot potential can then be restored by allowing the holding-gun current to charge a partially discharged spot back to its stable potential or by rewriting with the write-read beam. A study of computing cycles is being made to determine the available time for restoring the spot after reading, and intensification of the holding beam immediately after reading is being considered. Two methods can be used for reading. One method does not switch the signal plate during reading, and results in a small output pulse for a spot at the positive stable potential and a large output pulse for a negative spot. The other method switches the signal plate positive with a gate of one-half the amplitude used during the write-negative operation, and results in an output pulse of one polarity for a positive spot and of the other polarity for a negative spot.

Operation of the Whirlwind storage tube requires switching the signal plate by about 100 volts as a part of storing a negative charge. If switching is used during reading, a pulse of about 50 volts is required. The output signals which indicate the polarity of the



RF OUTPUT SYSTEM FOR STORAGE TUBE

stored charge are of the order of 0.1 volt in magnitude for a video output system, and must be distinguished from the large switching voltages. The distinguishing circuit must have a very short discrimination time if the access time of the storage tube and consequently the speed of the computer are not to be adversely affected.

If the reading operation is carried out without switching the signal plate and if the holding beam is relied upon to restore the charge lost during reading, then signal-plate switching can occur only during writing. Since on the average there is only one writing operation for each five or more reading operations, the output-circuit discrimination time is involved only once in 6 references to storage and is of relatively small importance. A number of possible circuits developed by the Project might be suitable for this use, at least temporarily; see Summary Report 5. These circuits operate on the output pulse resulting from a video pulse on the reading-gun grid and have shown a discrimination time of 25 microseconds.

It is by no means certain that the above type of reading can be tolerated. It may be necessary to re-write charges immediately after reading or to switch the signal plate during reading to obtain better signal-to-noise ratios and better checking. These questions can be answered only after further study and tube development. In either case the output-circuit discrimination time must be added to both reading and writing times, and thus becomes of great importance. For this reason the development of an output system using a radio-frequency intensity-modulated beam has been undertaken. It is expected that such a system will provide much shorter discrimination times than the video circuits so far developed and at the same time will be much more reliable. Another advantage of the r-f reading system is an improvement in signal-to-noise ratio, permitting reliable reading of smaller signals and thus reducing the minimum size of spot, or increasing the number of points that can be stored.

Design of the System

Briefly, the system operates with an r-f intensity-modulated reading beam, resulting in an

r-f pulse output from the signal plate. The phase of this output pulse reverses with the polarity of the signal being read out if the signal plate has been switched. After being amplified in an r-f amplifier, this signal is demodulated in a phase-sensitive detector, giving a video pulse of the appropriate sign. The reduction in switching transients results partly from the fact that fast recovery from overloads is easier to obtain from an r-f amplifier than from a video amplifier, and partly from separation of the signal from the switching transient in the frequency domain as well as in the time domain. Improved signal-to-noise ratio is contrary to what would be expected from theoretical considerations of noise power, but results from the fact that most of the noise is in the form of video disturbances which are outside the pass-band of the r-f amplifier.

A block diagram of the system is shown in the attached figure. The reading beam is modulated by applying a short carrier-frequency pulse to the control grid of the reading gun. A frequency of 10 megacycles was chosen for various practical considerations such as the physical size of the circuit associated with the signal plate and the relative ease of shielding for various frequencies. The grid is normally biased below cut-off and is driven into the conducting region, as in a Class C amplifier, by alternate half cycles of the modulating signal. The modulation is never made large enough to drive the grid positive, as this would result in poor focus. Coupling to the grid is through a double-tuned circuit to permit video pulses to be applied to the grid for writing.

The r-f carrier pulse is obtained from a pulse generator through a balanced transmission line. The power output of the pulse generator system is sufficient to drive a bank of storage tubes in parallel. The pulse generator consists of an oscillator, a buffer amplifier, and a grid-modulated output stage providing a peak power output of about 50 watts. Balanced circuits are used in all high-level parts of this system in order to produce only r-f voltages which are symmetrical with respect to ground and are therefore much less likely to cause interference. The design of the plate circuits of the output stage involves many of the same problems encountered in

the design of a wide-band i-f amplifier, because the envelope of the r-f pulse should have rise and fall times of approximately 1/4 microsecond.

The output signal obtained from the signal plate of the storage tube is coupled to the r-f amplifier through a double-tuned circuit similar to that used to drive the reading-gun grid. This permits the application of the necessary video switching gates to the signal plate during reading and writing. The phase of the output signal, relative to the modulating voltage on the grid of the reading gun, depends on the polarity of the signal being read. The beam current, and the current to the storage surface during reading, consist of approximately half-sine-wave pulses of 10-megacycle frequency. Reversing the polarity of the signal being read reverses the polarity of the net current pulses to the storage surface and thus reverses the phase of the excitation of the tuned output circuit. After being amplified to a suitable level, this r-f signal is applied to a phase-sensitive detector and demodulated to give an output signal, the polarity of which is determined by the polarity of the stored signal. The amplifier consists of 5 stages (two stagger-tuned pairs and one single stage) having a maximum gain of about 85 db and a bandwidth of 3.5 mc. The coherent phase-reference signal for the detector is obtained from the oscillator in the r-f pulse generator through a separate buffer-amplifier, phase-shifting circuit, and cathode-follower output stage.

In preliminary experiments on the television demonstrator this system gave an output signal which was superior to anything achieved with the former video output systems. The access time (the time during which the signal plate is switched, the signal is read, and the plate switched back to the original potential) was less than 20 microseconds; it will be reduced by further circuit refinement.

ORDERS IN THE WHIRLWIND COMPUTER

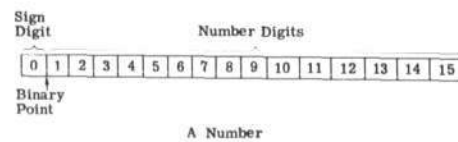
A desk calculator performs a single arithmetic operation at a time, when so ordered manually. It is the operator's task to see that the orders follow

a predetermined plan. Since human intervention can consume a major portion of the computing time, it is imperative to make the sequencing of operations, called programming, automatic for high-speed computation.

In Whirlwind I, as in other high-speed calculators, storage facilities make an automatic program possible. It will be helpful to distinguish between two physically identical types of storage: one for the orders of the program, the other for the numbers involved in the computation. Both the orders and the numbers are 16 binary digits long and are stored in storage registers of corresponding length. Thus in appearance there is no difference between numbers and orders; only their location in storage permits the machine to distinguish between them. Practically, there is but one type of storage in WW, any register of which may be used to store either a number or an order.

This article describes the system of orders to be used in WWI. There are many other possible systems, some differing in the number of references to storage given in each order, others in the major and minor details of the operations described by the orders. Any desired arithmetic or logical calculation can be carried out with only a very few kinds of orders. It is, however, always possible to devise special orders which make it easier to do the more common types of calculations. The system chosen for WW is completely general and at the same time flexible enough for easy use.

The first digit of a number specifies its sign, while the other fifteen determine its magnitude. The binary point (corresponding to the decimal point in the decimal system) is fixed on the left-hand end of



the number, so that the machine handles only numbers less than one. This fixed-point characteristic of the machine must be given due attention in programming; however, it does not decrease the general

LIST OF ORDERS

(Abbreviations: AC - Accumulator, DP - P-Register)

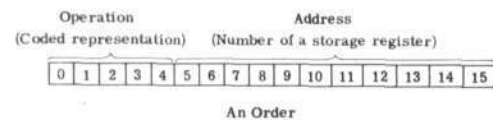
Name	OPERATION			ADDRESS	FUNCTION
	Code				
	Letter	Number			
	Decimal	Binary			
Clear & add	ca	16	10000	Locates operand, x	Puts x in AC
Clear & subtract	cs	17	10001	Locates operand, x	Puts -x in AC
Add	ad	18	10010	Locates operand, x	Adds x to contents of AC
Subtract	su	19	10011	Locates operand, x	Subtracts x from contents of AC
Clear & add magnitude	cm	20	10100	Locates operand, x	Puts /x/ in AC
Negative magnitude	nm	21	10101	Locates operand, x	Puts -/x/ in AC
Add magnitude	am	22	10110	Locates operand, x	Adds /x/ to contents in AC
Subtract magnitude	sm	23	10111	Locates operand, x	Subtracts /x/ from contents of AC
Multiply & roundoff	mr	26	11010	Locates multiplicand, x	Multiplies x by the contents of AC and rounds off to 16 digits (including the sign digit)
Multiply & hold	mh	27	11011	Locates multiplicand, x	Multiplies x by the contents of AC and holds full product in AC and BR.
Divide	dv	28	11100	Locates divisor, x	Divides contents of AC by x
Shift left	sl	29	11101	Specifies number of digits to shift	Shifts number left with respect to binary point and loses portion passing the binary point.
Shift right	sr	30	11110	Specifies number of digits to shift	Shifts number right with respect to binary point and rounds off 16 digits
Scale factor	sf	31	11111	Gives desired location of scale factor indication	Counts number of zeroes between binary point and first significant (one) digit of number in AC
Transfer to storage	ts	10	01010	Specifies storage register	Transfers contents of AC to specified storage register
Transfer digits	td	9	01001	Specifies storage register	Transfers address section of contents of AC to specified storage register to change address of an order
Subprogram	sp	15	01111	Specifies storage register	Breaks into program at the order stored in the specified register
Conditional program	cp	14	01110	Specifies storage register	Does same as sp but only if the contents of AC are positive

usefulness of the computer, because by a linear transformation any number can be changed to the range from -1 to +1.

The orders are stored in consecutive registers and are extracted by the control of the computer in the same sequence. Thus the arrangement of orders in storage corresponds to the program (or routine), though provision can be made in the program to break into the sequence at any desired point.

Functions of the Orders

An order in Whirlwind I specifies two things in general: the operation to be performed (What?) and the number that is to take part in the operation (Which?). The left 5 digits of the order give a coded representation of the operation, while the right 11 digits specify the storage register (or the address) in which the number in question is stored.



The Whirlwind I orders may be classified according to their functions, as follows:

- a) arithmetic manipulations
- b) transfer orders
- c) special orders

The most important orders are described in the accompanying table. A simple example of coding is used to illustrate their role.

Coding Example

Required: to prepare a program for the evaluation of the function

$$f(x) = Ax + \frac{1}{x} - Ax$$

where A is a known positive constant less than 1/2 and x is a variable with values between 3/4 and 1. We see that no number greater than one will occur in the calculation. We need storage registers to store A, x, and other quantities arising during the calculation.

We choose the following storage registers to hold these numbers:

Register No.	Number/content
100	A
101	1/2
132	x
208	Ax
117	x ²
133	f(x)

The random choice of register numbers emphasizes that numbers need not be stored in the sequence in which they are used, because the address section of an order can specify any of the storage registers.

The program orders, on the other hand, should usually be stored in consecutive registers. We might store this program in the registers indicated:

Register No.	Order-content		Function
	operation	address	
50	ca	132	Ax is computed and stored
51	mr	100	
52	ts	208	
53	ca	132	x ² is computed and stored
54	mr	132	
55	ts	117	
56	ca	101	$\frac{1}{2} - Ax$ is computed
57	su	208	
58	dv	117	
59	ad	108	f(x) is obtained and stored
60	ts	132	

The first three orders will be explained in detail as an example. The order stored in register 50 takes the number x out of storage register No. 132 and inserts it into the accumulator of the arithmetic element. The control of the computer then looks for the next order in the next storage register; i.e., in register 51. This order instructs the control to multiply the number in the accumulator by the number in storage register 100. This number is A for the equation being evaluated. The order therefore extracts the number A, which is thus brought into the arithmetic element to be multiplied by the number x, already in the accumulator. The result is rounded off to 16 digits. The next order, stored in register 52, transfers the contents of the accumulator, Ax, into storage register 208, as specified by the address section of the order.

Other Orders

This example is so simple that it illustrates only the basic coding principles and the more elementary arithmetic operations. The role of other orders in the tabulation is as follows: the shifting orders were listed with the arithmetic operations because one shift to the left results in a multiplication by two; one shift to the right, a division by two. These orders are often used for this purpose. They can also be used to separate certain digits of a number by shifting the rest of the register length; this might be done in order to find the fractional portion in an interpolation.

Sometimes in setting up the program it is impossible to tell in advance the magnitude of numbers that may arise in the process of calculation. The scale factor order is therefore introduced in the program to count the number of zeros to the right of the binary point. This is done by shifting the number in the accumulator to the left until a one appears next to the binary point, and counting the number of shifts. The number of shifts required is stored in the storage register indicated in the order. Thus the order accomplishes two things: it brings the significant part of the number in the accumulator up to the binary point, and it stores the scale factor for future use in the program.

The transfer-digits order puts only the address section of a number into storage. It can thus make up the address of later orders according to some arithmetic results. It is used for indexing when the same program is employed with different sets of numbers stored in different storage registers.

The subprogram and conditional program orders direct the control to change the sequence of orders by specifying the particular register from which the next order is to be extracted. The conditional program makes this action dependent on the sign of the number in the accumulator. The combination of these two orders gives a flexibility in coding not provided by the consecutive programming method alone. They permit use of the same subprogram at different places in the main program or employment of the same subprogram repeatedly in methods of successive approximations.

Fourteen other orders will be used with

Whirlwind I to assist such functions as operating with double-length numbers, speeding up computing by special subprogramming, displaying results graphically on an oscilloscope, and providing the necessary link between the computer and the input-output equipment.

A VIDEO AMPLIFIER FOR SYNCHROSCOPES

Use of Synchroscope on High-Frequency Signals

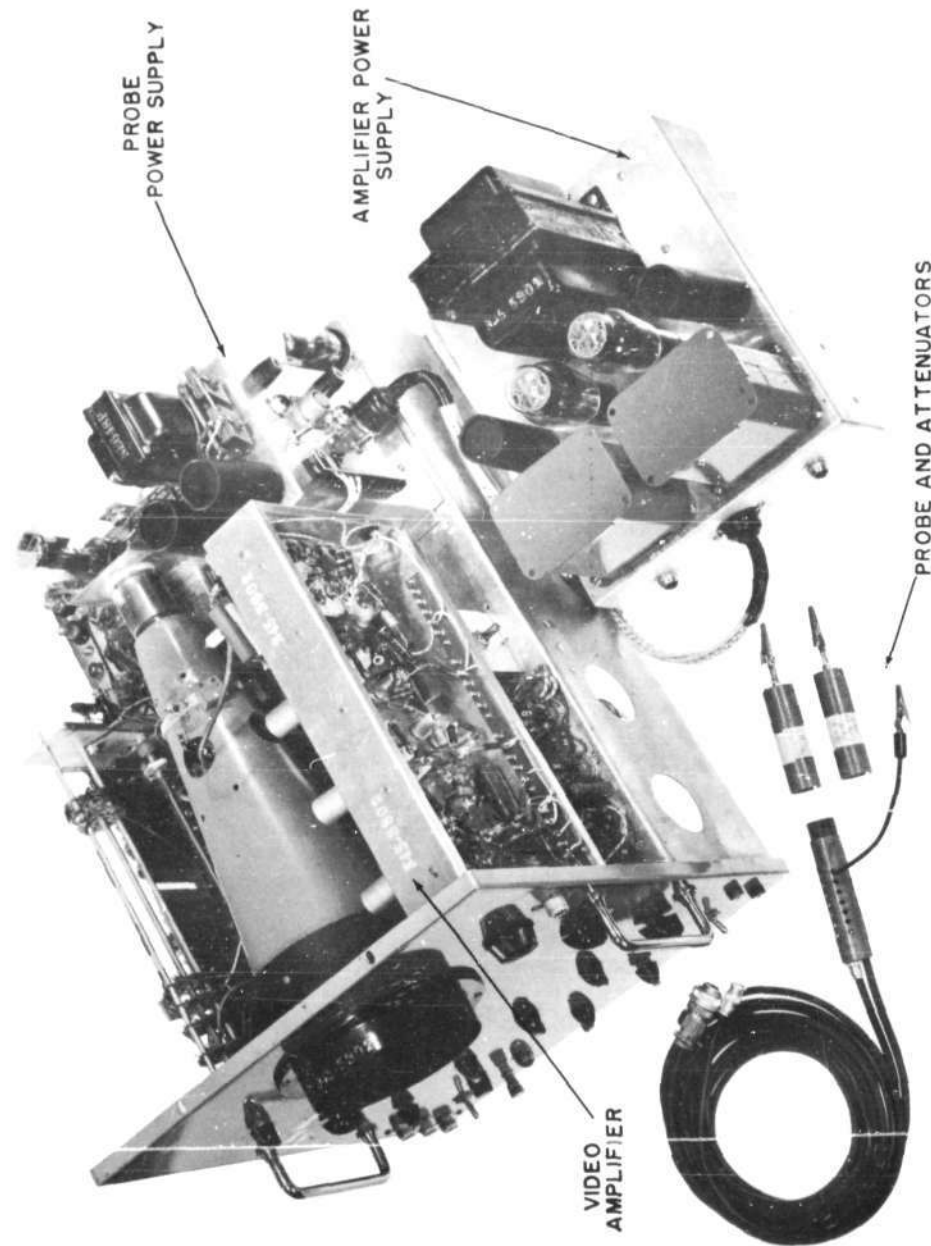
Development and testing of the elements of WWI require constant observation of high-frequency waveforms with a synchroscope. Much trouble has been encountered from stray capacitance and inductance in the leads connecting the synchroscope to the circuit whose waveform is being observed. Furthermore, varying the length of these leads during a series of observations has produced inconsistent measurements. In practically no case can a terminated cable be used for a lead, as the impedance level is so low that the circuit under inspection becomes heavily loaded. An unterminated cable may cause reflections and undesirable oscillations.

Testing with a Cathode-Follower Probe

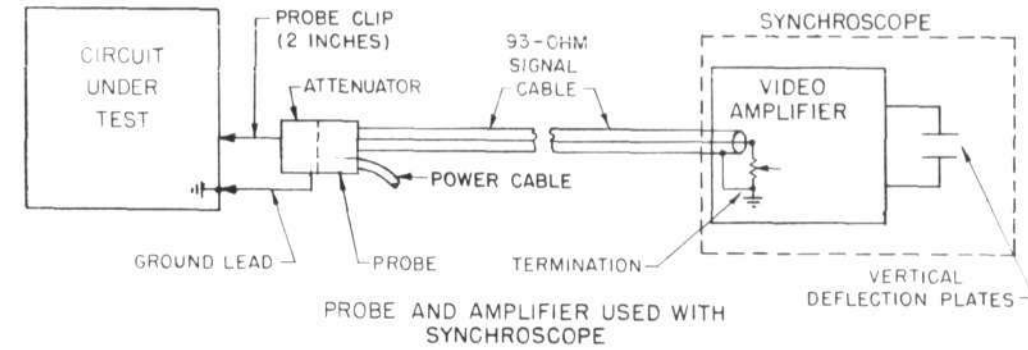
A cathode-follower probe (see the accompanying photograph) was constructed in the laboratory to overcome the problems of cable load on the circuit and variable length of lead from test point to synchroscope. This probe has an input capacitance of 6 to 9 μμf (1/3 that of commercial probes) and a high input impedance (10 megohms). However, its gain is about 1/2 or less, and an attenuator has to be used on the input to reduce the signal to a size that will not be distorted by the probe tube (approximately ± 1 volt).

Need for a Video Amplifier

Use of a probe to avoid inconsistent results from variable loading of circuits meant that high output amplitude had to be sacrificed. This pointed to the need for a video amplifier for the synchroscope; see accompanying block schematic. Because high-frequency signals and gates were to be observed,



VIDEO AMPLIFIER MOUNTED ON SYLVANIA MODEL 5 SYNCHROSCOPE, AND CATHODE-FOLLOWER PROBE



this amplifier had to have a very wide band. None of the commercial synchrosopes used by the Project had adequate amplifiers. It was thus necessary either to improve an existing amplifier or to design a new one.

The primary consideration in selecting a particular type of synchroscope for prototype modification, regardless of the presence or absence of any video amplifier, was scope performance. The Sylvania Model 5 was found best suited for immediate needs because of its fast sweep speed and trigger-delay circuit. This unit has no video amplifier, but its cabinet was found to be adequate for the installation of an amplifier of average size. In addition, it was available in quantity and thus could be made a part of standard test equipment.

An amplifier developed by the MIT Radiation Laboratory for the Sylvania Model 5 synchroscope was improved upon, but was still found to be inadequate (i.e. bandwidth not great enough). Accordingly, a new video amplifier had to be designed. Plans were drawn up for incorporating this amplifier in the Sylvania Model 5, but provisions were made for adapting it to other commercial synchrosopes.

Design Requirements

The design requirements were as follows:

1. Frequency response (between 3-db-down points) of 200 cps to 30 mc.
2. High output voltage: 120 to 180 peak-to-peak volts.
3. A relatively high gain: 150 to 250.

4. Single-ended input, push-pull output.
5. Minimum power consumption.
6. Small enough physical size to permit incorporation into a synchroscope.
7. Low input capacitance.

Construction

The final design of the amplifier constructed to meet these requirements employs 8 vacuum tubes and contains 5 stages: (1) first stage amplifier, (2) push-pull phase inverter, (3) push-pull second stage amplifier, (4) push-pull driver amplifier, (5) final amplifier. Overall dimensions of the unit (including tube space) are 5 x 8 x 14 inches. The accompanying photograph gives an idea of the installation problem which prompted this size and shows the position of the amplifier within the synchroscope.

Performance

To date, three video amplifiers have been installed in Sylvania Model 5 synchrosopes, and eleven new cathode-follower probes constructed. Performance has been most satisfactory. A 100-microsecond gate can be passed with only about 10 percent droop. Pulses of 0.05 microsecond or longer with rise times of at least 0.02 microsecond are amplified linearly, and may now be observed without changes in base-line widths or over-all shapes. Signals having 0.2-volt amplitudes may be measured. Any reasonable length of cable (well over 100 feet) may be used between a cathode-follower

probe and the synchroscope without worry about cable length or reactive effects. In addition, the synchroscope need not be moved around during tests, and the probe may now be used to eliminate variable circuit loading. The amplifier-probe combination is proving to be a highly useful laboratory instrument.

MARGINAL CHECKING — FIVE-DIGIT MULTIPLIER

Reliable operation over extended periods of time is a major requirement for large-scale computing equipment. As an aid in obtaining such operation in WWI, methods have been proposed for discovering marginal operation caused by deteriorated components. These methods are based on operation of the machine with supply voltages or other variables changed from their normal values so as to cause imminent failures to manifest themselves; see Summary Reports 6 and 8. In order to test the usefulness of marginal checking and at the same time obtain data on reliability of circuits of the type used in WWI, a life test will be run on the five-digit multiplier with periodic checks for marginal operation. (The five-digit multiplier is a prototype of the WWI arithmetic element; see Summary Report 3). The number of errors that occur in the cyclic solution of a problem will be recorded during the life test and used as a measure of the system reliability.

System Installed on Five-Digit Multiplier

Marginal checking facilities have been installed on the five-digit multiplier, and the system has undergone considerable testing during the last two months. This system is patterned after that planned for WWI. An amplidyne is used as the variable-voltage source, and an arrangement of manually operated switches permits it to be inserted in series with the d-c supply which is to be varied. Its output, which is manually controlled, covers a range of ±100 volts. Provision is made for independent variation of one electrode voltage for each of various groups of tubes, the tubes being grouped according to their function and also their location in digit columns. The functional groupings are (1) buffer

amplifiers, (2) gate tubes, (3) trigger tubes and cathode followers, (4) flip-flops, zero-side, and (5) flip-flops, one-side. These groups are subdivided according to location as follows: (1) digit panels 1 and 3, (2) digit panels 2 and 4, (3) digit panel 5, and (4) control panel. The screen voltage is the quantity varied for all tubes except trigger tubes and cathode followers, for which both screen and plate voltages are varied simultaneously.

Since the results obtained from a life test on the multiplier depend on the auxiliary equipment used to generate the control pulses as well as on the circuits of the arithmetic element, provision has also been made for varying the supply voltages to this auxiliary equipment. Grouping of tubes according to their functions was not practical with these units because of their type of chassis construction.

Operation of the System

In order to set the limits of voltage variation that can be tolerated in a marginal-checking procedure, it is desirable to set up sequences in which the performance of the circuit under test does not depend on prior operation of other tubes in the same voltage-variation group. This is particularly important since it is desirable to utilize the flip-flop indicator lights as an indication of failures. Such test sequences have been worked out for all flip-flops and a small fraction of the gates and buffer amplifiers. For the other circuits, progressive test sequences are required, and actual failure points can be determined only if their operating margins are narrower than those of circuits used in preceding steps. Tests made to date indicate that this is not a serious disadvantage, however, since a marginal circuit may be isolated from a knowledge of the step in the sequence at which the failure occurs.

Marginal checking of flip-flops has proved quite successful in locating unbalanced circuits. The procedure used is to trigger the flip-flop at about a one-kilocycle rate and then to raise the screen voltage on one of the tubes. Normally, under these conditions, both indicator lights on the flip-flop are illuminated, so that failure of the circuit to trigger will cause one light to be extinguished. By repeating

this process for the other tube and comparing the screen voltage variations that can be tolerated on the two sides, an indication of the degree of balance in the circuit can be obtained. Similar readings taken at both a short restorer period (<10 μs) and a long restorer period (>50 μs) provide some indication as to whether unbalance is due to the tubes or to deteriorated crystal rectifiers.

Marginal checking of gates, buffer amplifiers, trigger tubes, and cathode followers consists merely of decreasing the pertinent electrode voltages. The effect is a decrease in output amplitude in all cases. Since the pulses passed by gate tubes, buffer amplifiers, and trigger tubes are used to trigger specific flip-flops, the extent to which electrode voltages can be lowered is indicated by failure of these flip-flops to trigger. Cathode followers are used to couple between a flip-flop and the suppressor grid of a gate tube. Their performance, therefore, directly affects the output of their associated gate tubes, and failure points are indicated by the action of flip-flops being triggered by pulses passing through these gate tubes. Since trigger tubes and cathode-followers are checked simultaneously, only one failure point can be measured. The circuit causing the failure can be isolated by observing the operation of the two flip-flops involved.

Variation of the supply voltages to the auxiliary equipment produces failures which are less easily analyzed. However, with the aid of a synchroscope, failure points can be located and margins can be set for optimum operation.

Results of Marginal Checking

As a result of tests made with the marginal checking equipment the overall margin of safe operation of the multiplier has been considerably improved. Approximate differentials in voltage that can be tolerated for the different types of circuits are listed below.

Circuit	Differential	Supply Voltage	Percent Variation
Flip-flop	+ 40	+ 120	33
Buffer amplifier	- 90	+ 250	36
Gate tube (6AS6)	- 60	+ 150	40
Gate tube (7AK7)	- 30	+ 90	33
Trigger tube	-100	+ 150	67
Cathode follower	- 50	+ 150	33

The actual differentials obtained depend on the amplitudes of the driving signals used, so that measurements must be made with reference to given input-pulse amplitudes. The amounts of voltage variation required to produce an error in a cyclic problem solution, therefore, may be somewhat different from the normal values listed above because driving pulse amplitudes vary from point to point within the system. For example, the read-in gates which drive flip-flop grids have considerably wider margins than do the carry-to-left gates which drive buffer amplifiers.

In the two-month testing period (components in operation from 2000 to 6000 hours), the following deteriorated components have been located by marginal checking methods.

Component	Number	Total used in Arithmetic Element & Control
Flip-flop tubes	6	46
Crystal rectifiers associated with flip-flops	6	92
Buffer amplifier tubes	2	33
6AS6 gate tubes	7	39

It is hoped that during the life test which is to be started in the near future marginal checking will show trends in component deterioration. This would give valuable information on the manner in which deterioration occurs and permit timely replacements in order to ensure continuous reliable operation of the system.

VISITORS

During December the Laboratory had among its visitors the following:

Rear Admiral T. A. Solberg, Captain W. H. Leahy, Dr. T. J. Killian, Dr. Alan T. Waterman, Dr. Mina Rees, Mr. H. W. Fitzpatrick, Mr. Perry Crawford (on temporary duty with Research and Development Board), Captain J. G. Johns, and Captain A. L. Pleasants, all of ONR.

Vice Admiral Robert B. Carney, Deputy Chief of Naval Operations (Logistics) and Dr. C. B. Tompkins, Mathematics Branch, ONR.

Dr. George E. Kimball of the Operations Evaluation Group to discuss the use of computers in operations evaluation work.

Dr. S. N. Alexander and Mr. H. R. Senf of the National Bureau of Standards, interested especially in our storage tube program.

Professor H. J. Zimmermann of MIT and Mr. G. S. Smith of Melpan, Inc., who were interested in a possible application of storage tubes to a radar signal-discrimination problem.

Mr. Lawrence D. Hindall of Northrup Aircraft Company, who wished to learn about the characteristics of storage tubes.

Mr. C. L. Wright, Jr., of the Stability Section of the Bureau of Ships.

Dr. C. F. Muckenhoupt and R. W. Hart of the Boston Branch, ONR.

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APPENDIX
REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were among those issued during December:

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
SR-13	Summary Report No. 13	20	-	10-48	
R-134	The Five-Digit Multiplier	48	27	12- 3-48	N. H. Taylor
R-145	The Register Panel	12	9	12- 7-48	R. R. Rathbone
E-161	Code for Solution of Simultaneous Equations by Elimination	32	1	11- 4-48	A. Orden
E-165	Summary of Tube Information on Plate Current Deterioration	2	-	11-30-48	N. H. Taylor
E-167	A-C Power in WWI	2	-	12- 8-48	C. W. Watt
E-168	D-C Coupled Flip-Flops	4	3	12-17-48	C. A. Rowland
M-704	Thyratron Control of A. C. Spot Welder for Storage Tube Assembly	2	1	11-23-48	H. Klemperer
M-705	End Carry for Point Off	1	-	11-24-48	R. P. Mayer G. G. Hoberg
M-709	Master's Thesis Research Proposal: A Low-Speed Analogue for Analysis of Flip-Flops	5	2	11-29-48	J. M. Hunt
M-710	New Orders in WWI; Effect on Construction	1	-	11-26-48	H. Fahnestock
M-713	Pulse Transformers on Whirlwind Panels	1	-	11-29-48	G. G. Hoberg
M-714	Storage Tube 53: Construction and Processing	2	-	11-29-48	M. Florencourt
M-718	GT08 Check Register	1	-	12- 1-48	J. M. Salzer
M-720	Synchronization with the Synchronizer	3	1	12- 2-48	J. M. Salzer
M-722	Special Clear and Computer Complement	2	-	12- 2-48	J. M. Salzer
M-724	Storage Tube 53: Test Results	3	-	12- 2-48	M. Florencourt
M-725	Sylvania Tracings, Delivery to MIT	1	-	12- 7-48	H. Fahnestock
M-726	The Dispersion Action of the Collector	1	-	12- 6-48	J. S. Rochefort
M-727	Storage Tube 47	1	-	12- 7-48	M. Florencourt
M-730	Bi-Weekly Report, Part I, 12-10-48	14	-	12-10-48	
M-731	Bi-Weekly Report, Part II, 12-10-48	17	-	12-10-48	
M-733	Meeting at Eastman Kodak Company	2	-	12-13-48	J. A. O'Brien
M-734	Progress Report: A Dual-Triode Capacitively Coupled Flip-Flop	2	2	12-10-48	M. H. Hayes
M-743	Bi-Weekly Report, Part I, 12-24-48	11	-	12-24-48	
M-744	Bi-Weekly Report, Part II, 12-24-48	12	-	12-24-48	
C-74-1	Code for the Square Root	3	-	12- 3-48	P. Franklin
C-75	Meeting on December 7; Conference Note C-74	2	-	12- 2-48	W. G. Welchman

<u>No.</u>		<u>No. of Pages</u>	<u>No. of Drwgs.</u>	<u>Date</u>	<u>Author</u>
C-76	Solution of Problems in Conference Note C-73	3	-	12- 2-48	W. G. Welchman
C-77	Codes for the Square Root II	6	-	12- 6-48	P. Franklin
C-78	Problems for December 7 to 13	3	-	12- 7-48	E. Reich
C-79	Ship Control Problem	2	-	12- 7-48	W. G. Welchman
C-80	Ship Control Problem	3	-	12-10-48	W. G. Welchman
C-82	Problem for December 21, 1948	1	-	12-15-48	W. G. Welchman

