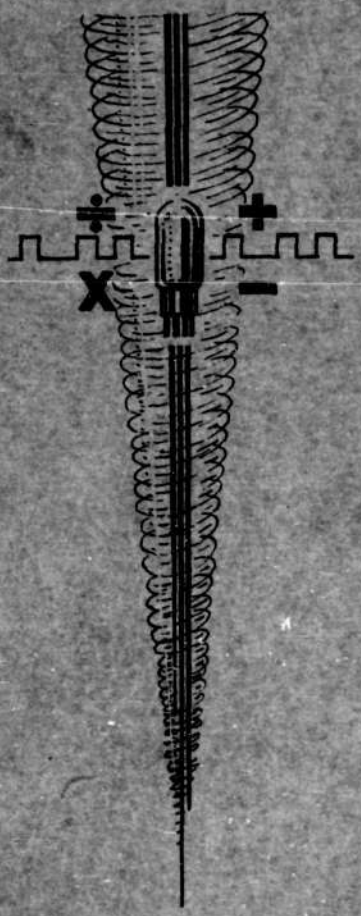

PROJECT WHIRLWIND

Contract N5ori60

SUMMARY REPORT NO. 2

VOLUME 19

TEST EQUIPMENT AND MISCELLANEOUS CIRCUITS

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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SPECIAL DEVICES CENTER

PROJECT WHIRLWIND
Summary Report No. 2
November, 1947

TEST EQUIPMENT AND MISCELLANEOUS CIRCUITS

Volume 19 of 22 Volumes

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

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INTRODUCTION

Basic test equipment for research in computer circuits must include a synchroscope and a pulse generator. Because of the high pulse-repetition frequency and short pulse length used in the Whirlwind computers, a synchroscope with a very fast sweep is necessary. The Model 5 synchroscope has been used more than any other scope in the Whirlwind program and is shown in PB-295, together with a camera for photographing wave forms. A sweep calibrator is described in E-58. The most widely used test equipment designed by Project Whirlwind has included a gas-tube pulse generator for generation of short pulses at low pulse repetition frequencies and a high-frequency clock-pulse generator. The high-frequency (1 to 6 Mc) clock-pulse generator is very similar to the master clock that will be used in Whirlwind I. It is described in E-48 and shown in photographs PB-258, PB-259, and PB-260.

In order to use the a-c coupling scheme, a source of pairs of pulses spaced approximately ten microseconds apart is necessary. This generator, called a restorer-pulse generator, is described in E-52 and M-114 and is shown in PB-255, PB-256, and PB-257. A similar generator will be used in Whirlwind I. A general-purpose gate and delayed-trigger generator is described in E-38. An early clock-pulse generator, designed to work with a low-frequency serial-type adder is described in E-89. A tube tester designed and built in this laboratory for obtaining static and pulse characteristics is shown in PB-272.

An investigation of gate circuits made early in the program to evaluate the methods available for gating is described in E-109.

An evaluation of various methods of generating pulses on the low-impedance digit-transfer bus is contained in E-121. An analysis of the problem of simultaneously pulsing the grids of sixteen tubes in sixteen different racks is presented in E-89.

A method of terminating a low-impedance cable for point to point transmission is described in E-59. The use of pulse transformers for step-down at the transmitting end of the cable and a step-up at the receiving end is described in E-60.

A high-speed step counter for use with the 5-digit multiplier is described in M-126. The step counter for Whirlwind I will have five instead of three stages, but will be very similar in other respects to the counter described.

The time-pulse distributor described in E-45 is now obsolete. The time-pulse distributor planned for Whirlwind I will employ an eight-position switch and a three-stage binary counter instead of the eight-stage ring counter described in E-45.

In order to begin construction of prototype units for Whirlwind I as early as possible and to transfer the design of the various parts of the computer to Sylvania, preliminary designs of some units have been transmitted to Sylvania along with an explanation of the status of the design. The design of the register panel, which includes the check register, the program register, and the program counter, and the design of the flip-flop storage have been transferred to Sylvania in this manner. E-55, M-105, E-63, include lists of drawings of these preliminary designs and also a discussion of which parts may be considered definite and which parts are subject to change.

Assembly drawings of the variable frequency clock pulse generator and the restorer pulse generator are included in Vol. 1B.

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MEMORANDUM NO. M-38

TO: J. W. Forrester, and Patrick Youtz

6345
Page 1 of 8 pages

FROM: J. R. Macdonald

SUBJECT: Tests on Anodized Aluminum Surfaces

REF: 1JRM73-87, 2AJT28-37

DATE: November 27, 1946

Graphs
A-38139-G
A-38140-G
A-38141-G
A-38142-G
A-38143-G
A-38144-G
A-38145-G

A - Subject and Object of Tests

These tests were carried out on 12 anodized aluminum samples which had been treated differently after the anodizing process, with the view of determining pertinent electrical characteristics of the samples for comparison of the effects of the different treatments.

B - Procedure and Apparatus for Tests

1) An aluminum holder with a hole of .40 cm^2 area at one end was used to hold a drop of mercury at a given position on the anodized surface.

2) Using mercury in the above holder as an electrode, measurements were made with the Q meter which led to the value of capacitance/unit area, Q, and shunt resistance of the surfaces at different frequencies. In all cases where it was possible in this and succeeding tests, three measurements were made on the obverse of each sample and one on the reverse, in order to give a measure of the irregularity of the surface.

3) A low loss breadboard for clamping mercury holder and sample in a definite, firm relative position was constructed using a 1" polystyrene rod. A variable voltage source was connected across the mercury and sample, and the current and voltage tabulated for voltages ranging from 2 to 550 volts, in order to measure the breakdown voltage of the samples.

4) Using a mixture of chromic and phosphoric acids the aluminum oxide was dissolved from a portion of each side of each sample. Micrometer measurements before and after the removal of the surface film determined its thickness. From this thickness it was possible to compute the capacitance/unit area of each sample in terms of its dielectric constant. Comparing with the values of capacitance/unit area measured on the Q meter, it was possible to compute average values of the dielectric constant for each sample.

C - Comparison of Results for the Different Samples

1) The overall average results are summarized as follows:

   a. Average capacitance/unit area = 300 $\mu\mu f/cm^2$

   b. Average dielectric constant = 5

   c. Average minimum breakdown voltage = 300 volts

   d. Average d.c. resistance at breakdown = 3.5 megohms

   e. Average Q at 1 MC = 50

   f. Average shunt resistance at 1 MC = 75 kilo-ohms

2) Individual results are tabulated in Table I.

3) In Table II ratings are given to each sample on the basis of maximum breakdown voltage and minimum variation over the surface in R, C, and Q, with a rating of 1 indicating the best sample for each criteria. From these ratings an overall rating is computed, which is a measure of the uniformity of the surface.

The following tentative conclusions may be drawn from the ratings of the different groups(see Memorandum No. M-36, for treatment of each group).

1) Temperatures of the order of 10 to 15°C during anodizing preferable to 20°C.

2) Boiling samples in distilled water produces the most uniform surface.

No conclusions concerning the treatment which produces the surface with best electrical characteristics (highest breakdown voltage, highest C and Q) can be drawn because of the lack of uniformity of the surfaces. Three measurements on one side is not enough to insure a good approximate value of the maximum C, Q, and breakdown voltage. The quantities given in Table I are not accurate for some of the following reasons:

1) Variation in thickness, dielectric constant, and resistance over the surface of a sample. See Graph A-38142-C, showing variation of resistance with position.

2) Variation of breakdown voltage with position of electrode on surface. See Graph A-38142-C.

3) Pronounced dielectric absorption in the anodized layer; this causes the rate of change of applied d.c. voltage and the

TABLE I

Sample No.	Max.+Min. Empirical C μμf	Theoretical C K = 5 μμf	μμf	d Obverse Reverse $In. \times 10^{-4}$	Max Q	Max Shunt Resistance at 1 MC a.c. KΩ.	Shunt Resis at Breakdown Voltage d.c. MΩ.	Max +Min. Breakdown Voltage
1	125	100	125	7	63	80	.11	460
			K=6.3	9			6.9	300
2	159	174	150	4	17	21	1.33	460
	140		K=4.3	5		19	2.00	240
3	150	139	130	5	16	23	1.66	500
	87		K=4.7	5		19	.82	390
4	100	174	100	4	19	30	5.3	475
			K=2.9	7			.5	300
5	127	139	120	5	100	152	6.0	300
	105		K=4.3	6		205	6.0	40
	86					164		
6	129	174	115	4	100	169	4.1	250
	101		K=3.3	8		62	50	25
7	155	100	155	7	27	28	1.43	500
			K=7.8	5			.6	300
8	138	174	138	4	42	25	2.0	300
	137		K=4.0	6		49	.75	300
9	160	100	137	7	80	19	10.4	520
	114		K=6.9	6		150	1.33	400
10	115	116	110	6	70	76	5.0	500
	105		K=4.7	6		140	4	400
11	148	116	125	6	35	42	2.9	550
	102		K=5.4	7		55	1.33	400
12	171	139	156	5	20	25	1.75	525
	142		K=5.6	5		19	1.19	400

TABLE II

Sample No.	Max. Voltage	Minimum Variation in R	Minimum Variation in C	Minimum Variation in Q	Sum	Overall Rating
1	6	10	2	10	28	7
2	7	2	4	2	15	2
3	4	2	6	5	17	3
4	5	5	10	9	29	8
5	8	1	1	1	11	1
6	9	6	9	5	29	8
7	4	4	7	4	19	4
8	4	4	6	3	17	3
9	3	7	8	6	24	6
10	4	3	5	4	16	3
11	1	3	8	5	17	3
12	2	2	3	3	10	1

a) Overall Sums for Rating:

Samples			Rating
1 + 2 + 3 + 4	=	20	3
5 + 6 + 7 + 8	=	16	2
9 +10 +11 +12	=	13	1
1 + 5 + 9	=	14	3
2 + 7 +11	=	9	2
3 + 8 +12	=	7	1
4 + 6 +10	=	19	4

b) Sums of Voltage Ratings

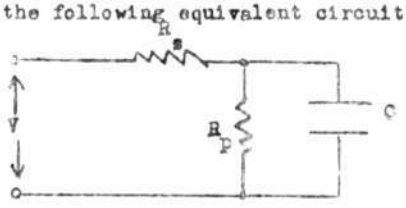
Samples			Rating
1 + 2 + 3 + 4	=	23	3
5 + 6 + 7 + 8	=	25	3
9 +10 +11 +12	=	10	1
1 + 5 + 9	=	13	2
2 + 7 +11	=	12	2
3 + 8 +12	=	10	1
4 + 6 +10	=	18	4

time a given voltage is applied to both exert a very marked effect upon the results of the d.c. measurements. The history of the sample with regard to time and value of past applied voltage must be taken into account to obtain measurements at all meaningful. In these preliminary tests it was thought accurate enough to make most of the d.c. measurements at 25-volt steps, with a minute wait at each step to establish equilibrium. From Graph No. A-38143-G, it would seem that more than a minute would be needed for equilibrium. However, these curves were obtained by applying the final voltage instantaneously, not increasing from zero in small increments and, hence, are not applicable here.

4) Absorption of moisture from the air by the samples. The initial tests were made after the samples had been exposed to the atmosphere for some time. Later, a dessicator was used and the samples kept therein except during the tests themselves. Results were more consistent although the preferable procedure would be to carry out the measurements with the samples in a dessicator at all times (assuming tests made in air). It was noted that after samples had been exposed to the outside atmosphere for some time, the application of a d.c. voltage produced a current which fell off tremendously but slowly. This effect cannot be explained wholly by polarization current, but is probably caused by the current heating and drying the spot being measured.

D - Detailed Discussion of Results for a Given Sample

1) For d.c. the following equivalent circuit is applicable.



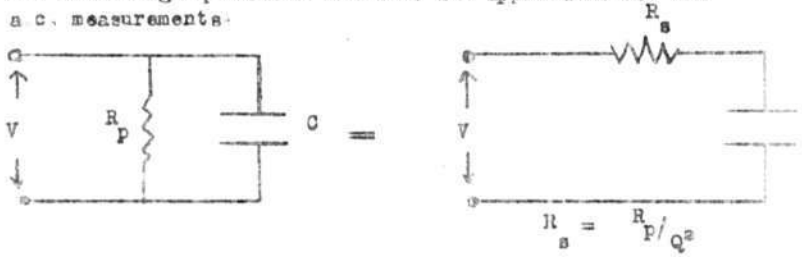
From measurements of the initial charging current at V = 100 volts, it was found that $R_s \cong 100$ KΩ, and from measurements of the steady current when equilibrium was attained $R_p \cong 7$MΩ, for sample 5. Thus, $R = R_p + R_s \approx R_p$.

As will be seen from Graphs Nos. A-38139-G and A-38140-G, R is a function of the applied voltage. The value of R also depends on the point of measurement, and upon the near past voltage history of that point. The breakdown voltage also varies with position. An interesting healing

phenomena was observed - it being found that if the breakdown current did not flow more than two or three seconds, the surface would heal itself (within 1/2 sec.) and its resistance would again become high. As Graph No. A-38141-G shows, however, the voltage of succeeding breakdowns at the same spot decreases in general, being roughly inversely proportional to the number of breakdowns and proportional to the time which elapses between successive breakdowns. If the breakdown current (limited to less than .5 ma) is allowed to flow for more than a few seconds, the surface is permanently burned and broken down. The resistance after permanent breakdown was measured as about 1 ohm.

Various anomalous effects were observed in these d.c. measurements. For instance: the portion a-b on Graph No. A-38142-G where the sample exhibits a constant current characteristic. These effects cannot be explained adequately on the basis of the foregoing tests. In order to do this, tests should be made in which the many variables involved were more carefully controlled and measured.

2) The following equivalent circuits are applicable for the a.c. measurements.



at 1 MC $C = 121$ μμf, $R_p = 150$ KΩ $R_s = 11$ Ω Sample No. 5

at 10 MC $C = 130$ μμf, $R_p = 5.9$ KΩ $R_s = 2.5$ Ω

See Graph No. A-38144-G which gives C, Q, and R_p as functions of frequency. Graph No. A-38145-G shows R_p extrapolated to 100 cycles per second, practically zero frequency. This is far too long an extrapolation to be accurate, but it at least gives one an idea of the order of magnitude of R_p. As shown on this Graph, R_p = 7 megohms at 100 cps. A study of the curve involved in the extrapolation shows that R_p at 100 cps will be between the values of 5 to about 400 MΩ. The point R_p = 7 MΩ at f = 100 cps is

plotted and is within this range. This value of R_p was obtained from d.c. measurements at 100V. However, the value of R_p is a function of the voltage applied. Within the Q range of samples being measured the a.c. voltage applied to the sample is of the order of 1 volt. Thus, the graph should probably be extrapolated to 200 ro 300 megohms, at zero frequency for this low voltage.

In the appendix the force with which the mercury electrode is attracted to the surface of the sample at 500 volts is computed. This force is about 1/3 pound, and is, hence, not negligible compared to the weight of the mercury. The force on the drop of mercury due to surface tension and that of gravity are of the same order of magnitude, whereas that due to electrostatic attraction is fifty times greater than the weight. Thus, a large voltage causes the mercury to flatten out considerably and to penetrate into the pores of the surface of the sample. It is interesting to note that the flattening remains, even after the voltage is removed, which indicates that the mercury is well distributed in the surface irregularities. Microscopic examination(and even visual examination) confirms this conclusion. Considerably poorer contact was achieved with flat metal electrodes. Because of these effects, it is impossible to decide how closely results obtained with the mercury electrode will apply to measurements using electron beams.

E - Recommendations for Future Tests

1) Machine samples to very fine smoothness before anodizing, to minimize surface varintions.

2) Use an anodizing bath and electrode of physical conformation such that the current density over the face of each sample is constant.

3) Process at least two samples similarly after anodizing, in order that a meaningful average of succeeding measurements can be obtained.

4) If measurements are not carried out in a vacuum, let them be made in a dessicator held to a constant temperature.

5) Make measurements using mercury anode, silver or gold plate anode, and electron beams if feasible.

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APPENDIX

A) Computation of electrostatic force on mercury

Approx' $F = \frac{CV^2}{2d}$ newtons (d in meters)

C = 121 μμf

V = 500 volts

$d = \frac{4}{10,000}^{in} = 1.016 \times 10^{-5}$ meters

$F = \frac{121 \times 10^{-12} \times 25 \times 10^4 \times 10^5}{2 \times 1.016} = 1.5$ newtons

= .34 pounds

B) Weight of mercury

Assume central circular section of spherical

drop = .40 cm^3 r = .357 cm.

Volume = $\frac{4}{3}\pi r^3$ = .2 cm^3 e = density = 13.55 g_{m/cm^3}

F = W = Mg = 980.4 x .2 x 13.55 = 2660 dynes

= .0266 newtons

$\frac{F \text{ voltage}}{\text{weight}} = \frac{1.5}{.026} = 56$

C) Surface tension $P = \frac{3T}{r}$ $\frac{\text{dynes}}{cM^2}$ T = 465 $dynes/_{cm}$

P x A = Force = $\frac{2TA}{r} = \frac{2 \times 465 \times .4x4}{.357}$ = 4160 dynes

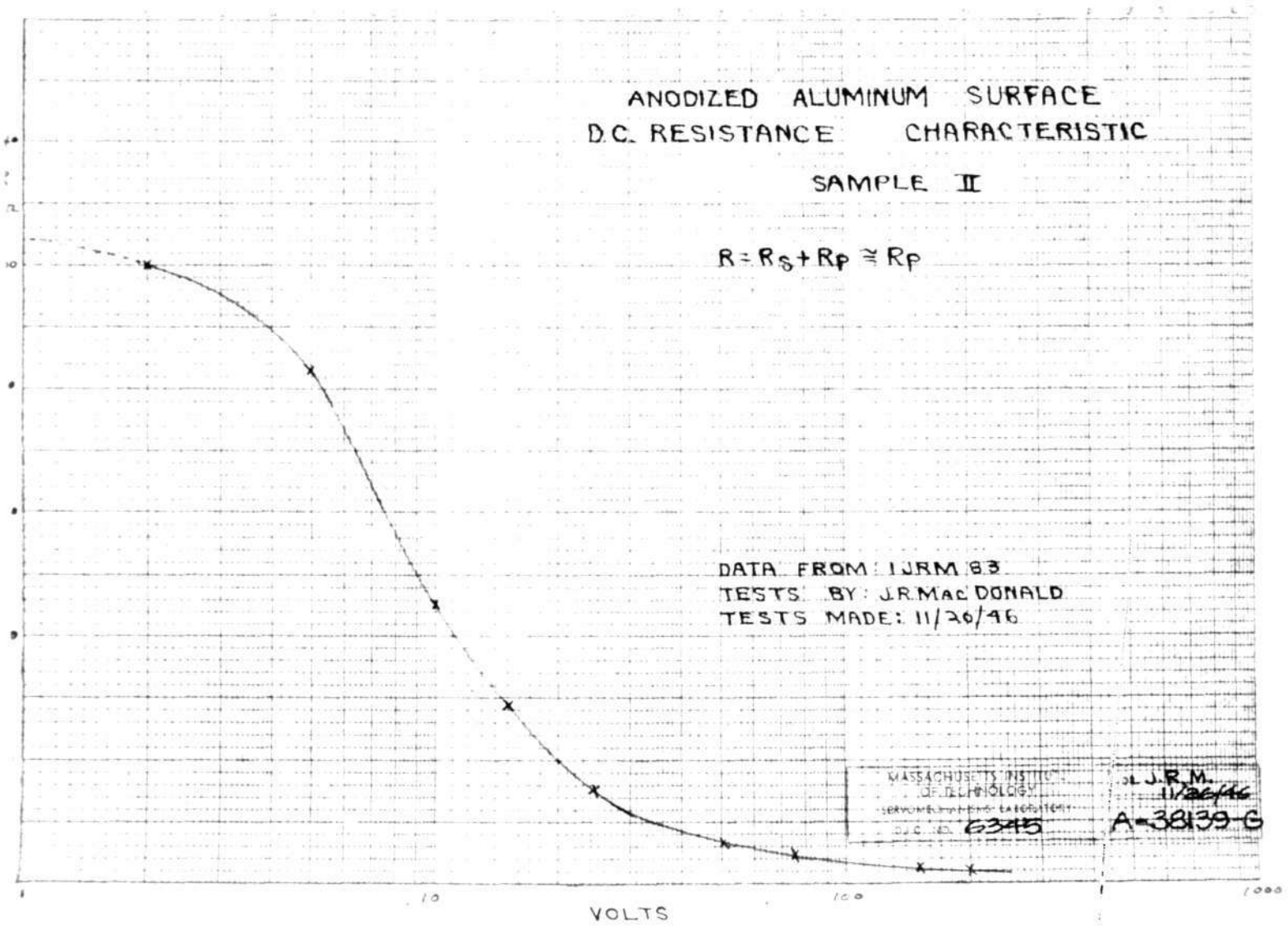
= .042 newtons

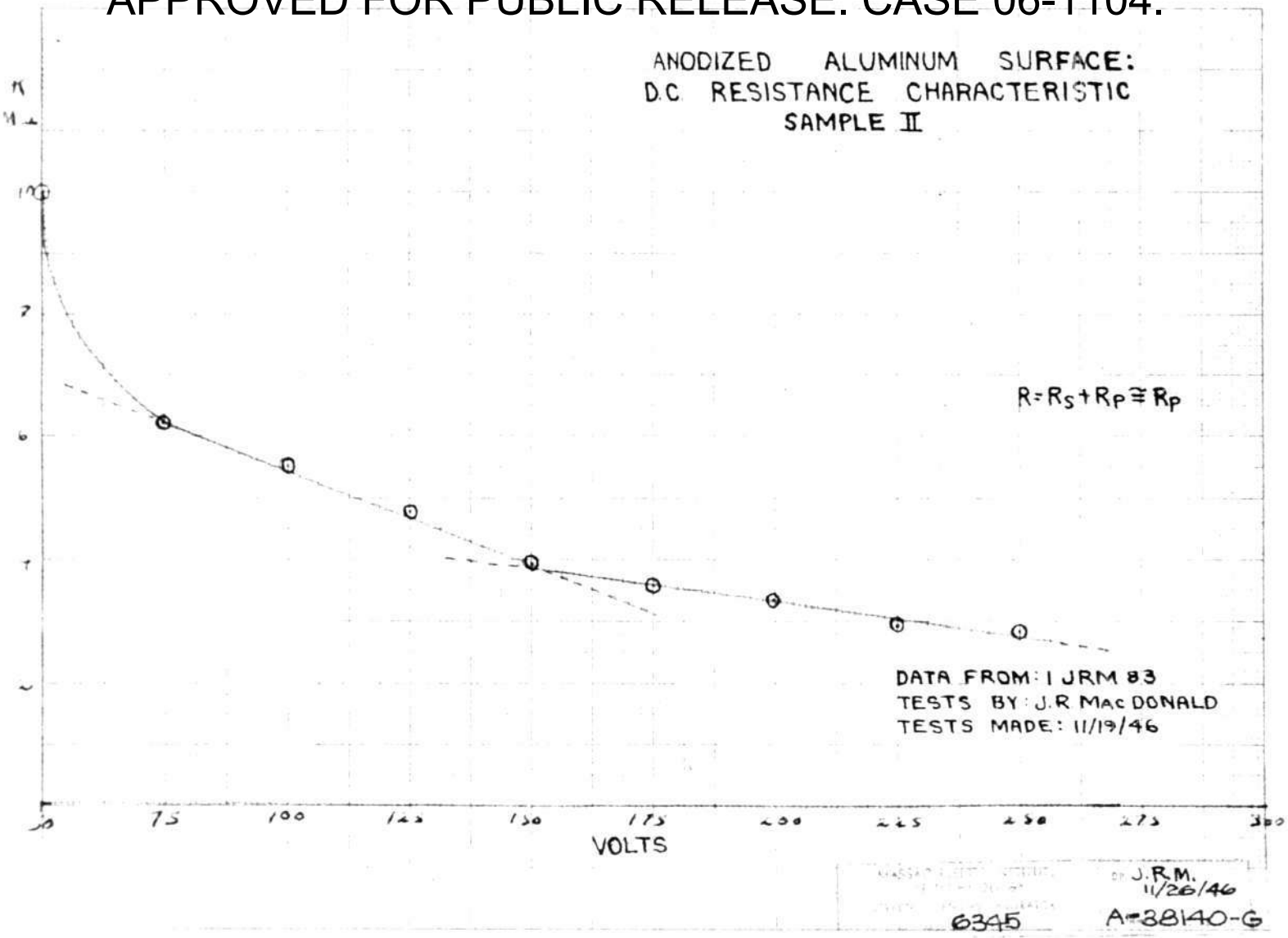
A = Spherical surface area in this formula.

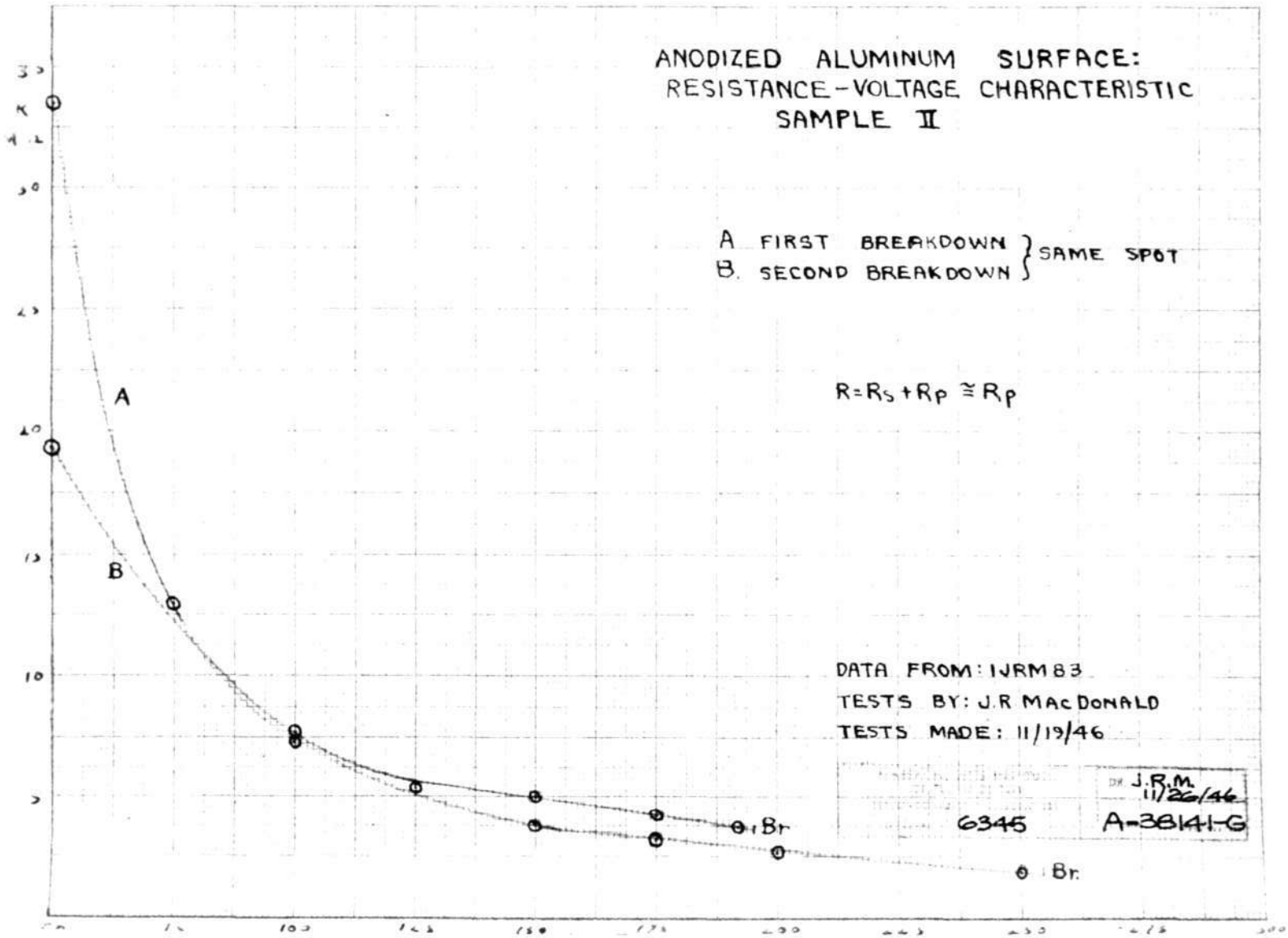
D) Force due to vapor pressure A = .40 cm^3

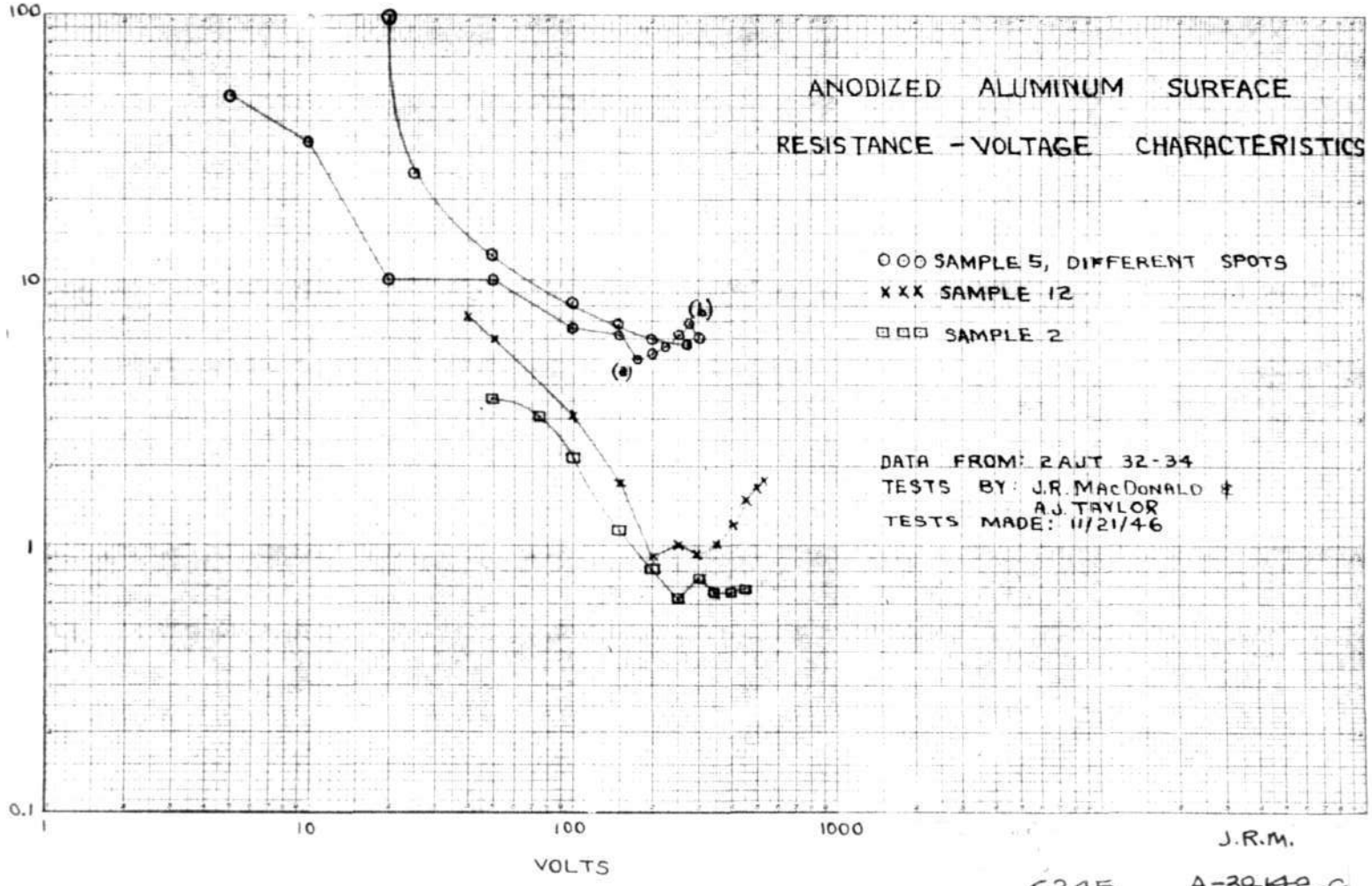
= .0015 $mr/_{Hg}$ x A = .80 dynes = 8×10^{-6} newtons

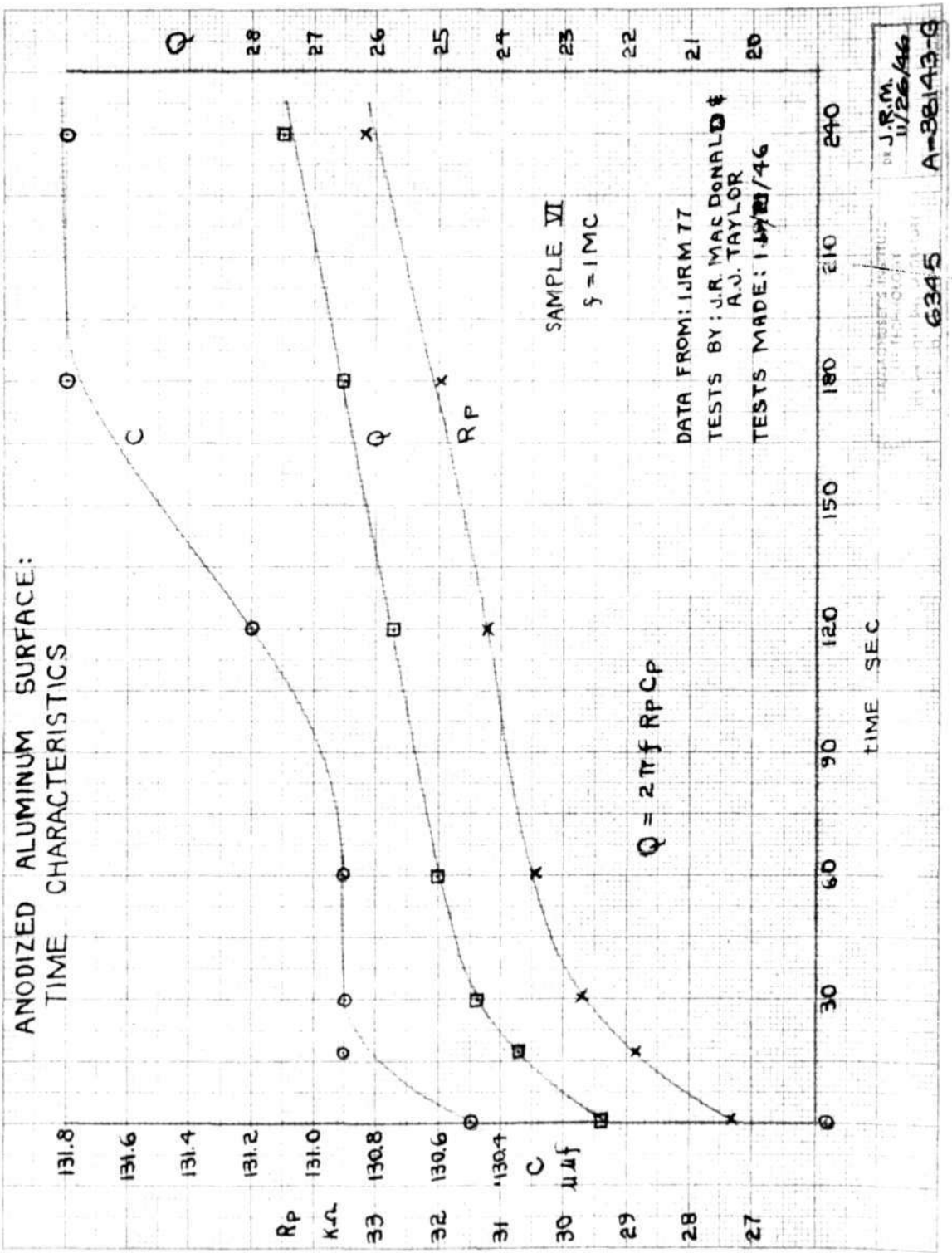
A = bottom area of drop = .40 cm^3

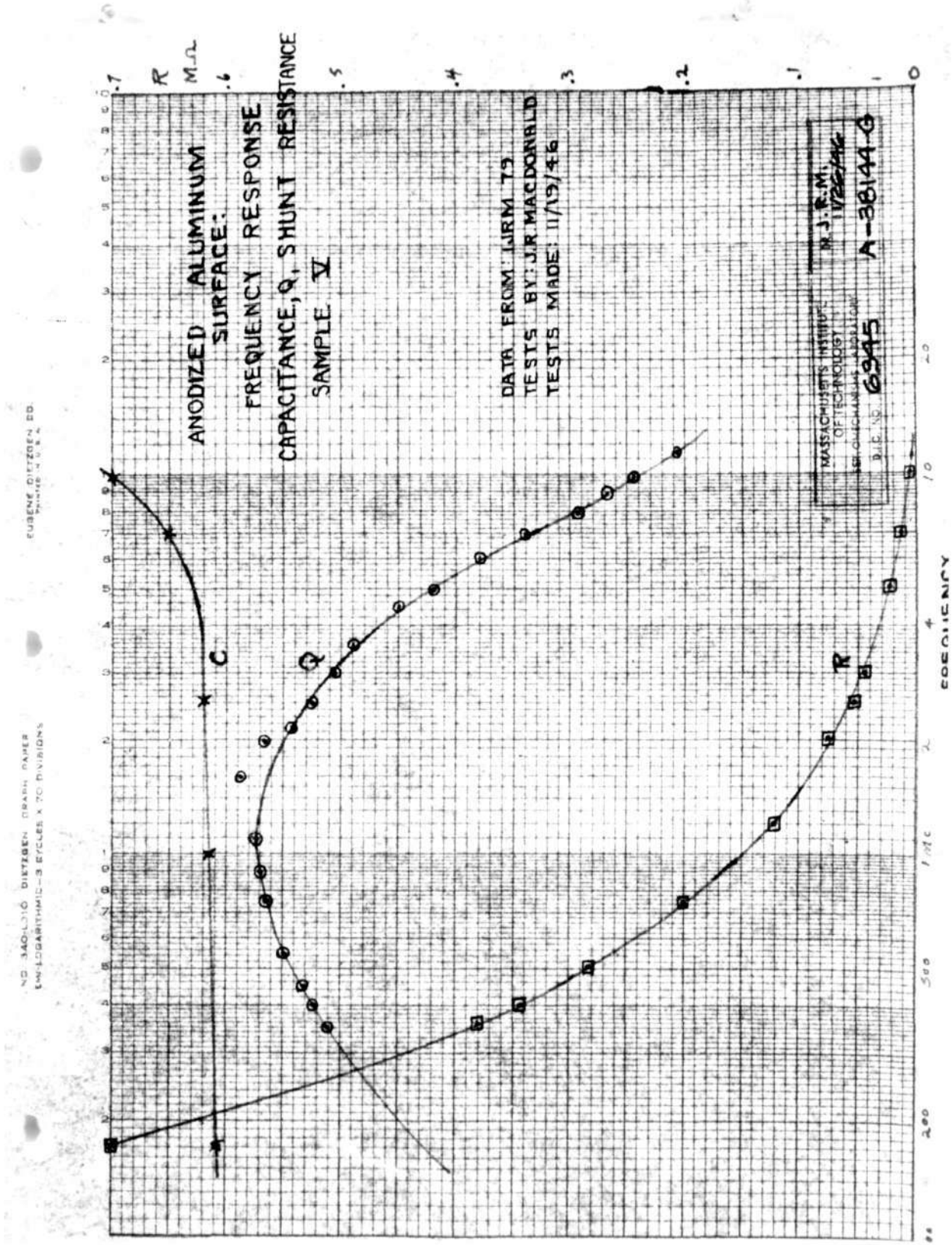


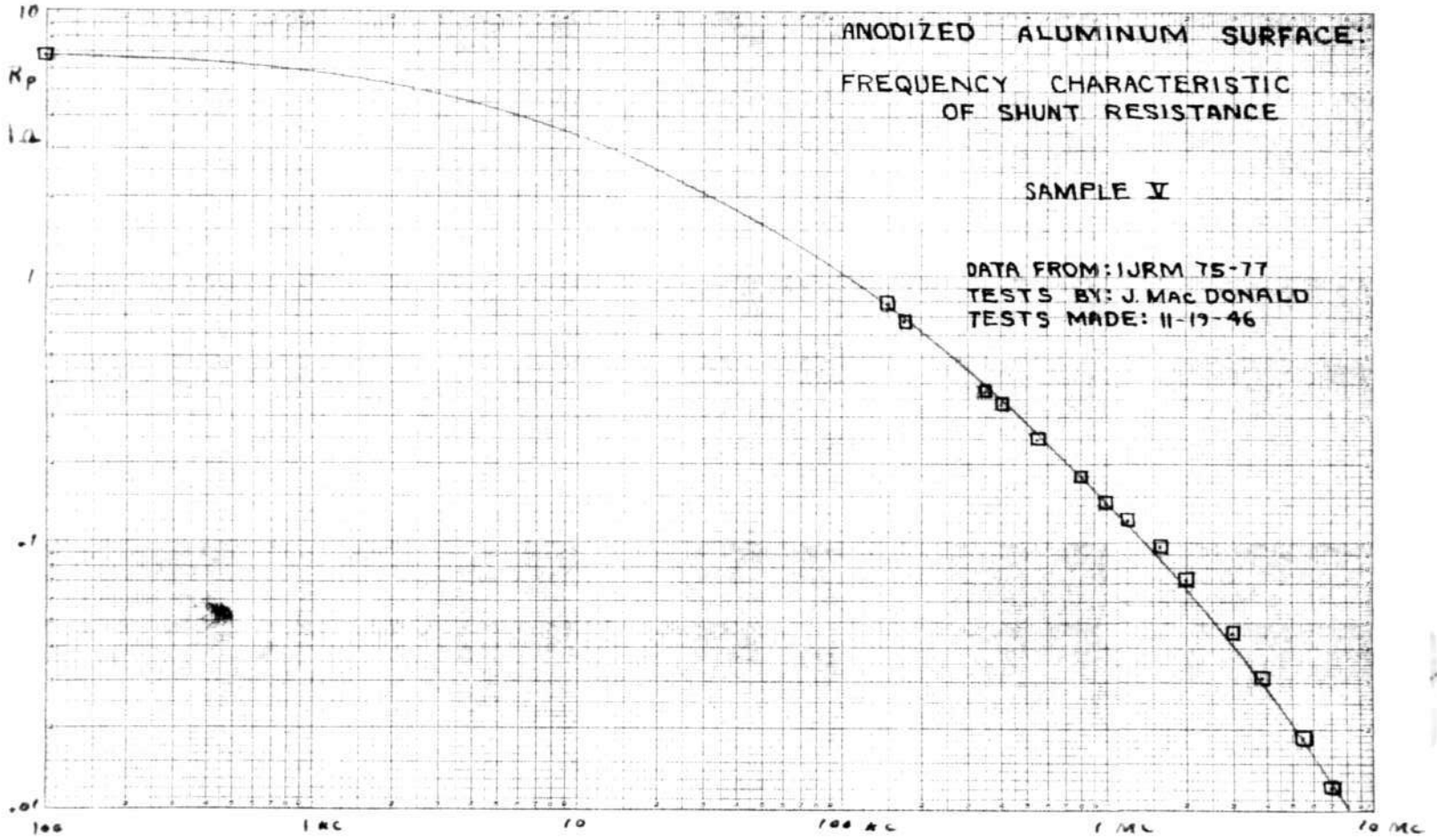












J.R.M.
11/26/46

6345 A-38145-G

ENGINEERING NOTES NO. E-48

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: 6345 Engineers — 6345

FROM: Harry Kenosian — Page 1 of 2 pages

SUBJECT: Variable Frequency Clock Pulse Generator — Drawings: C-30607

DATE: July 18, 1947

General Description

The variable frequency clock pulse generator provides pulses at an impedance of 46.5 ohms which are .05 μs wide at the baseline and the P.R.F. is continuously variable from 0.9 to 6 megacycles. The pulse amplitude starts dropping off at about 4 megacycles. The actual amplitude depends on the emission characteristics of the 3E29 output amplifier. However, the output amplitude is usually between 50-70 volts. An amplitude control is provided so that the pulse amplitude can be reduced to zero volts. It is necessary that the output impedance be matched to 46.5 ohms; otherwise, the shape of the output pulse will be affected. This condition is necessitated by the fact that the output transformer must see its characteristic impedance. The "Synchronizing Output" jack is designed to work directly into the input of a General Electric Decade Counter.

Circuit

The circuit, Drawing C-30607, consists of a variable frequency sine wave oscillator which is fed into a 6L6G R-L-C peaker. The output of the 6L6G peaker is fed to a 6L6G cathode follower which drives a 3E29 power amplifier. 6L6's were used in this circuit rather than 6Y6's because the plate and screen dissipation of the 6L6 is higher, and the 6L6 was found to be less prone to parasitics by virtue of its lower mutual conductance.

Electrode dissipations are reduced to a minimum by keeping all stages operating normally off. Signal bias is used in the oscillator and R-L-C peaker circuit. The 3E29 bias is controlled by means of a potentiometer which is the amplitude control.

The output pulses are reduced in width somewhat at reduced amplitudes so that if it is absolutely necessary that the pulse width be maintained, then an attenuator can be used between the cable and the circuit to be tested.

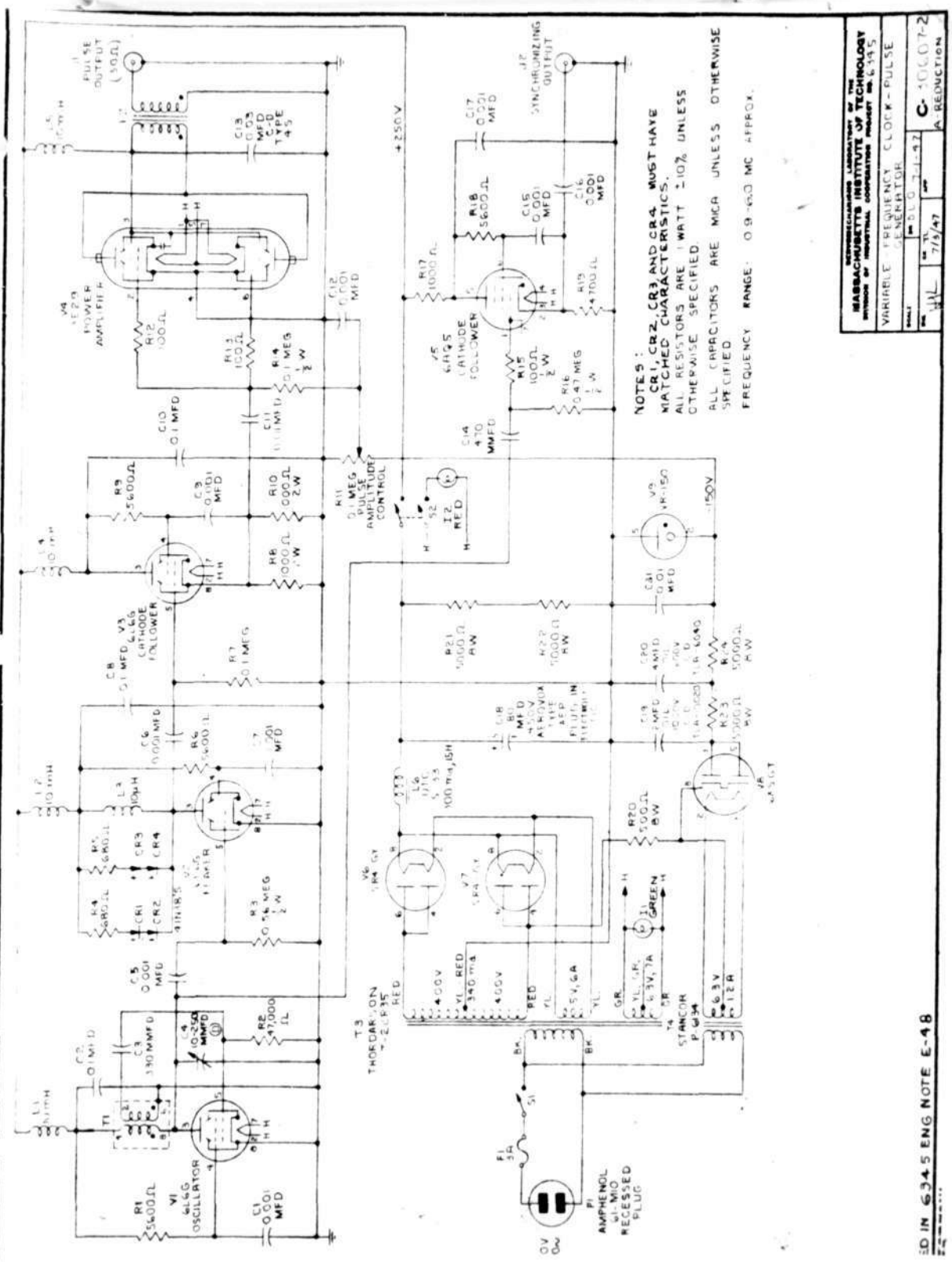
Plug-in coils are provided to change the frequency range. There are three coils for each unit. The spare coils are mounted on a small raised shelf on top of the chassis. These coils cover the range from 0.9 m.c. to 6 megacycles.

If it is found necessary to work under the chassis, caution should be exercised when working on the circuits associated with the oscillator and peaker. The radio frequency voltages associated with these circuits are quite high, consequently painful r-f burns will result if any ungrounded point be touched.

Synchronizing voltage is obtained from the output of a 6AQ5 cathode follower whose input is coupled to the output of the sine wave oscillator. The synchronizing pulses are approximately half-sine waves. The synchronizing voltage was designed to work into a G.R. Decade Counter, whose output pulse can be used to trigger a synchroscope. If sharper pulses are needed for synchronizing, these may be obtained from the generator output. However, these pulses will be subject to variation in amplitude as the amplitude control is varied. The advantage of using the synchronizing voltage provided on the generator is that this voltage is independent of the output circuit and can be loaded in any way without affecting the output circuit.

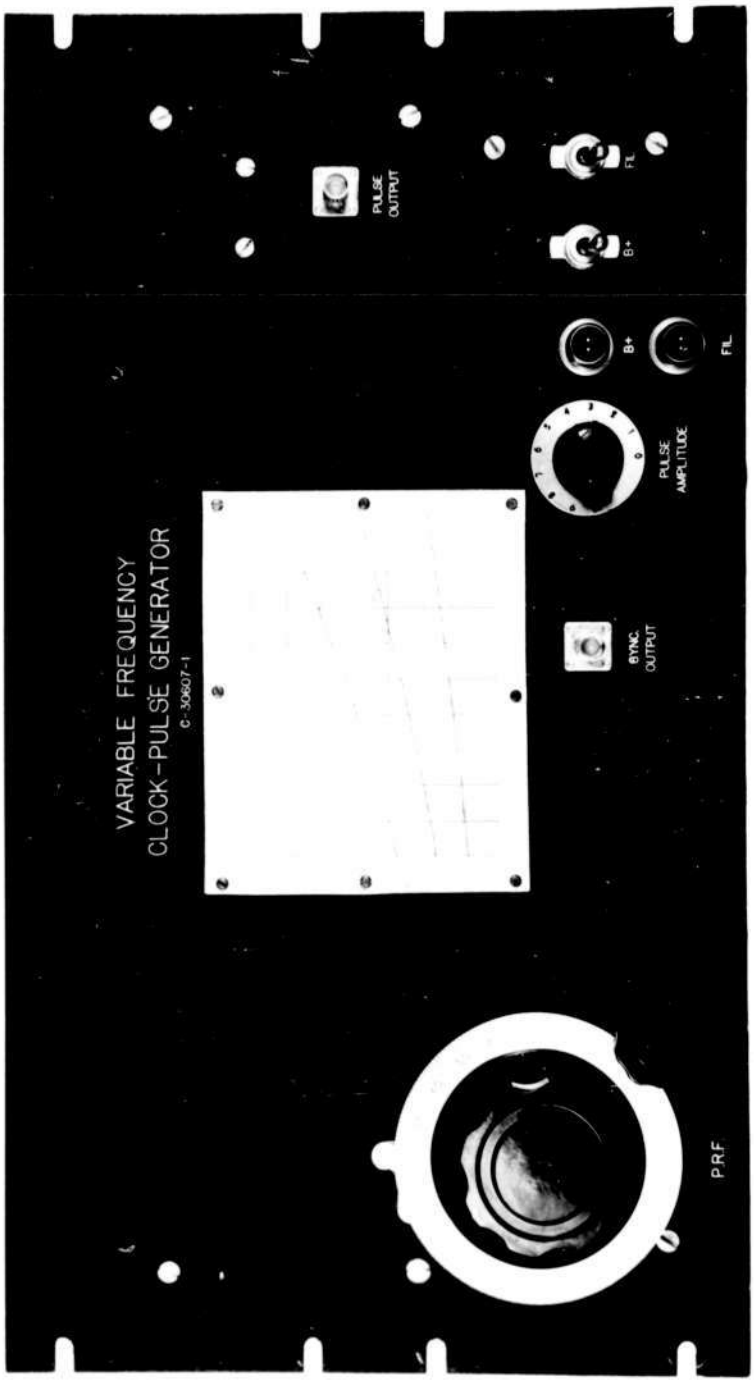
Harry Kerosian
Harry Kerosian

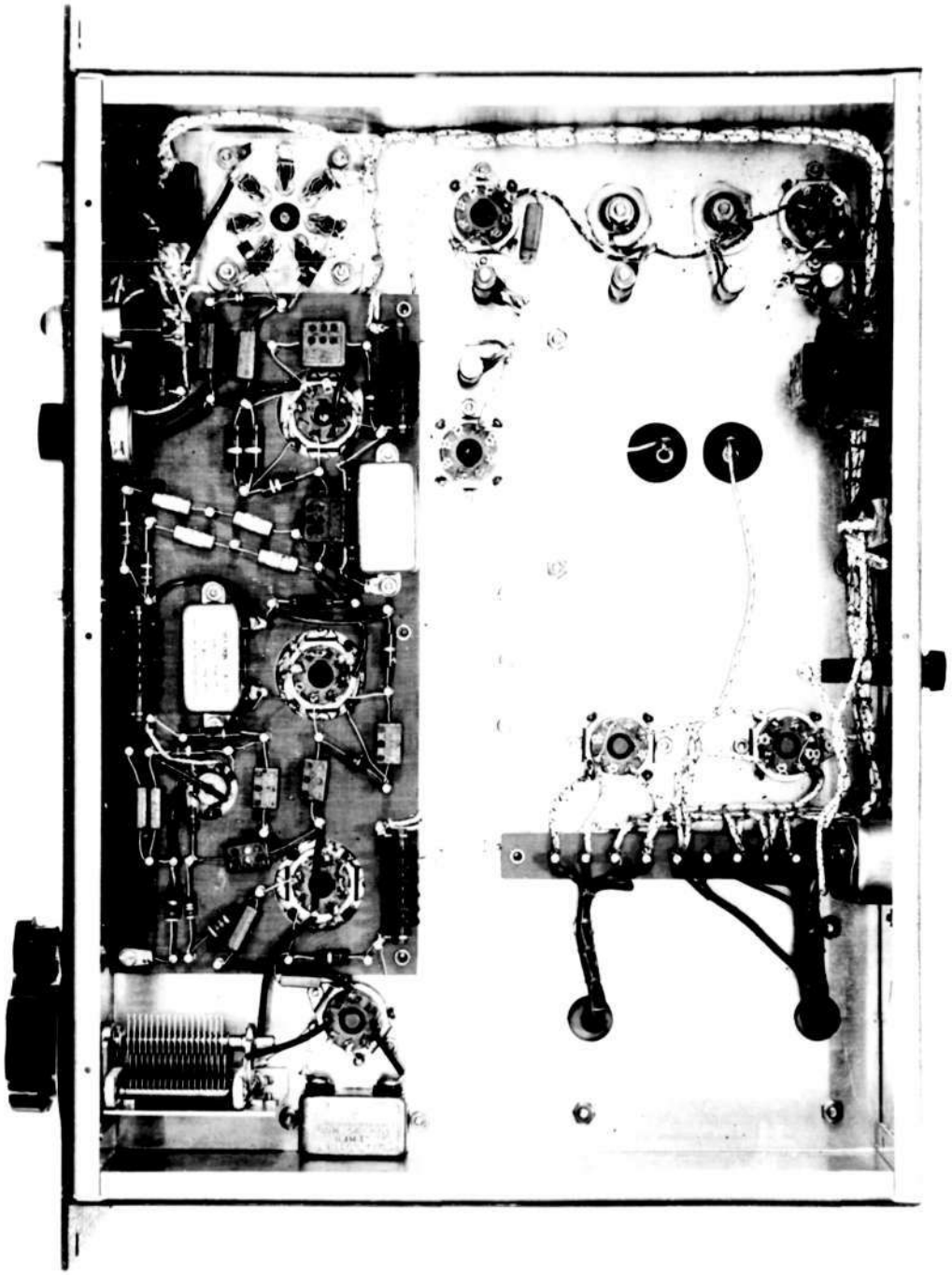
HK:bas:vh

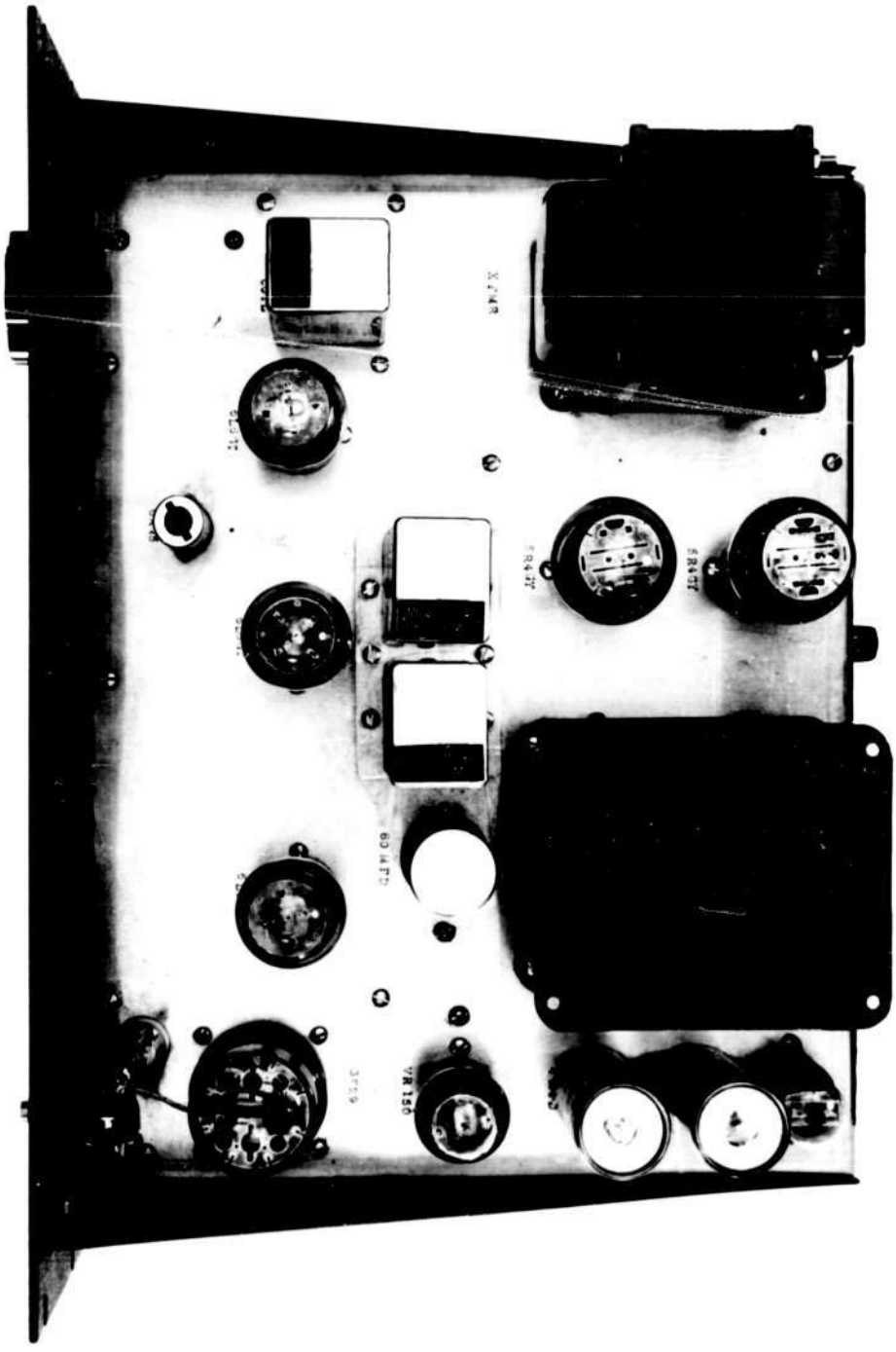


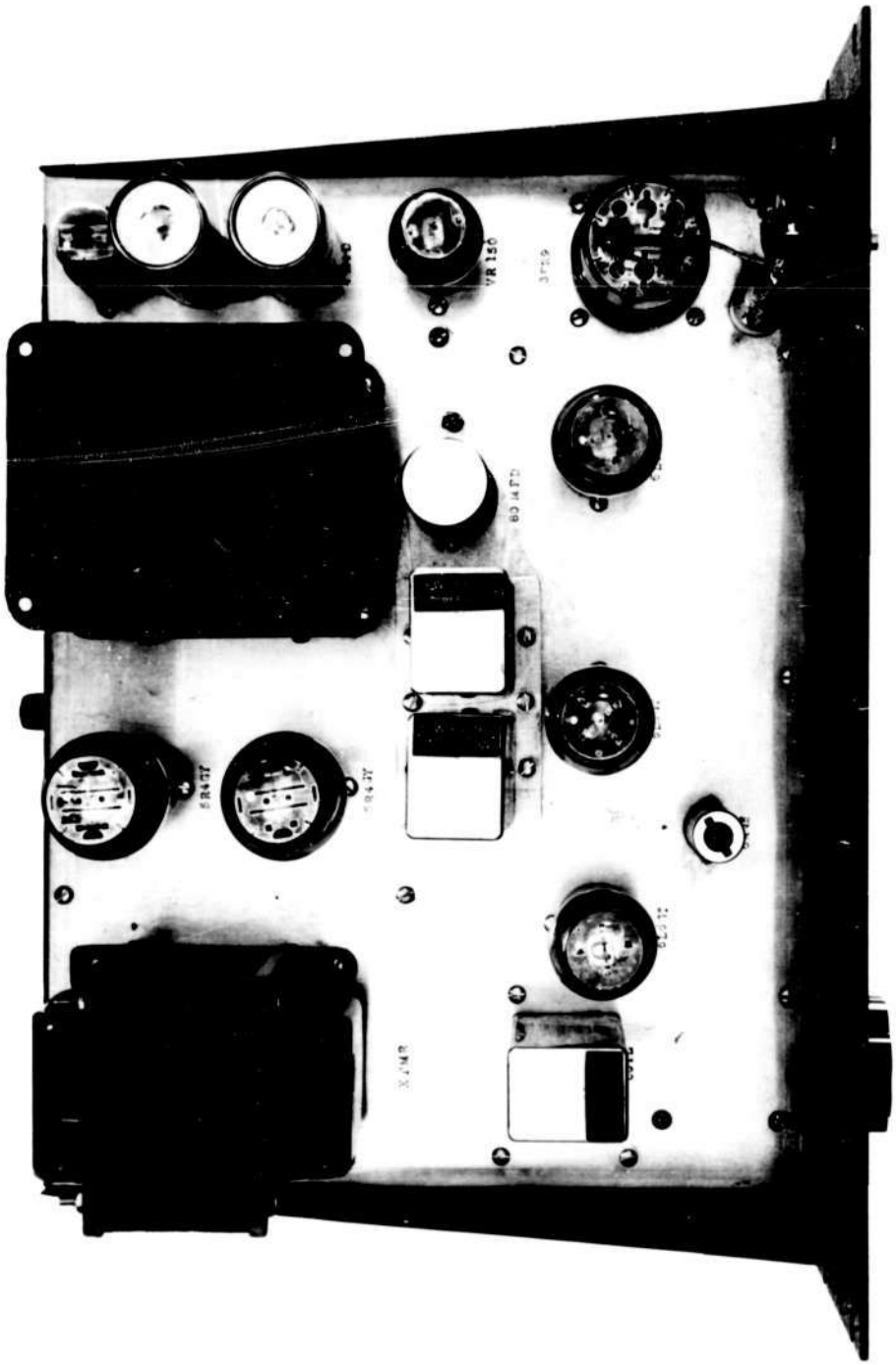
D IN 6345 ENG NOTE E-48

C-30007-2









Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: RESTORER PULSE GENERATOR

To: 6345 Engineers, R. March, E. Nickerson, Sylvania Engineers

From: Harry Kencsian

Date: October 24, 1947

Description

The restorer pulse generator provides paired, positive pulses 1 μs apart at a repetition frequency of 100 kc. The maximum pulse amplitude is 30 volts and the pulse width is approximately .1 μs at the base line.

A single positive or negative pulse can be obtained from a push-button controlled circuit. The push-button pulse is synchronized with the 100 kc. paired pulses. The "low frequency input" jack is connected to the grid of the gas tube (V14) which provides the push-button pulses so that the push-button pulses can be fired externally from a repetitive trigger source.

The input impedance can be made either 93 ohms or high impedance by means of a toggle switch on the front panel.

A source of 1 mc. triggers is required for operation. The paired-pulse and push-button pulse outputs were designed to work into a 93 ohm terminated line.

Circuit

The circuit is shown on Drawing D-30770-1. A 7F8 flip-flop (V2) divides the 1 mc. input to 500 kc. square waves. These square waves are amplified by a 6AG7 (V3) resonant-load amplifier, which feeds the 6L7 (V4 and V5) 5:1 modulation-type frequency divider. The 100 kc. output of the frequency divider is coupled to a 6AG7 (V6) buffer amplifier. The buffer drives a 6AG7 (V7) R-L-C peaker, which has a clipping circuit on the grid. The output of the R-L-C peaker is coupled to a 6AG7 (V8) line driver and to a 6760 (V10) cathode follower which feeds a 1 μs delay line. The output of the delay line is coupled to the grid of a 6AG7 (V9), which has its plate tied to the 6AG7 (V8) which drives the line. As a result the output transformer (T1) feeds the line with two pulses which are spaced 1 μs apart. The second pulse is slightly wider than the first pulse due to the widening effect of the delay line.

To obtain the push-button pulses, the 100 kc. sine wave output of the 6AG7 (V6) is fed into a 7F8 (V11), both halves of which are cascaded overdriven amplifiers. The 1 μs output pulse of the second half is connected to the control

grid of a 2D21 (V13) gas tube which is biased off. When the push-button is depressed, the bias on the shield grid is removed, which allows the 100 kc. pulse to fire the gas tube. The energy source for the gas tube is a .01 µf condenser (C45) which is charged through a high resistance. The leading edge of the output of the first gas tube is applied to the grid of the second gas tube (V14) through a variable delay network. The output pulse width is controlled by the series R-L-C circuit of the second gas tube. The output from the cathode of the second gas tube is coupled to the grid of a 6AG7 (V15) line driver.

The 1 µs output pulse of the 7F8 overdriven amplifier (V11) is connected to a jack (J5) through a cathode follower (V12). This 100 kc. output can be used for triggering a circuit in synchronism with the paired output pulses. Its amplitude is approximately 50 volts and the pulse width is about 1 µs.

Amplitude controls for each of the paired pulses and push-button pulses are provided on the front panel. The delay adjustment for the push-button pulses is on top of the chassis. The delay adjustment is used to control the position of the push-button pulse relative to the paired pulses. The position of the push-button pulse can be varied over a 10 µs period.

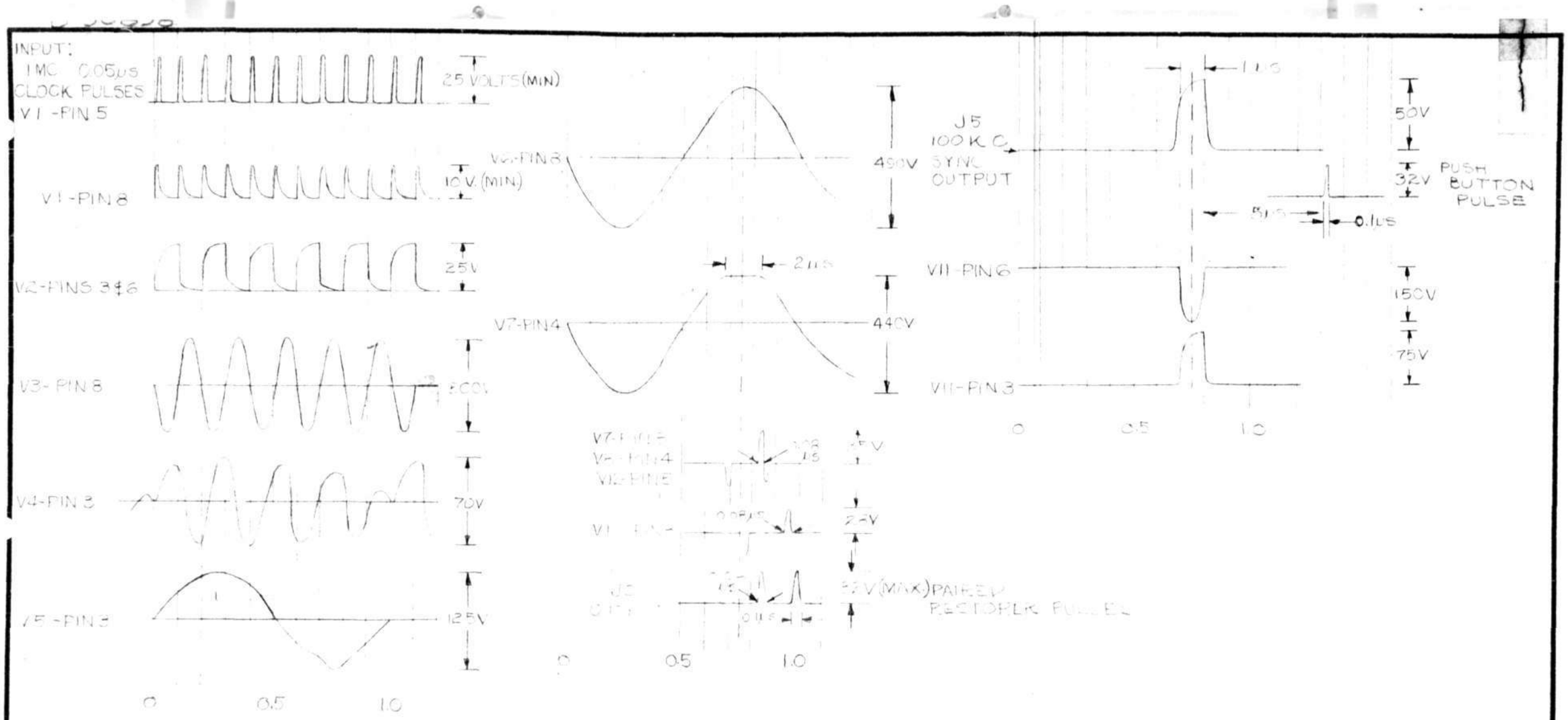
Future Considerations:

In case the need should arise, the interval between the paired pulses can be changed to 0.5 µs by replacing the 1 µs delay line with a 0.5 µs delay line. The repetition period can be changed to 12 µs by tuning the frequency divider so that it divides by six, instead of by five. To make this change, it would be necessary only to replace two of the fixed tuned condensers in the resonant circuits.

Signed Harry Kyrosian
Harry Kyrosian

HK/sp

Drawings: B-30893
B-30770-1

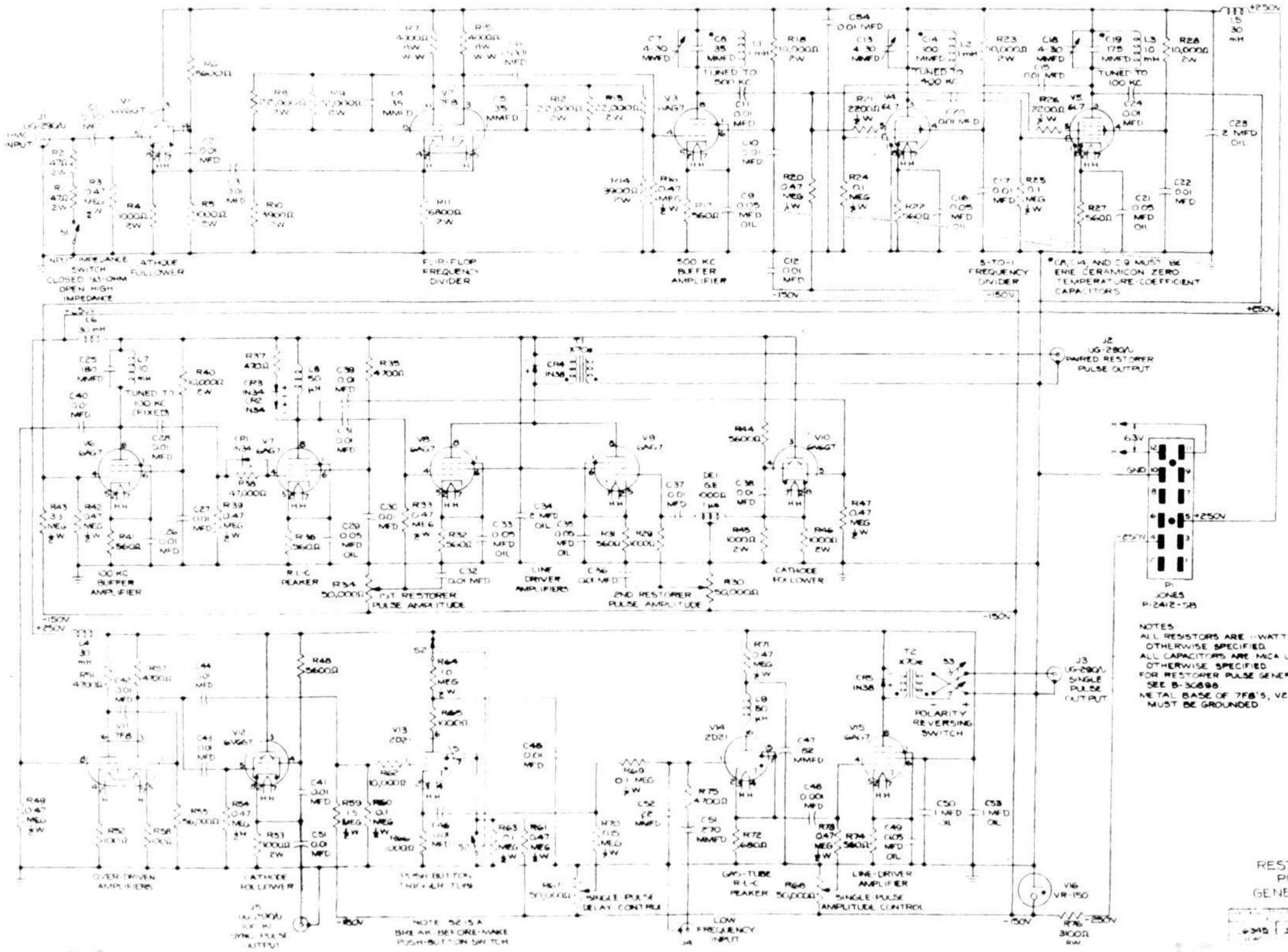


SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

TIMING DIAGRAM OF
RESTORER PULSE GENERATOR

SCALE:	DR. McHUGH 9-26-47	B- 30898
ENG. HC	CK.	APP.

D-30770-1



NOTES
ALL RESISTORS ARE ½-WATT ±10% UNLESS OTHERWISE SPECIFIED.
ALL CAPACITORS ARE MICA UNLESS OTHERWISE SPECIFIED.
FOR RESTORER PULSE GENERATOR WAVEFORMS SEE B-30898.
METAL BASE OF 7F8'S, V2 AND V11, MUST BE GROUNDED.

RESTORER PULSE GENERATOR

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: CHANGES IN DRAWINGS OF RESTORER PULSE GENERATOR

To: J. W. Forrester, H. Fahnestock, Sylvania Engineers, R. Murch
N. Taylor, C. Watt, D. R. Brown

From: Harry Kenosian

Date: October 9, 1947

The following drawings used for the Restorer Pulse Generator have been corrected as noted below:

D-30770-1 Restorer Pulse Generator

Grid resistor for V15 is labeled R73, 0.47 megohm, ½ watt.
Cathode resistor of V15 is R74, 560 ohms, 1 watt.
C8 is 35 mmfd. instead of 33 mmfd.
Add note: The metal bases of 7F8's, V2 and V11, must be grounded.

A-30776-1 and A-30777-1 Terminal Board Details

Missing 3/16 dimension between right-hand edge of board and adjacent pair of holes added.

A-30785-3 Terminal Board Assembly

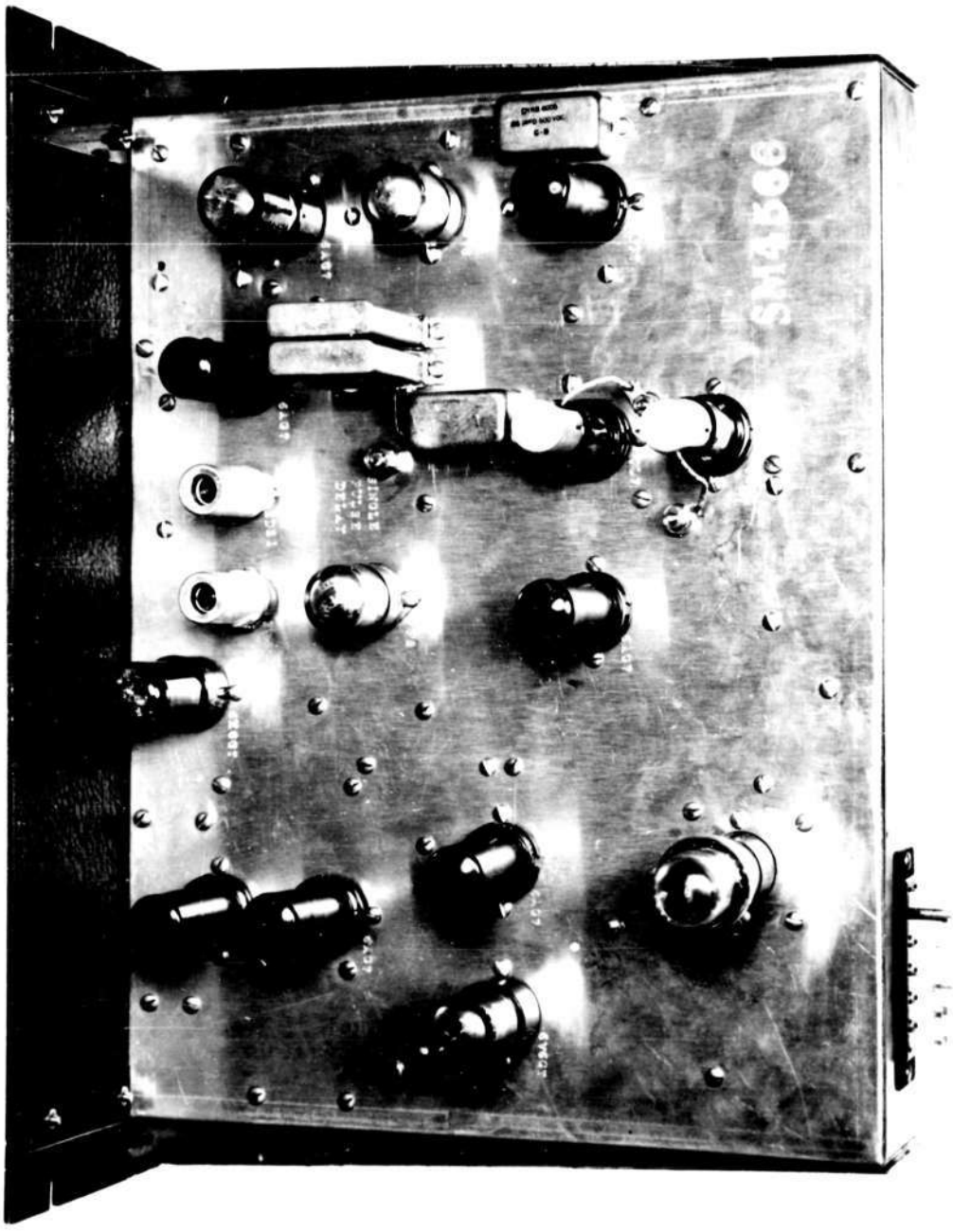
Item 4 in parts list, 4-40 x 9/16 lg. screw, changed to 4-40 x 5/8 lg. screw.

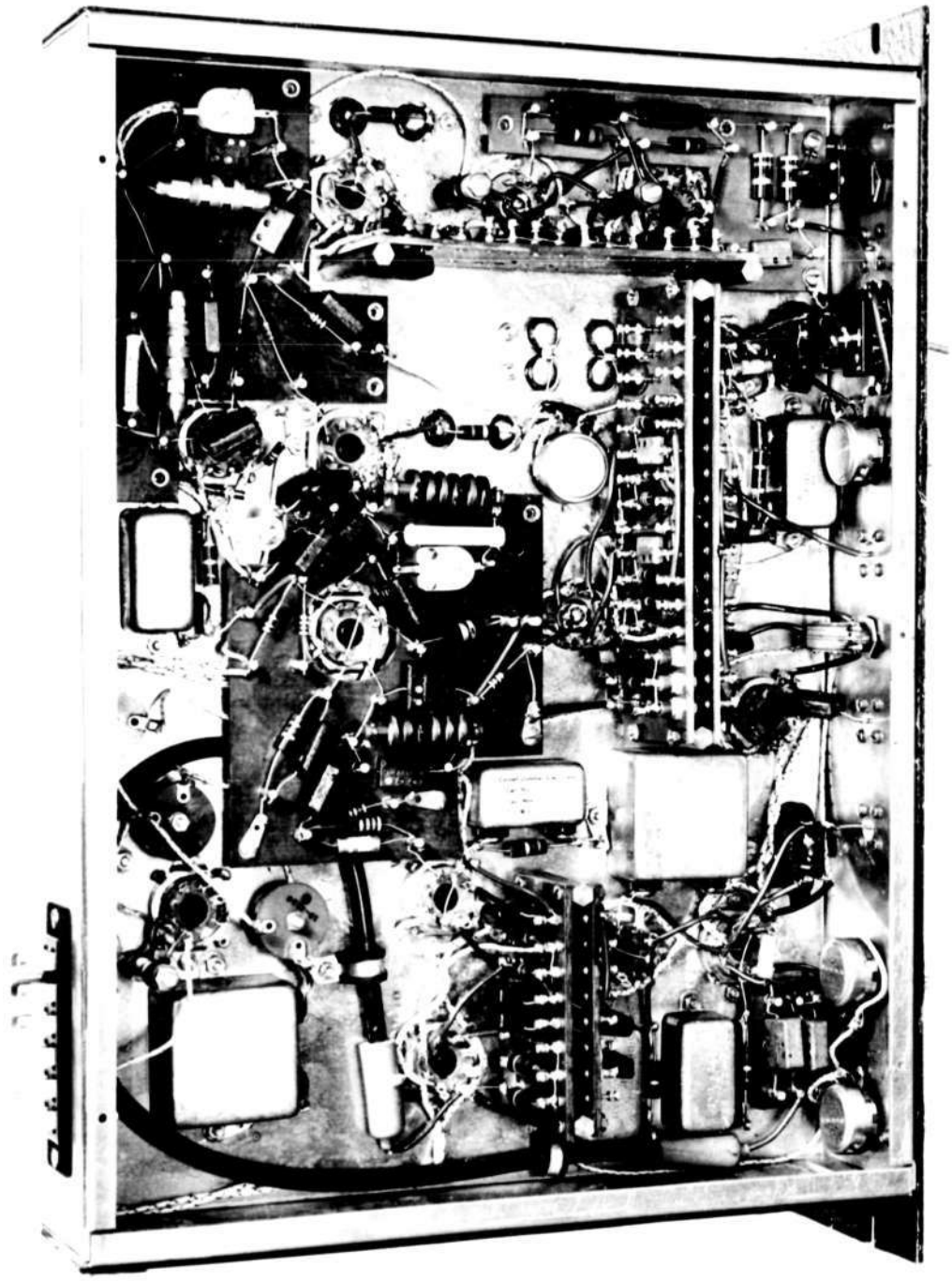
B-30787-5 Terminal Board Assembly

In mechanical parts list, part no. of item 3 is X-1216-D instead of X-1426-D. In electrical parts list C25 is 180 mmfd. instead of 180 mfd.; L5, 30 mH is changed to L3, 10 mH. On front view of assembly L-5 is changed to L-3.

Signed Harry Kenosian
Harry Kenosian

FP 255





ENGINEERING NOTES NO. E 58

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: 6345 Engineers — 6345

FROM: J. J. O'Brien — Page 1 of 1

SUBJECT: Sweep Calibrator — Drawing: D-50771

DATE: August 19, 1947

REFERENCE: Model 5 Synchroscope Instruction Manual p.p. 14 - 16

Instrument

There is available to the laboratory a sweep calibrator primarily intended for use on the Model 5 Synchroscope. The circuit is that of Radiation Laboratory Drawing Number A-6529-A, with a few minor modifications.

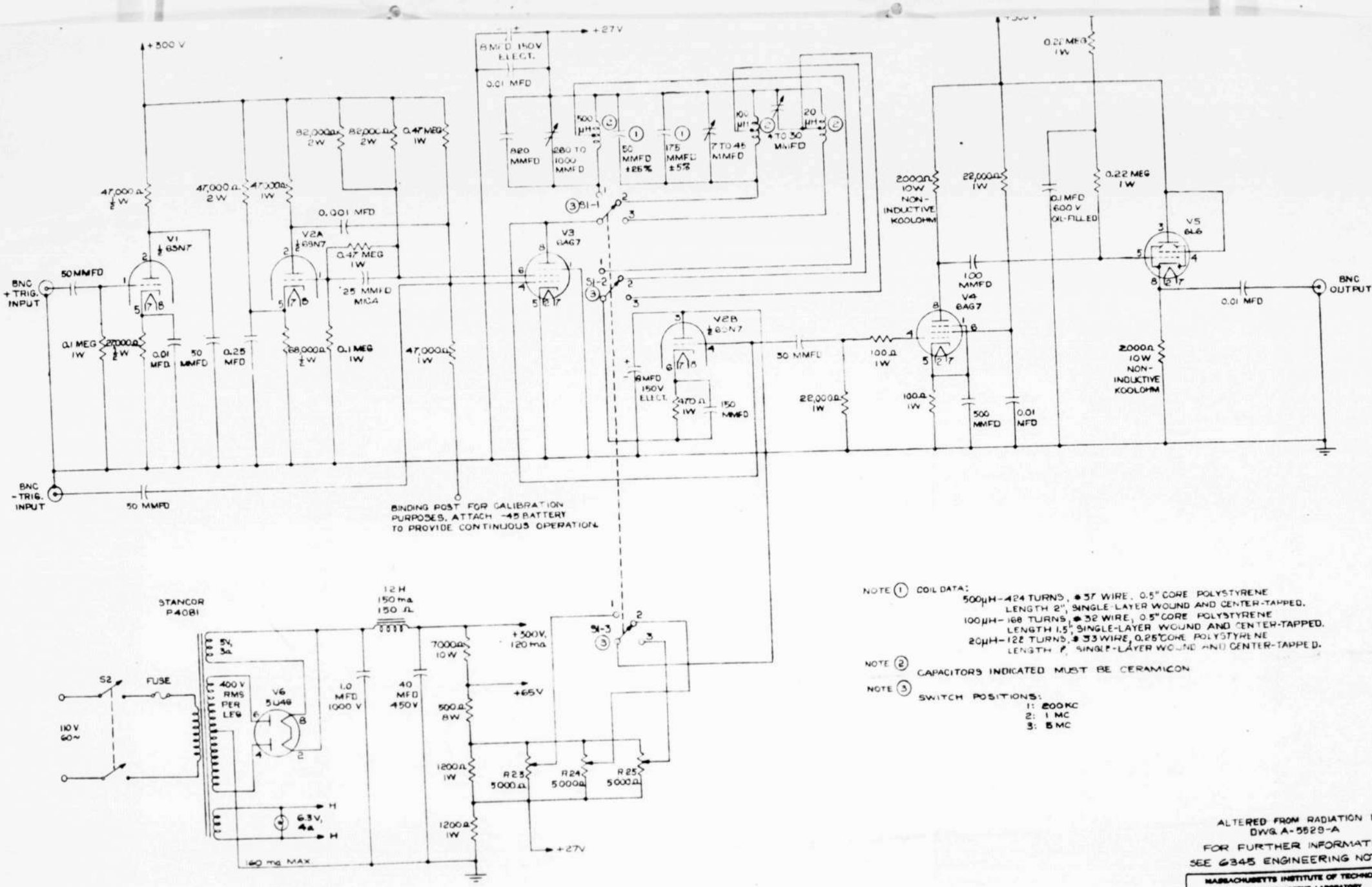
The calibrator when triggered has a sinusoidal output of either 0.2, 1 or 5 megacycles.

Adjustment

The three tuned circuits of the calibrator will require occasional alignment. Probably the easiest method is to use a 1 megacycle crystal controlled clock and a Lissajous pattern. A battery of -45 volts will be connected to a binding post, thus marked on the top of the chassis, so the calibrator will give c.w. output and not require an input trigger.

J. J. O'Brien

JJO/rp



NOTE (1) COIL DATA:
500μH – 124 TURNS, #37 WIRE, 0.5" CORE POLYSTYRENE
LENGTH 2", SINGLE-LAYER WOUND AND CENTER-TAPPED.
100μH – 168 TURNS, #32 WIRE, 0.5" CORE POLYSTYRENE
LENGTH 1.5", SINGLE-LAYER WOUND AND CENTER-TAPPED.
20μH – 122 TURNS, #33 WIRE, 0.25" CORE POLYSTYRENE
LENGTH ¾", SINGLE-LAYER WOUND AND CENTER-TAPPED.

NOTE (2) CAPACITORS INDICATED MUST BE CERAMICON

NOTE (3) SWITCH POSITIONS:
1: 200 KC
2: 1 MC
3: 5 MC

ALTERED FROM RADIATION LAB DWG. A-5529-A

FOR FURTHER INFORMATION SEE 6345 ENGINEERING NOTES E-58

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY
D.I.C. NO. 6345

SWEEP CALIBRATOR, MODEL A — D-30771

6345
Report No. 1-89

SERVOMECHANISMS LABORATORY
Massachusetts Institute of Technology
Cambridge, Massachusetts

Date of Report: March 4, 1946 Page 1 of 3 Pages

Written by: Louis D. Wilson Drawings:
D-30050
B-38110-C
B-38111-C

Subject: Timing Signal Generator for Digital Computer

Identification: This report covers the development of a timing pulse generator to be used in a 125,000 pulse per second experimental digital computer.

Conclusions: The timing pulse oscillator produced is a satisfactory piece of test equipment which does the job for which it was intended. However, in the light of work we have carried out since the completion of the design, the required output could be produced by simpler and more reliable circuits. The timer would provide more accurate timing if the selected pulses were squared before gating rather than after.

If this were done, and if a 6SJ7 were used for the gate tube with the gating signal on the screen grid and the squared 250 KC sine wave on the control grid, the amplitude of the output pulses could be much greater. Also, a DC coupled multivibrator (flip-flop) triggered by the squared 250 KC sine wave would provide a more reliable gate which could be used over a greater frequency range than the synchronized free-running multivibrator used. However, even with these improvements, it does not, at this time, seem likely that this type of timing pulse generator could be used at the much higher pulse repetition frequencies contemplated for the final computer.

Discussion: The operation of the timing pulse generator produced will be easily understood by correlating the indicated voltages and waveforms shown on the drawing C-39002-2 with the brief discussion which follows. The waveforms shown were observed with a TS 34/AP Oscilloscope, using the standard probe and high impedance input. The DC voltages were measured with an RCA voltohmyst.

A 250 KC sine wave signal of 0.1 volt RMS amplitude is amplified by the tuned amplifier V_1 to about 50 volts. The output of this stage is fed through the cathode follower V_2, which serves to prevent excessive loading of V_1, to grid pin 4 of V_3 and to grid pin 5 of V_4. V_3 is a multivibrator whose free-running repetition frequency is about 125 KC. This multivibrator synchronizes with the 250 KC signal fed to grid pin 4 and runs at half the frequency of the input sinusoid. The

square wave voltage appearing at plate pin 5 of V_3 is fed to the third grid(pin 8) of V_4 while the 250 KC sine wave is applied to the first grid(pin 5). Both of these grids are biased a sufficient amount below cutoff so that the tube(V_4) acts as a "gate" or "coincidence" tube and conducts appreciably only when both grids are in the positive positions of their AC cycles. The phasing of the two signals on the grids is such that alternate positive half cycles of the 250 KC sine wave cause V_4 to conduct. The resulting rounded negative pulses appearing on the plate of V_4 are inverted and amplified by V_5. The excursions of the plate of V_5 are limited by the diodes of V_6, producing the square pulses desired. At the final output of the 6L6 cathode follower (V_7) appear positive pulses of approximately 12 volts amplitude and 2 microseconds duration occurring every 8 microseconds(125 KC repetition rate). The rise and fall times of these pulses(to 95% of maximum value) are approximately equal to each other and are each about 0.35 microseconds.

In the course of the development work some difficulty was experienced with the operation of the gate tube(V_4). Three approaches to the gating problem were investigated. First, a pentode with gate signal applied to suppressor and signal to be gated applied to control grid was tried. The suppressor voltage plate current characteristics of the 6AG7 and 6SJ7 were investigated. Curves of the results for a typical tube of each type are plotted on Drawing B-38110-0. The complete data for 6 tubes of each type may be found in LTR618-23. This work showed the suppressor characteristics of the 6AG7 to be very unreliable since there was a variation from tube to tube of more than 80%. Also, the suppressor required - 80V to -100V bias to cutoff plate current, it would therefore not be too satisfactory for gating purposes.

The 6SJ7 proved to be better suited to the purpose. The suppressor characteristics did not seem to vary by more than about 15% (6 tubes tested) and for +300 volts on the plate and +115 on the screen grid plate current cutoff occurred at about -80 volts on the suppressor. The data indicated that satisfactory gating operation could be obtained with a negative bias of about 85 volts and a positive gating signal of 30 volts to 70 volts amplitude applied to the suppressor. The control grid would also be biased below cutoff and the signal to be gated would be a positive pulse of sufficient amplitude to swing the control grid almost to the grid current point(to about -1 volt).

This method was tried and is usable. However, some difficulty was experienced with capacitive coupling from suppressor to plate. This caused some of the gate signal to appear at the plate even if the tube was kept below cutoff by the control grid.

This circuit requires further investigation using the Western Electric 6AS6, a pentode with carefully controlled suppressor characteristic and smaller suppressor-plate capacity. This tube is designed for this type of application.

Secondly, a pentagrid tube type 6SA7 was used with gate signal applied to grid number 3 and the signal to be gated applied to grid number 1. To determine operating conditions to be used, tests were run on the control characteristics of the two control grids, grid 1 (pin 5) and grid 3(pin 8). The plotted results of these measurements may be found on Drawing B-38111-G. From these tests, it was determined that satisfactory gating operation should be obtained by biasing both grids with a negative potential of 15 volts or more and swinging them from this point up to -2 or -3 volts during the time the tube was to conduct. The circuit used in the timing oscillator was of this type and is quite satisfactory in this application. It has, however, at least one limitation. Since the 6SA7 is a low-current tube, the pulse amplitude and possible rise time are somewhat limited.

Finally, tests were run using 6AK5 and 6SJ7 pentodes with the gating signal applied to the screen grid and the singal to be gated applied to the control grid. Measurements of the control characteristics of the screen and control grids of these tubes were made. The results of this work may be found on Drawing B-38111-G.

Either of these tubes may be used as a gate tube in this way with good results. They have the advantage that only a fraction of a volt negative bias on the gating grid(screen grid) is sufficient to hold the tube below cutoff even with the control grid positive by several volts. This bias is easily obtained by means of the average negative voltage built up across the coupling capacitor to this grid since the grid draws current during the gate. (This biasing arrangement is, of course, only satisfactory for constant pulse repetition rate.) On the control grid, a negative bias of 10 volts with plate at +150V and screen at +100 volts will maintain cutoff conditions.

In application where grid clipping of the top of the gated signal is desirable or, at least not objectionable, and where the loading on the signal source due to grid conduction is not objectionable, the coupling circuit may also be used to provide the necessary negative bias here. (Again, this is only true for constant prf.)

Using this method of providing the bias voltage and with +300 volts plate supply, a gate signal of about 50 volts amplitude and a 10 volt pulse to be gated, output pulses of 100 volts are easily obtained with almost infinite loss onthe unwanted signals. The only important limitation of this circuit is the fact that the gating signal source must be capable of supplying a considerable amount of power to the screen grid.

Engineer in charge: Louis D. Wilson

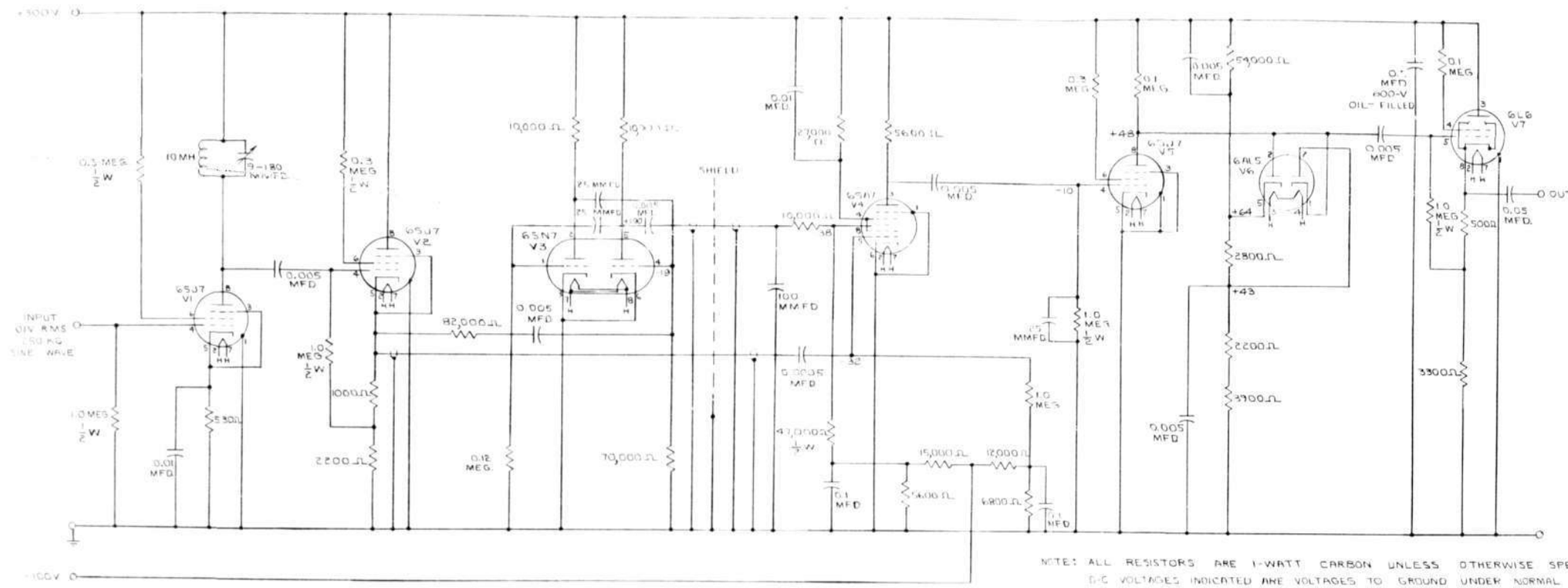
Technicians: Frank H. Cornell

Approved By: Jay W. Forrester

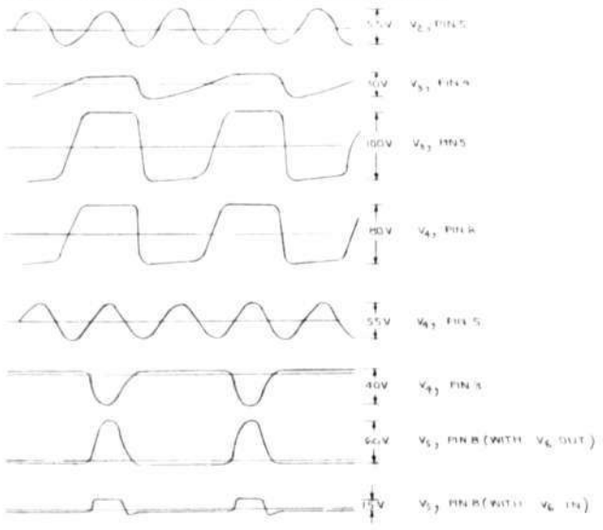
LDW:bas

D-3005O-1
WO.

TOLERANCES NOT OTHERWISE SPECIFIED:
DECIMAL ± .005 FRACTIONAL ± 1/64



VOLTAGE WAVE-FORMS AT VARIOUS POINTS IN CIRCUIT



NOTE: ALL RESISTORS ARE 1-WATT CARBON UNLESS OTHERWISE SPECIFIED. D-C VOLTAGES INDICATED ARE VOLTAGES TO GROUND UNDER NORMAL OPERATING CONDITIONS.

125 KC PULSE GENERATOR CIRCUIT SCHEMATIC

RESTRICTED

ITEM	MATERIAL - DESCRIPTION	PART NO.	QUAN.

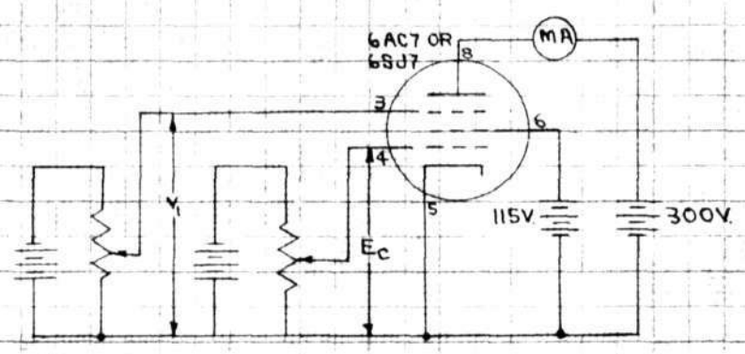
SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6545

CIRCUIT SCHEMATIC PSIA-LFC

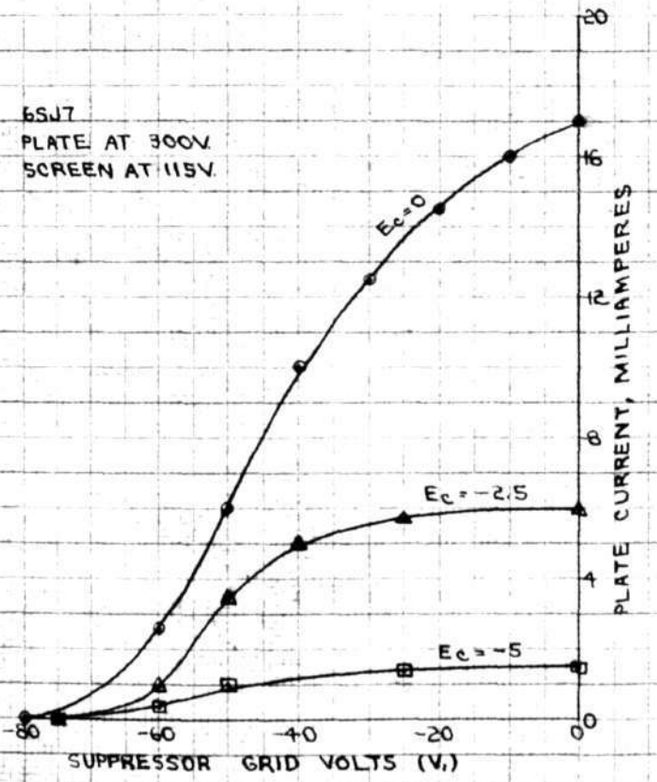
SCALE: | DR. D.L.D. 3-19-46 | CK. TL. 3/21/46 | APP. | TR. J.J.W.

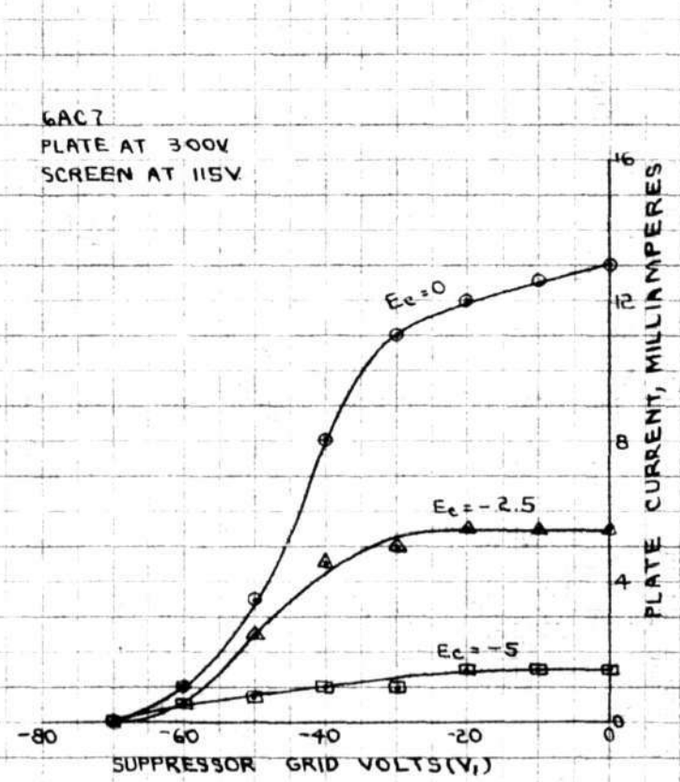
D-30050-1

SUPPRESSOR GRID TRANSFER CHARACTERISTICS OF 6AS7 AND 6SJ7 VACUUM TUBES.



DATA FROM IFHC 18-23
TESTS MADE BY FHC
TESTS MADE 1/3/46
ENGINEER IN CHARGE: LDW
CURVE DRAWN 3/16/46

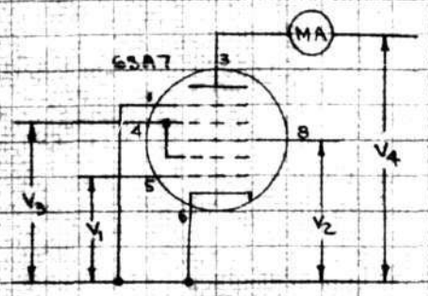




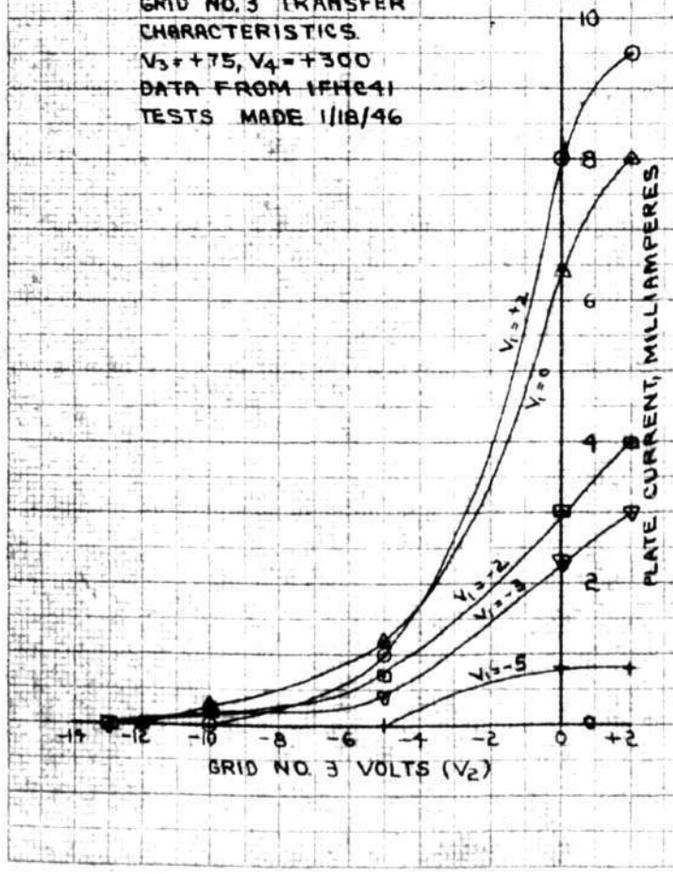
D.L.O.

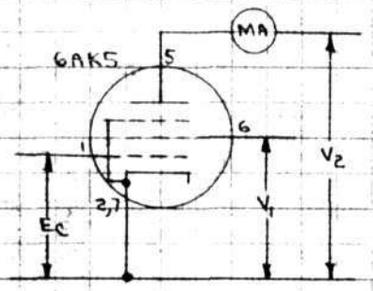
6345 B 38110-G

TRANSFER CHARACTERISTICS OF GRID NO. 3 OF 6SA7 AND SCREEN GRIDS OF 6SJ7 AND 6AK5.
TESTS MADE BY FHC
ENGINEER IN CHARGE: LOW
CURVE DRAWN 3/15/46

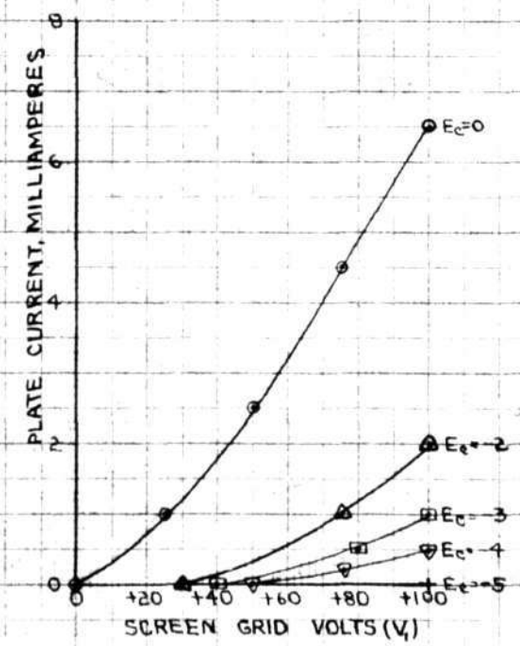


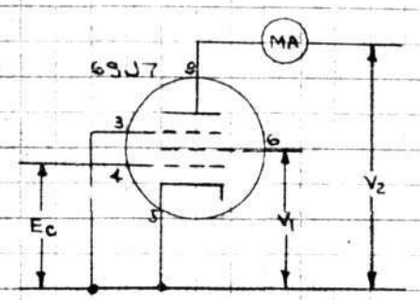
6SA7
GRID NO. 3 TRANSFER CHARACTERISTICS.
$V_3 = +75$, $V_4 = +300$
DATA FROM IFHC41
TESTS MADE 1/18/46



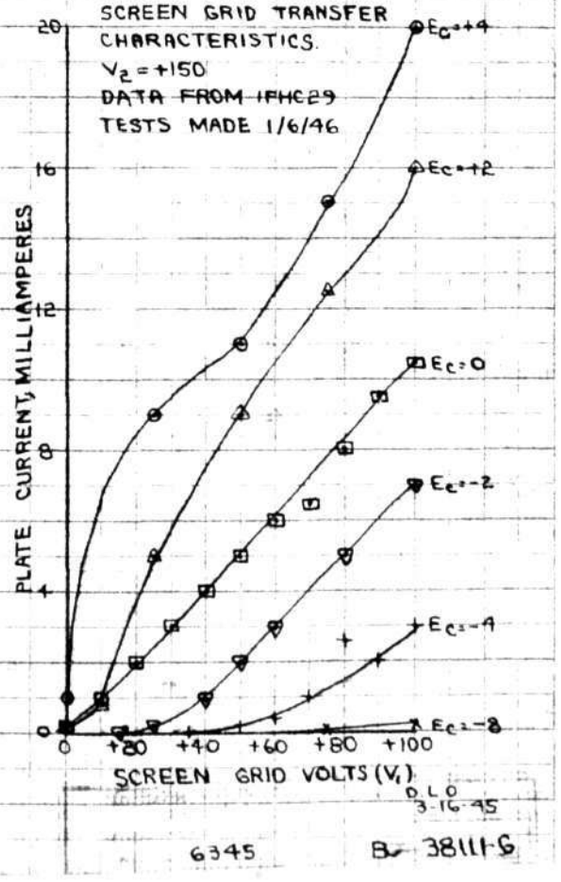


6AK5
SCREEN GRID TRANSFER CHARACTERISTICS.
$V_2 = +150$
DATA FROM IFHC29
TESTS MADE 1/6/46





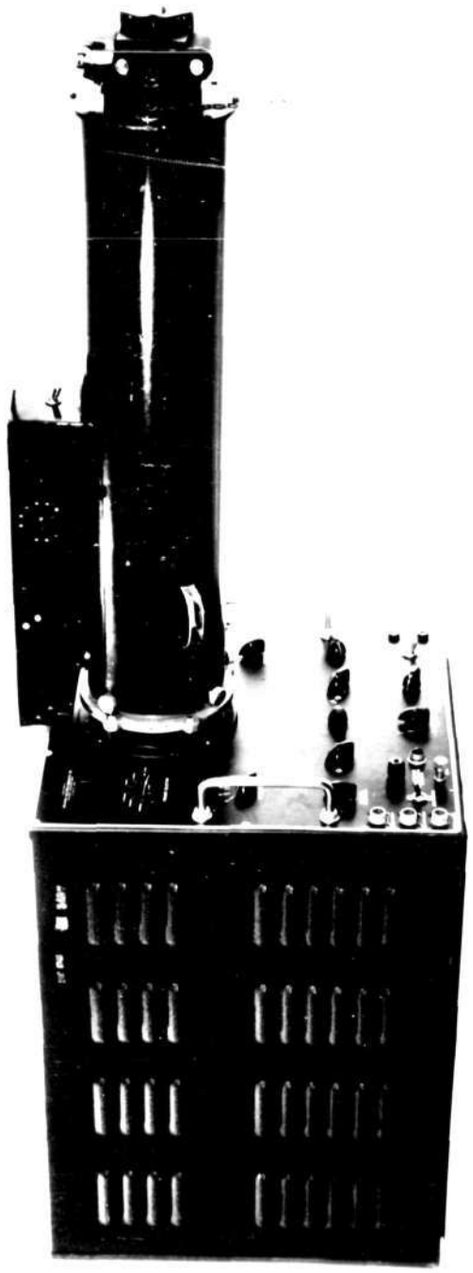
6SJ7
SCREEN GRID TRANSFER CHARACTERISTICS.
$V_2 = +150$
DATA FROM IFHC29
TESTS MADE 1/6/46



D.L.O.
3-16-45

6345 B- 38111-G

FB 212



FB-295

6345
Report No. R-109

SERVOMECHANISMS LABORATORY
Massachusetts Institute of Technology
Cambridge, Massachusetts

Date of Report: December 17, 1946 — Page 1 of 14 pages

Subject: Gate Circuits — Drawings Listed in Table of Contents

Written by: David R. Brown

References:

A. 6345 Engineering Notes No. E-25, A Program for the Computer, Switching, and Engineering Divisions.

B. Radiation Laboratory Technical Series, Book 3, Chapter 10, Section 18.3.

C. 6345 Report No. R-105, Characteristic Curves of the 1N34 Germanium-Crystal Diode.

D. 6345 Report No. R-104 Static Characteristic Curves for Western Electric 6AS6 Vacuum Tube.

E. NDRC Division 14, Report No. 158, Analysis of the 6SA7 Gated Amplifier.

F. 6345 Report No. R-89, Timing Signal Generator for Digital Computer.

TABLE OF CONTENTS

This is a report on an investigation of gate circuits which has been conducted to develop some gate circuits suitable for use in computer equipment and test equipment as outlined in Reference A.

General Discussion of Gate Circuits

A gate circuit is a time coincidence device which, ideally, produces an output pulse only during the time that two or more pulses are applied to the gate circuit. Only gate circuits which produce an output pulse when two input pulses are present will be discussed here. The two signals applied to the gate circuit will be called the input signal and the gate signal. The input signal usually consists of a train of pulses. These pulses will appear at the output only during the time that a gate pulse is applied. By properly timing the gate pulse any given pulse or pulses in the train may be selected.

Two classes of gate circuits will be discussed, those which employ diodes and those which employ tubes with one or more grids. An excellent discussion of gate circuits in general and of diode gate circuits may be found in Reference B.

A number of the important properties of a gate circuit may be determined if the amplitude of the output pulse as a function of the input-pulse amplitude and the gate-pulse amplitude is known. This might be shown as a family of curves as in Drawing No. A-30190. Note that the output pulse as a function of the input pulse may be determined for any given gate-pulse amplitude including zero gate. Also, the output pulse as a function of gate-pulse amplitude may be determined for any given input-pulse amplitude including zero input pulse. The output pulse for zero input pulse is the gate pulse which appears at the output. These curves should also indicate the polarity of the input, gate, and output pulses. The input-pulse impedance, the gate-pulse impedance, and the output impedance of the gate circuit are important properties. The rise time, fall time, and droop introduced by the gate circuit on a nearly rectangular input pulse are also important. Other factors are the number of tubes required, the power required, the voltages required, and the effect of variation in supply voltage and characteristics of circuit components.

Description of Some Practical Gate Circuits

In general, the performance of a gate circuit can be predicted by an analysis based upon the characteristics of its components. This practice has been adopted. After the characteristics were obtained and a simple analysis made, the gate circuit was constructed and its performance checked. The arrangement used for testing the gate circuit is shown in Drawing No. A-30191. A Model 5 synchroscope, No. 53, was internally synchronized at 500 cycles. The output trigger was used to trigger two gas-tube pulse generators. The output of one pulse

generator was delayed about one-third microsecond with respect to the other. The delayed pulse was used as the input pulse; it had a length of 0.25 μs and a rise time and a fall time of approximately 0.01 and 0.03 microsecond respectively. The amplitude of the input pulse could be adjusted by means of an attenuator as shown in the figure. The gate pulse had a length of 1 μs and a rise time and a fall time of approximately 0.05 microsecond. The amplitude of the gate pulse could be adjusted by means of an attenuator built into the pulse generator. The output pulse from the gate under test was applied directly to the deflection plates of the cathode-ray tube. The impedance of the pulse generators, as seen from the gate circuit under test, was less than 100 ohms. The capacitive load on the output of the gate circuit under test was approximately 5 micro-microfarads.

A. Diode Gate Circuit - The circuit diagram of the diode gate circuit is shown in Drawing No. A-30192. If an input pulse is applied in the absence of a gate pulse, the diode conducts and the amplitude of the output pulse is:

$$(1) \qquad e_o = \left(\frac{r_f + R'}{R_2 + r_f + R'} \right) e_i$$

$$\text{where} \quad R' = \frac{R_3 R_g}{R_3 + R_g}$$

If a gate pulse larger than the input pulse is applied, the diode does not conduct and the amplitude of the output pulse, neglecting R', is

$$(2) \qquad e_o = \left(\frac{r_b}{R_2 + r_b} \right) e_i$$

The charge and discharge time constant for the shunt capacitance across the output terminals is $R_2 C_s$. Note that C_s includes the diode capacitance. The rise and fall time will be about 2.2 times this time constant.

The resistance the input-pulse generator works into is R_1. The gate-pulse generator works into a resistance R_3. The output resistance is approximately R_2.

Two factors determine the choice of R_2. One, the resistor R_2 must be large compared to $r_f + R'$ as seen from Equation (1). Two, the output impedance must be made low to keep the rise and fall times of the output pulse short. Now, for a 1N34 crystal diode, r_f is about 100 ohms and r_b is about 100,000 ohms, as shown in Reference C. Suppose R' is

300 ohms. From Equation (1), R_2 should be 6000 ohms for an output pulse 5 percent of the input pulse in absence of a gate pulse. Any decrease in R_2 will increase the amplitude of the output pulse in absence of a gate pulse. Notice that a germanium-crystal diode is superior to a vacuum-tube diode for this application, since r_f is the important property rather than r_b. Considering the case where a gate pulse has been applied, Equation (2), R_2 can be quite large before the output-pulse amplitude is appreciably attenuated. An R_2 of 6000 ohms would permit an output-pulse amplitude 95 percent of the input-pulse amplitude.

The circuit tested in the laboratory had the component values listed in Drawing No. A-30192. The characteristic curves of this gate circuit, determined from Equations (1) and (2), are shown in Drawing No. A-30193. The two points indicated were checked experimentally. The rise time and fall time introduced on a nearly rectangular pulse measured 0.03 microsecond.

The outstanding advantages of the diode gate circuit are that no power supply is necessary and no vacuum tubes are required. The disadvantages are the very-low-impedance gate-pulse generator required and the high output impedance required for large attenuation of unwanted input pulses.

B. Two-Diode Gate Circuit - A circuit diagram of the two-diode gate circuit is shown in Drawing No. A-30194. Diode 2 is normally conducting because of the bias voltage $E_{kk'}$. The voltage E_{kk} is selected so that Point A will be negative at all times in the absence of a gate pulse. Then, if an input pulse is applied to the circuit, diode 1 will remain conducting and diode 1 will remain non-conducting. As a result, the signal will be greatly attenuated. If a gate pulse is applied, diode 2 will stop conducting; and, when an input pulse is applied, diode 1 will conduct. This permits the signal to appear across the output terminals only somewhat attenuated. Note that the gate-pulse amplitude must be nearly the sum of the amplitude of the input pulse and the bias voltage $E_{kk'}$.

If no gate pulse is applied, an approximation of the output-pulse amplitude is given by

$$(3) \qquad e_o = \left(\frac{R' - r_f}{R_1 + R' + r_f} \right) \left(\frac{R_4}{R_4 + r_6} \right) e_1$$

$$\text{where } R' = \frac{R_3 R_5}{R_3 + R_5}$$

The amplitude of the output pulse, e_o, if a gate pulse of sufficient amplitude is applied and the current through the non-conducting

diode is neglected, is

$$(4) \qquad e_o = \left(\frac{R_4}{R_1 + R_4 + r_f} \right) e_i$$

If no gate pulse is applied, the portion of the input pulse which appears at Point A is

$$\left(\frac{R' + r_f}{R_1 + R' + r_f} \right) e_i$$

The quiescent voltage at Point A is given by

$$-\left(\frac{R_1 + R_2}{R_1 + R_2 + R_3 - r_f} \right) E_{kk}$$

and must be less than the portion of the input pulse which appears at point A; or,

$$(5) \qquad E_{kk} > \left(\frac{R_1 + R_2 + R_3 + r_f}{R_1 + R_2} \right) \left(\frac{R' + r_f}{R_1 + R' + r_f} \right) e_i$$

If E_{kk} is less than this amount, Equation (3) will not hold and an appreciable portion of the input pulse will appear at the output.

If a gate pulse of sufficient amplitude is applied, the portion of the input pulse which appears at Point A is

$$\left(\frac{R_4 + r_f}{R_1 + R_4 + r_f} \right) e_i$$

The gate pulse must be of sufficient amplitude to drive the cathode of diode 2 positive by at least that amount; or,

$$(6) \qquad e_g > E_{kk} + \left(\frac{R_4 + r_f}{R_1 + R_4 + r_f} \right) e_i$$

The charging time constant for the shunt capacitance across the output terminals will be approximately $(R_1 + r_f) C_s$. The discharge-time constant will be approximately $R_4 C_s$.

The input-pulse generator works into a resistance load.

$R_2 + R_4 + r_f$. The gate-pulse generator works into a resistance load R_3. The output resistance is $R_1 + R_1 + r_f$ in parallel with R_4 during a pulse and R_4 alone between pulses.

Now consider the gate circuit of Drawing No. A-30194 with the component values listed. Assume that 30-volt input pulses are to be gated. The output pulse for no gate applied, is, from Equation (3)

$$R' = \frac{(330)(100)}{330 + 100}$$

$$= 77 \text{ ohms}$$

$$e_0 = \left(\frac{77 + 100}{330 + 77 + 100}\right)\left(\frac{2,200}{2,200 + 100,000}\right) 30$$

$$= 0.15 \text{ volt}$$

The output pulse, for a gate of sufficient amplitude applied, is, from Equation (4)

$$e_0 = \left(\frac{2,200}{330 + 2,200 + 100}\right) 30$$

$$= 16.7 \text{ volts}$$

Next, determine E_{kk} from Equation (5).

$$E_{kk} > \left(\frac{330 + 10,000 + 330 + 100}{330 + 10,000}\right)\left(\frac{77 + 100}{330 + 77 + 100}\right) 30$$

$$> 7.3 \text{ volts}$$

Make E_{kk} equal to 10 volts; then e_g is given by Equation (6).

$$e_g > 10 + \left(\frac{2,200 + 100}{330 + 2,200 + 100}\right) 30$$

$$> 27.4 \text{ volts}$$

The characteristics of this gate circuit are shown in Drawing No. A-30195. The two experimental points indicated were taken with zero gate and with a 26-volt gate pulse. The rise time and fall time introduced by the gate circuit were not measurable.

The outstanding advantages of the two-diode gate circuit are:

that no vacuum tubes are required and negligible rise time and fall time are introduced. The outstanding disadvantages are the very-low-impedance gate-pulse and input-pulse generators required and the attenuation of wanted input pulses introduced by the gate circuit.

C. 6AS6 Gate Circuit - Some static characteristics of a 6AS6 pentode are shown in Drawings No. A-30196 and No. A-30197. The circuit used to obtain the characteristics of Drawing No. A-30196 is shown in Drawing No. A-30198. The plate-supply and screen voltages were held constant at +100 volts. The suppressor voltage was held constant at +15 volts. A 1000-ohm resistor was placed in series with the plate. The plate current, i_b, the screen current, i_{c_2}, and the control-grid current, i_{c_1}, are plotted for negative and positive values of control-grid voltage, e_{c_1}. Cutoff may be defined as the magnitude of the voltage at which the extrapolated straight-line portion of the $i_b - e_{c_1}$ curve intersects the zero axis. This is 3 volts as shown at point A in Drawing A-30196.

The circuit used to obtain the characteristics of Drawing No. A-30197 is shown in Drawing No. A-30199. The plate-supply and screen voltages were held constant at +100 volts. The control-grid voltage was held constant at +2 volts. A 1000-ohm resistor was placed in series with the plate. The plate current, i_b, the suppressor current, i_{c_3}, the screen current, i_{c_2}, and the control-grid current, i_{c_1} are plotted for negative and positive values of suppressor voltage. The cutoff for the suppressor may be defined the same as for the control-grid. It is 5 volts as shown at point B in Drawing No. A-30197.

These characteristics were obtained using an average tube, tube No. 6 referred to in Reference D.

The gate circuit is shown in Drawing No. A-30200. The fixed-bias voltages were selected as approximately three times the cutoff voltages. The cutoff for the control-grid was found to be 3 volts. Make the fixed bias, then, -10 volts. The cutoff for the suppressor was found to be 5 volts. The fixed bias, then, should be -15 volts. Note that a 10,000-ohm resistor is placed in series with the control grid. The clipping properties of this scheme permit a much greater variation of the amplitude of the input pulse. This may be seen from the characteristics of Drawing No. A-30201. Suppose that the suppressor is at +15 volts and an input pulse of 15 volts is applied to the gate circuit. The control grid will draw current and the actual control-grid voltage will be determined by the intersection of the $i_{c_1} - e_{c_1}$ curve and

the straight line, $e_{c_1} = 5 - 10{,}000\, i_{c_1}$, point C. The actual grid voltage may be determined in this manner for a number of input-pulse amplitudes. When the control-grid voltage is known, the plate current may be determined from Drawing No. A-30196. The plate voltage, hence the output-pulse amplitude, is then known. The output pulse versus input pulse, for the suppressor at +15 volts, is shown in Drawing No. A-30201.

Again refer to the gate circuit shown in Drawing No. A-30200. Suppose that the input pulses are of such an amplitude that the actual grid voltage is driven to +2 volts. The effect of variation of the amplitude of the gate pulse may be determined fromthe characteristics of Drawing No. A-30197. The output pulse is plotted as a function of gate-pulse amplitude in Drawing No. A-30202.

From Drawings No. A-30201 and No. A-30202 the design input-pulse amplitude and gate-pulse amplitude may be selected. An input-pulse amplitude of 15 volts and a gate-pulse amplitude of 20 volts appear desirable. This corresponds to an actual control-grid voltage of approximately 2 volts. The grid resistance, Drawing No. A-30196, is 4,000 ohms. The resistance the input-pulse generator works into is 4,000 plus 10,000, or 14,000 ohms. The suppressor-grid resistance, Drawing No. A-30197, is approximately 6,000 ohms. The resistance the gate-pulse generator works into is therefore 6,000 ohms. The output resistance will be R_L in parallel with r_p during the pulse and R_L between pulses. From Drawing No. A-30196, r_p is 4,000 ohms when e_{c_1} is 2 volts. Therefore, the output resistance will be 800 ohms during the pulse and 1,000 ohms between pulses.

The rated dissipation of the 6AS6 is 1.7 watts on the plate and0.75 watts onthe screen. The actual dissipation must be calculated for two cases: one, the suppressor cutoff; two, the suppressor positive. The electrode voltages, currents, and dissipations are tabulated for these two cases in Table 1. The duty cycle may vary over a wide range; the maximum will probably be about 0.25. Then the allowable instantaneous dissiptation may be calculated on the basis of a duty cycle of 0.25 and a steady-state dissipation not exceeding 50 percent of the rated dissipation; thus, the instantaneous dissipation for either of the two cases should not exceed 3.4 watts on the plate and 1.5 watts on the screen. Notice that for the first case, the allowable screen dissipation is exceeded by 0.2 watt.

The performance of the gate circuit is illustrated by the waveforms of Drawing No. A-30203. Waveform A shows a 0.25-microsecond input pulse; waveform B shows a 1-microsecond gate pulse. The output-pulse waveforms, for several input-pulse amplitudes, are shown in C, D, E, and F. These data are also plotted as experimental points in Drawings No. A-30201 and A-30202.

TABLE I

	e_1 = 15V, e_g = 0			e_1 = 15V, e_g = 30V		
	e V	i ma	P w	e V	i ma	P w
CONTROL-GRID	0.9	0.5	0.000,5	2	0.4	0.0098
SCREEN	100	17	1.7	100	8	0.8
SUPPRESSOR	-15	0	0	15	2.5	0.04
PLATE	100	0	0	80	20	1.6

Electrode Dissipation - 6AS6 Gate Circuit - E_{cc_2} = 100V

The outstanding advantages of this gate circuit are the fairly high resistance into which the input-pulse generator and gate-pulse generator work and the output-amplitude-versus-input-amplitude characteristic. The outstanding disadvantages are the polarity inversion of thepulse, the supply voltages required, and the excessive screen dissipation. A pulse transformer might be used in the plate circuit to re-invert the pulse.

In an effort to reduce the screen dissipation, the screen voltage was reduced from 100 volts to 50 volts. The circuit diagram is shown in Drawing No. A-30204. Note that R_L has been increased to 2,200 ohms.

The control grid characteristics are shown in Drawing No. A-30205 and the suppressor characteristics are shown in Drawing No. A-30206. The circuits used for obtaining the data are shown in Drawings No. A-30207 and No. A-30208. Curves of output-pulse amplitude versus input-pulse amplitude and of output-pulse amplitude versus gate-pulse amplitude are shown in Drawings No. A-30209 and No. A-30210. Note that for this gate circuit the cutoff voltages are less and the required input-pulse and gate-pulse amplitudes are less. An input-pulse amplitude of 13 volts and a gate-pulse amplitude of 20 volts appear desirable.

The grid resistance is 3,500 ohms. Then, the resistance the input-pulse generator works into is 3,500 plus 10,000 or 13,500 ohms. Then, the resistance the gate-pulse generator works into is 5,500 ohms. The output resistance will be R_L in parallel with r_p during the pulse and R_L between pulses. From Drawing No. A-30205, $\bar{r}_p$ is 7000 ohms when e_{c_1} is 2 volts. Therefore, the output resistance will be 1,700 ohms during the pulse and 2,200 ohms between pulses.

The electrode dissipations are listed in Table 2. Notice that for both cases the dissipation is well below the allowable dissipation.

The performance of the gate circuit as illustrated by the

TABLE 3

	e_{i} = 13V, e_{g} = 0			e_{i} = 13V, e_{g} = 30V		
	e V	i ma	P w	e V	i ma	P w
CONTROL GRID	1.1	0.68	0.000,8	2	0.5	0.001
SCREEN	50	7.5	0.4	50	4.0	0.2
SUPPRESSOR	-10	0	0	10	1.5	0.015
PLATE	100	0	0	77	10.5	0.82

Electrode Dissipation - 6AS6 Gate Circuit - E_{cc_2} = 80 V

waveforms of Drawing No. A-30211. These data are also plotted as experimental points in Drawings No. A-30209 and No. A-30210.

The 6AS6 gate circuit is also discussed in Reference F.

D. 6SA7 Gate Circuit - The pentagrid gate circuit of Drawing No. A-30212 may employ a type 6SA7 tube. The low-current properties of this tube make it less desirable for obtaining pulses with short rise and fall times. An analysis of the 6SA7 gate circuit may be found in Reference E. The circuit is also discussed in Reference F.

E. Cathode-Coupled Gate Circuit - A cathode coupled gate circuit is shown in Drawing No. A-30213. The gate circuit consists of two cathode followers placed in parallel with a common cathode resistor. The grids are returned to ground or some positive voltage so that both tubes are normally conducting. The application of a negative pulse to V_1 will cutoff that tube but will cause little change in voltage at the output because V_2 will draw more current. If a negative gatepulse is applied to cutoff V_2 also, the input pulse will appear at the output as a negative pulse. This gate circuit is described in Reference B.

F. Two-Triode Gate Circuit - A two-triode gate circuit is shown in Drawing No. A-30214. Tubes V_1 and V_2 are normally conducting and have a common load resistor. Tube V_3 is directly coupled to the plates of V_1 and V_2. The supply voltages, E_{bb_1}, E_{bb_2}, and E_{cc_2}, are chosen so that V_3 will not conduct unless both V_1 and V_2 are cutoff. The output pulse will also be negative. As long as the input pulse and the gate pulse are of sufficient amplitude to cut off V_1 and V_2, the output-pulse amplitude will be independent of the amplitudes of the input and gate pulses. A modification of this gate circuit was tested in the laboratory; the circuit is shown in Drawing No. A-30215. With an input

pulse and gate pulse greater than 5 volts the output pulse was 13 volts. The gate circuit introduced a rise time of 0.07 μs and a fall time of 0.05 μs on a nearly rectangular 0.25-μs input pulse.

G. Screen Gate Circuit - A gate circuit employing a pentode with the gate pulse applied to the screen is shown in Drawing No. A-30216. This gate circuit, employing the 6AK5 and 6SJ7, is discussed in Reference F. The gate-pulse amplitude required and the current drawn by the screen are large, making the gate circuit less desirable.

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APPENDIX

LIST OF SYMBOLS

SYMBOL	DEFINITION
C_s	Shunt capacitance
e_b	Total plate voltage
E_{bb}	Plate supply voltage
e_c	Total grid voltage
E_{cc}	Grid supply voltage or bias voltage
e_g	Gate-pulse amplitude
e_i	Input-pulse amplitude
E_{kk}	Cathode bias voltage
e_o	Output-pulse amplitude
i_b	Total plate current
i_c	Total grid current
p	Instantaneous power
r_b	Static back resistance of diode
r_f	Static forward resistance of diode
R_g	Internal resistance of gate-pulse generator
R_i	Internal resistance of input-pulse generator
r_p	Static plate resistance
V	Vacuum tube

LIST OF DRAWINGS

Drawing No.	Title
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A-30196	Control-Grid Characteristic - 6AS6 - E_{cc_2} = 100V
A-30197	Suppressor Characteristic - 6AS6 - E_{cc_2} = 100V
A-30198	Circuit for Measuring Control-Grid Characteristic 6AS6 - E_{cc_2} = 100V
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A-30200	6AS6 Gate Circuit - E_{cc_2} = 100V
A-30201	Output vs. Input-6AS6 Gate Circuit - E_{cc_2} = 100V
A-30202	Output vs. Gate - 6SA6 Gate Circuit - E_{cc_2} = 100V
A-30203	Waveforms for 6AS6 Gate Circuit - E_{cc_2} = 100V
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A-30205	Control-Grid Characteristic - 6AS6 - E_{cc_2} = 50V
A-30206	Suppressor Characteristic - 6AS6 - E_{cc_2} = 50 V

LIST OF DRAWINGS(CONT'D)

Drawing No.	Title
A-30207	Circuit for Measuring Control-Grid Characteristic - 6AS6 - E_{cc_2} = 50 V
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A-30209	Output vs. Input - 6AS6 Gate Circuit - E_{cc_2} = 50V
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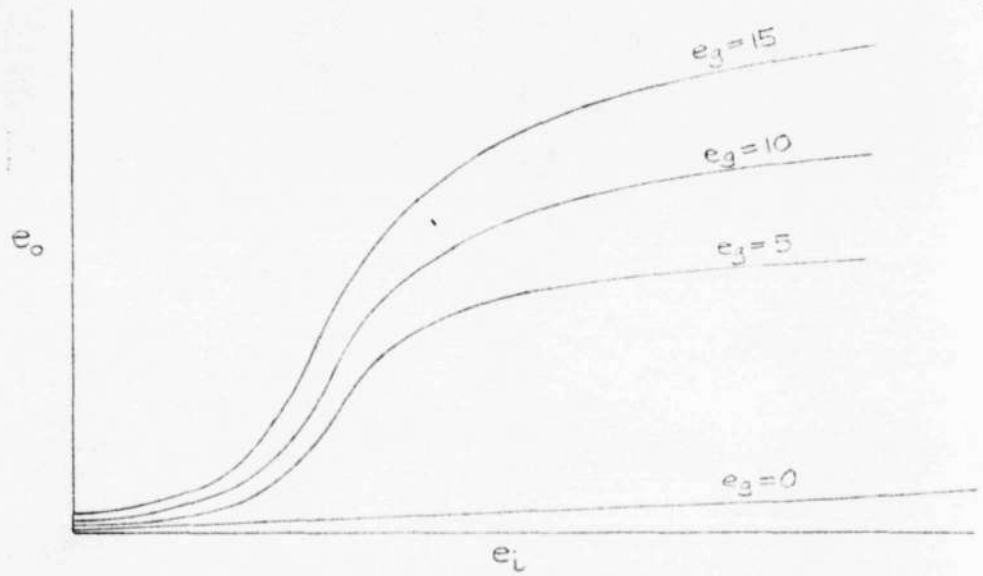
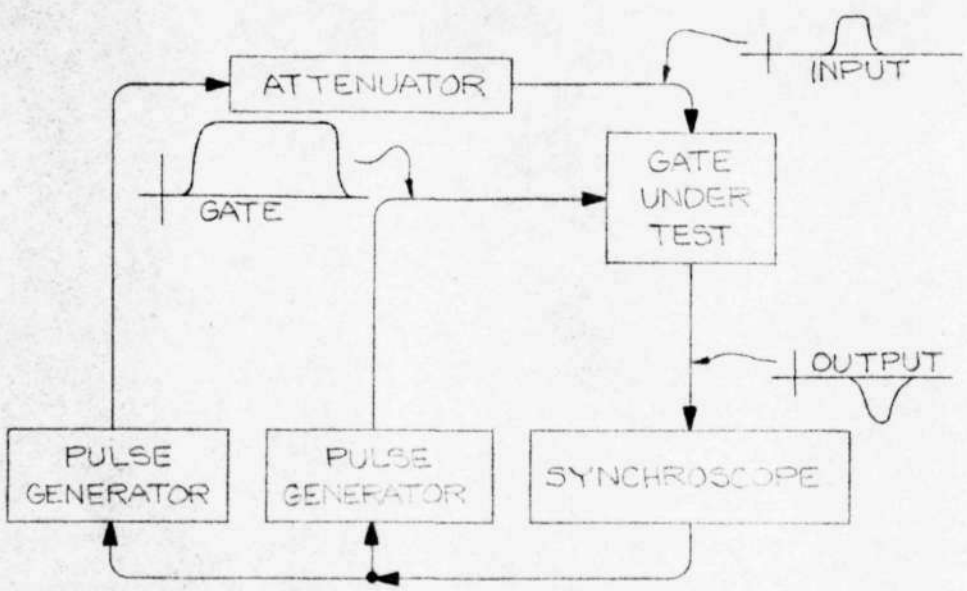
A-30213	Cathode-Coupled Gate Circuit
A-30214	Two-Triode Gate Circuit
A-30215	Modified Two-Triode Gate Circuit
A-30216	Screen Gate Circuit



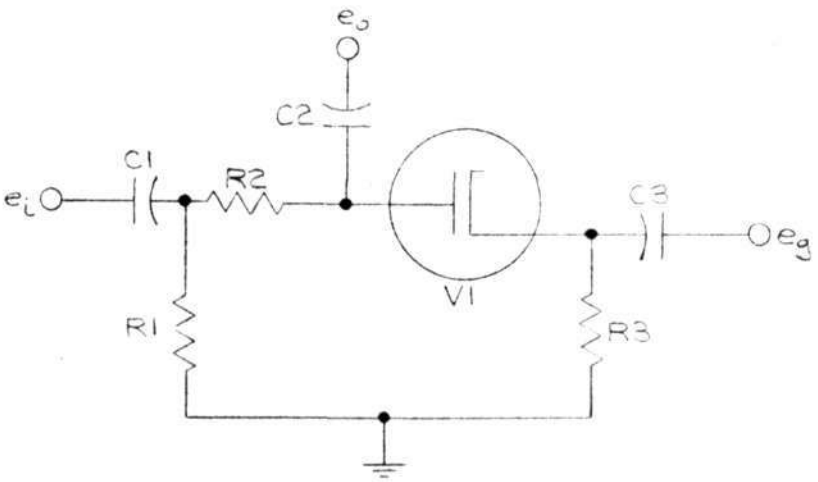
GATE-CIRCUIT CHARACTERISTICS

USED IN 6345 REPORT R-109



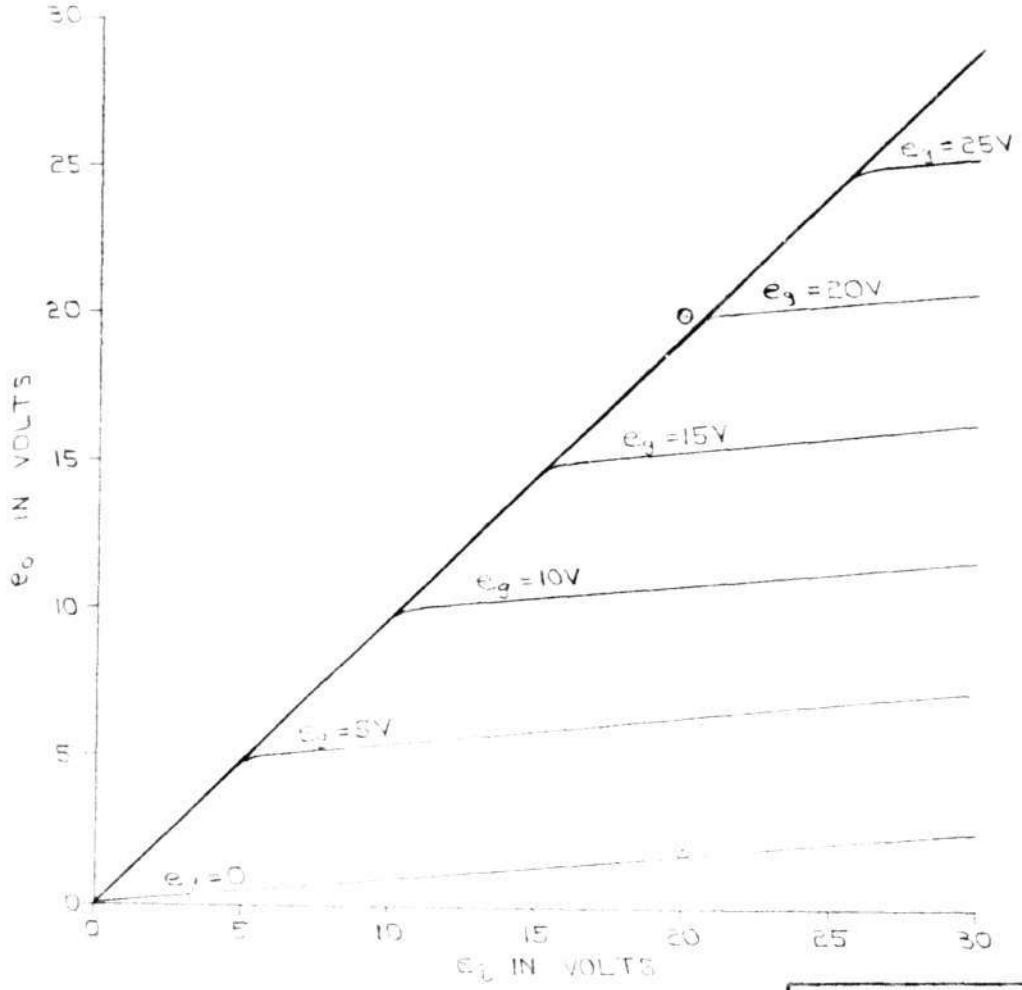
ARRANGEMENT FOR TESTING GATE CIRCUITS

USED IN 6345 REPORT R-109



DIODE GATE CIRCUIT

R1 = R3 = 100Ω
R2 = 2200Ω
V1 REPLACED BY IN34



CHARACTERISTICS OF AEG-
DIODE GATE UNIT

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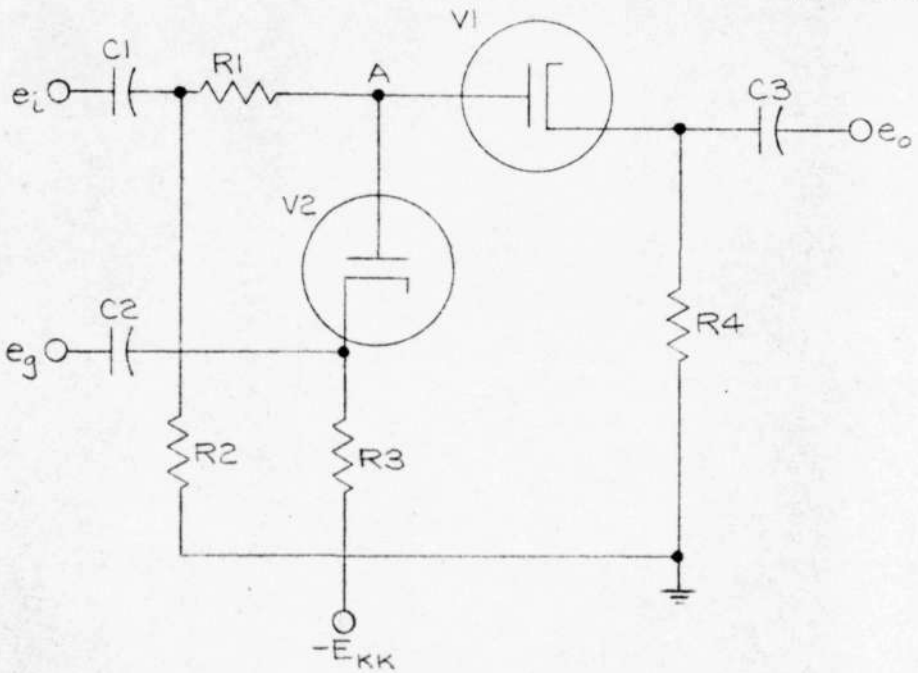
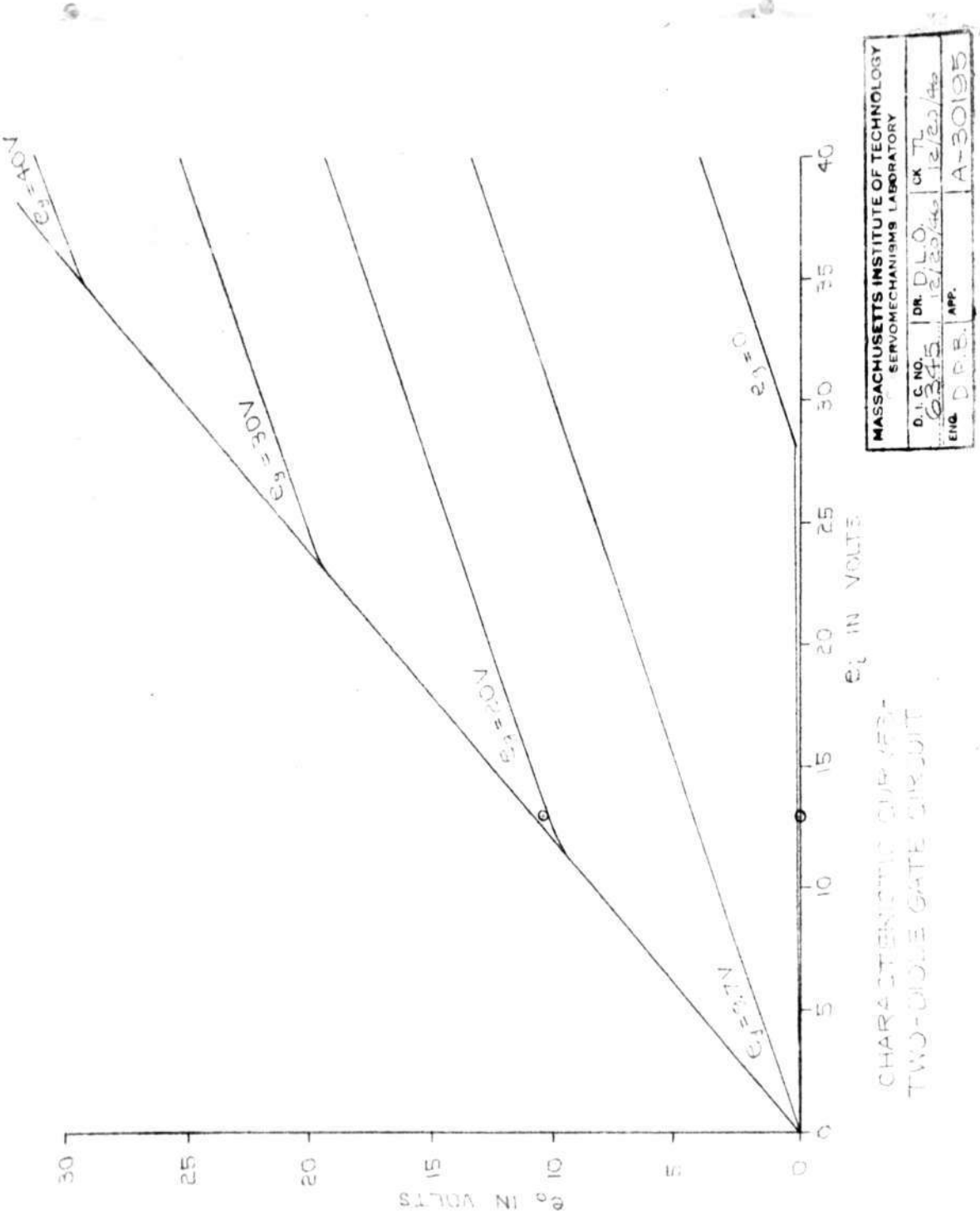
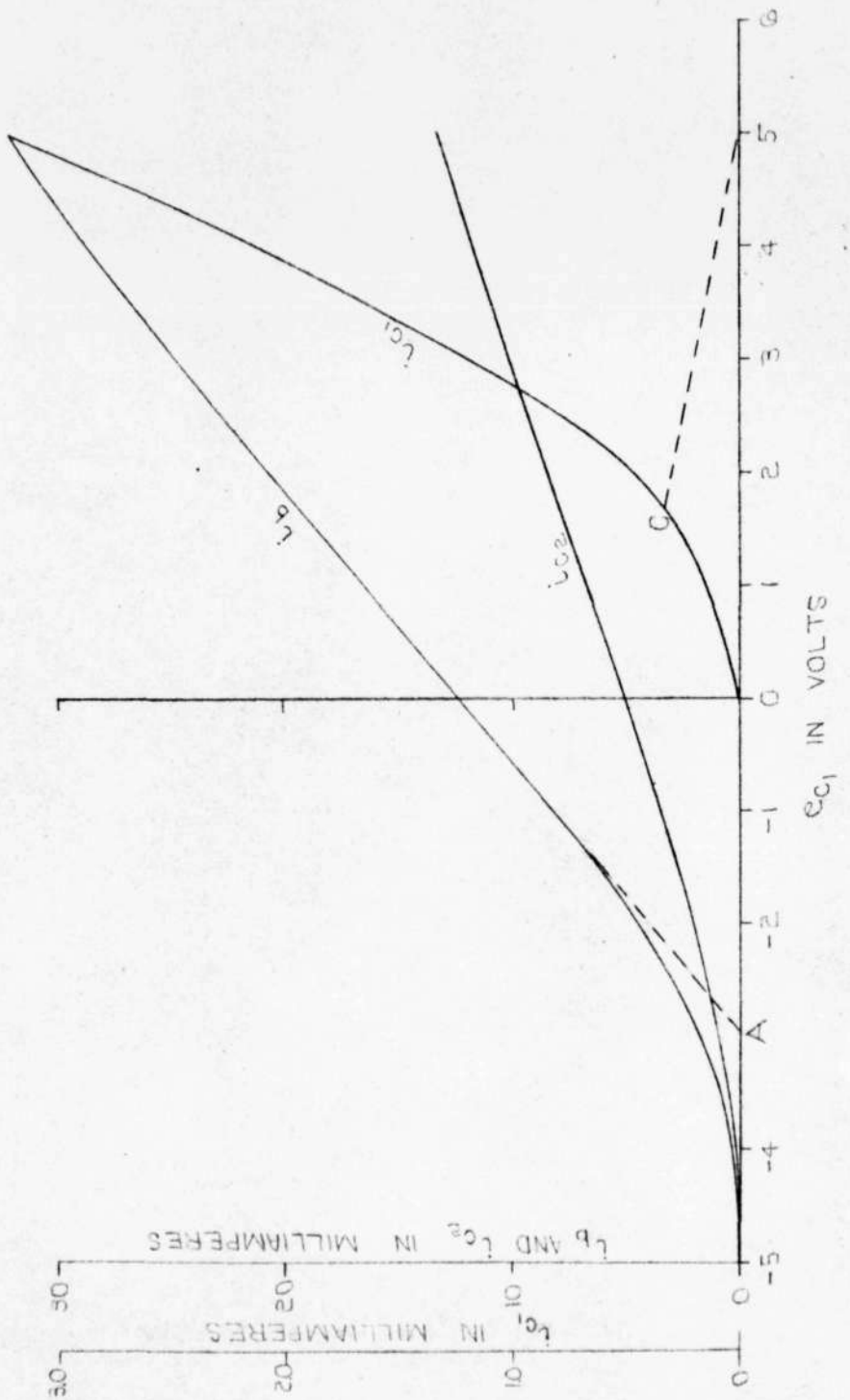
ENG. D.R.S.	APP.	A-30123



TWO-DIODE GATE CIRCUIT

C1 = C2 = 0.1 MFD
R1 = R3 = 330Ω
R2 = 10,000Ω
R4 = 2200Ω
E_{KK} = 10V
V1 AND V2 REPLACED BY IN34'S





CONTROL-GRID CHARACTERISTIC -
GAS G - E_{c_2} = 100V

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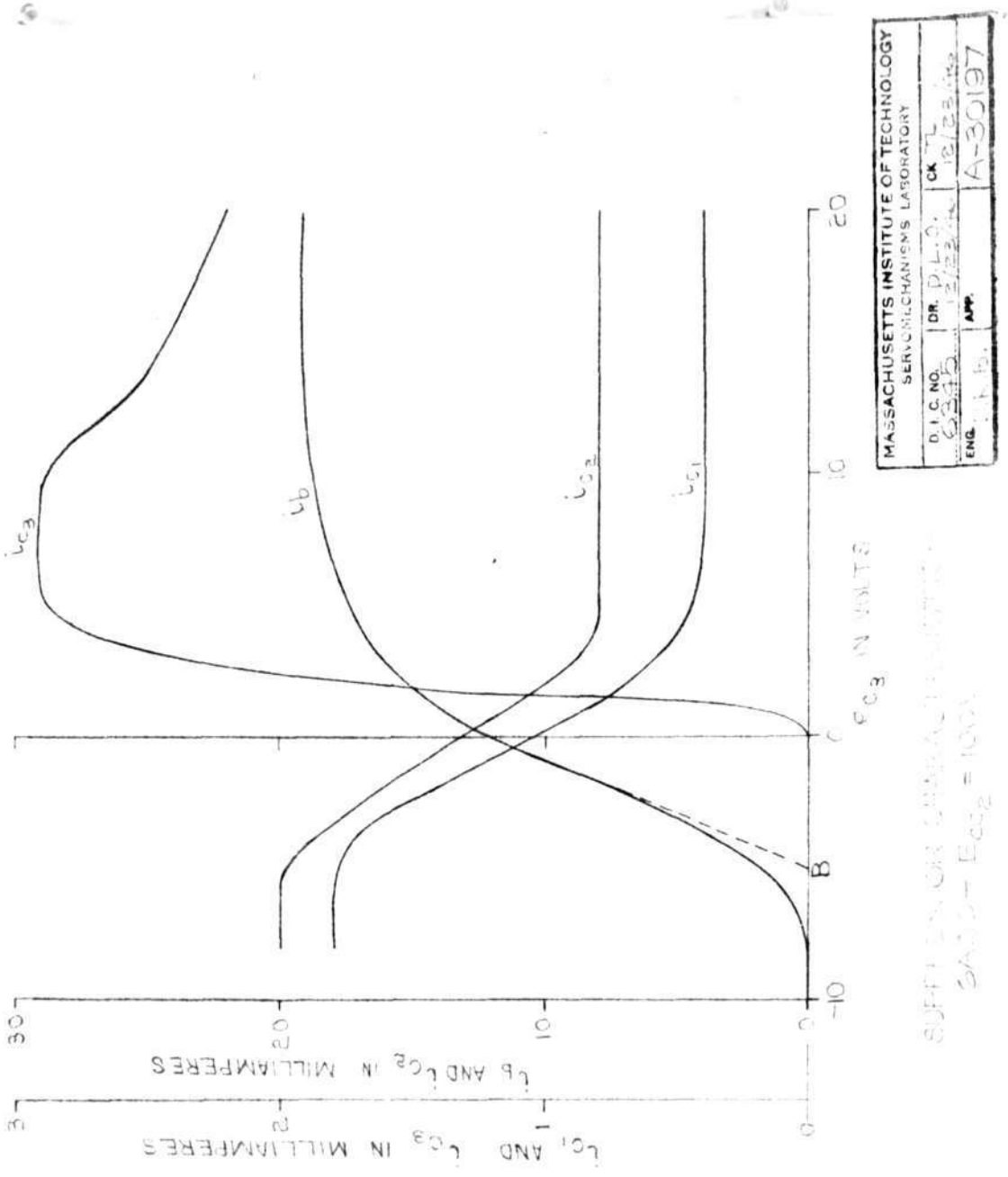
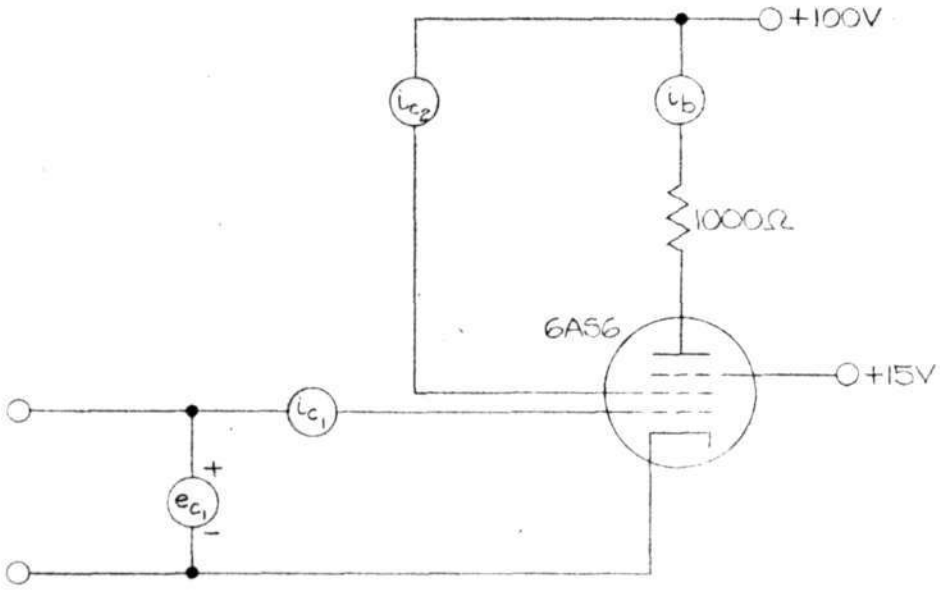
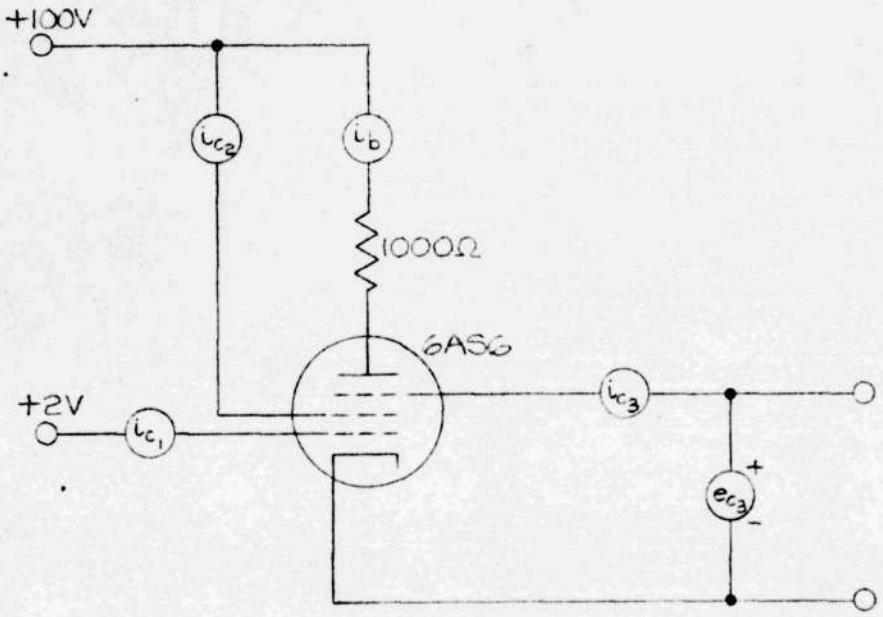


A-30197

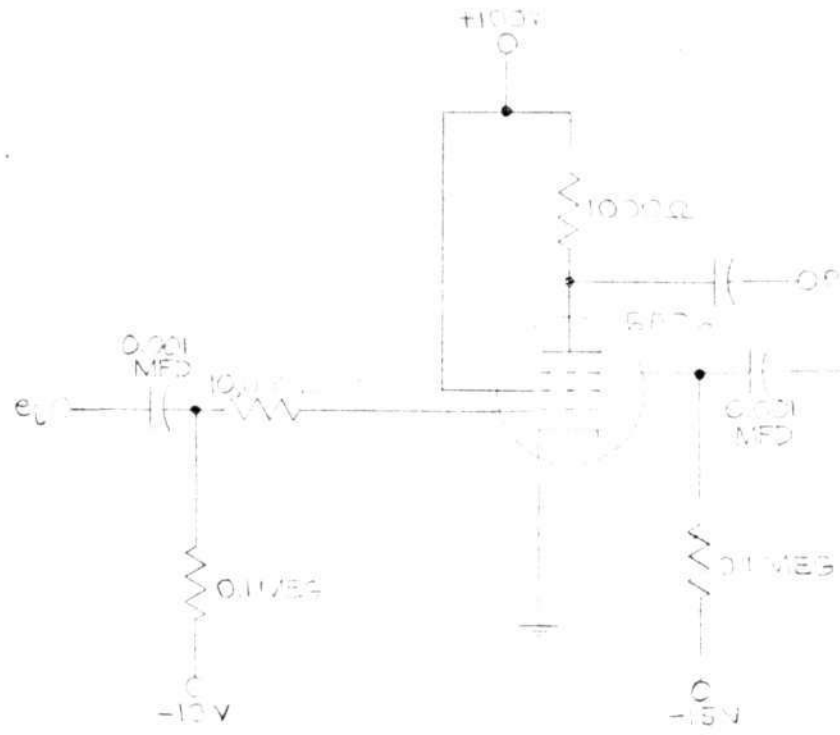


CIRCUIT FOR MEASURING CONTROL-GRID CHARACTERISTIC
6AS6 - E_{cc_2} = 100V

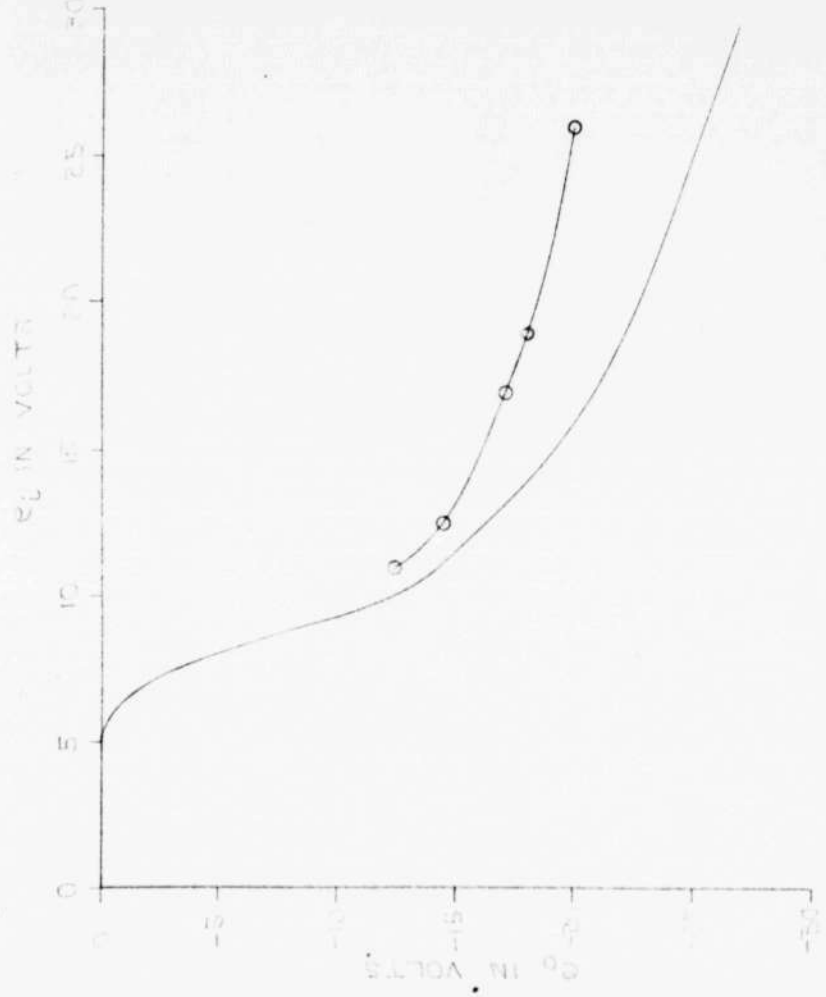


CIRCUIT FOR MEASURING SUPPRESSOR CHARACTERISTIC
6AS6 - E_{cc_2} = 100V

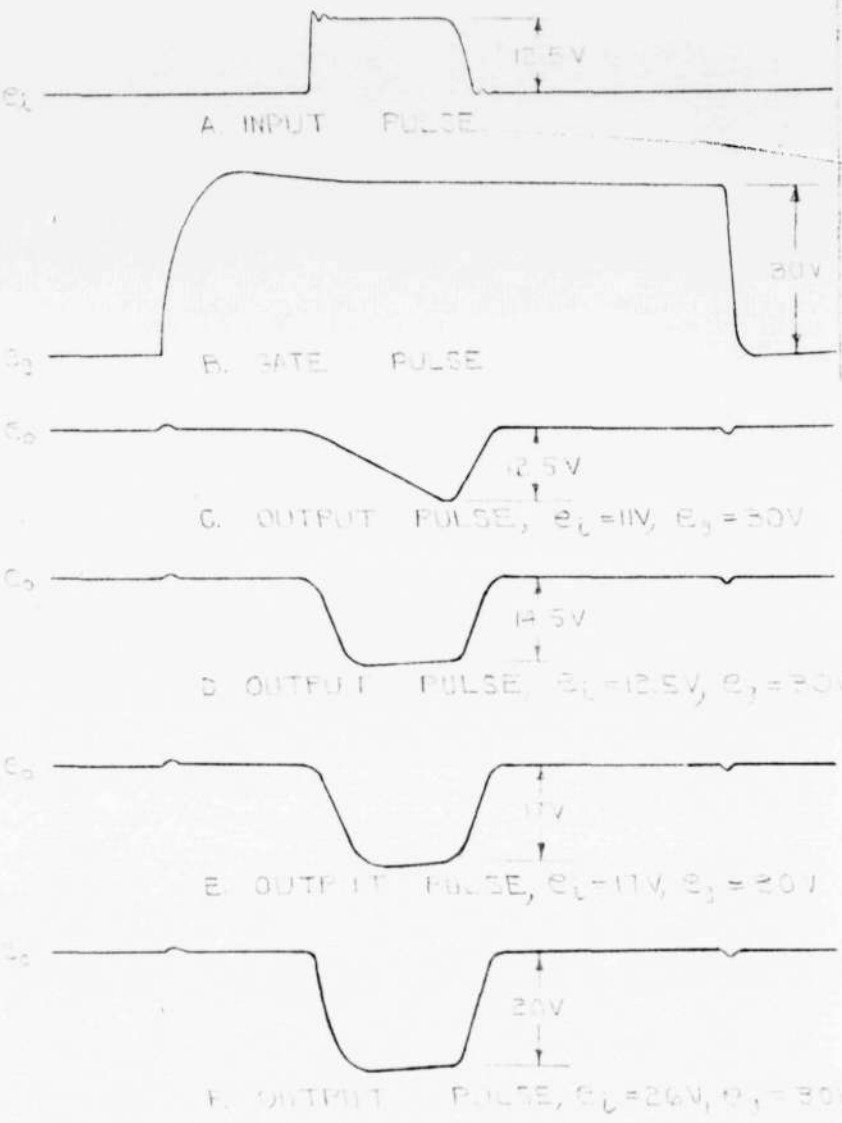
USED IN GRL REPORT R-109



GRID GATE ... E_{cc} = 100 V



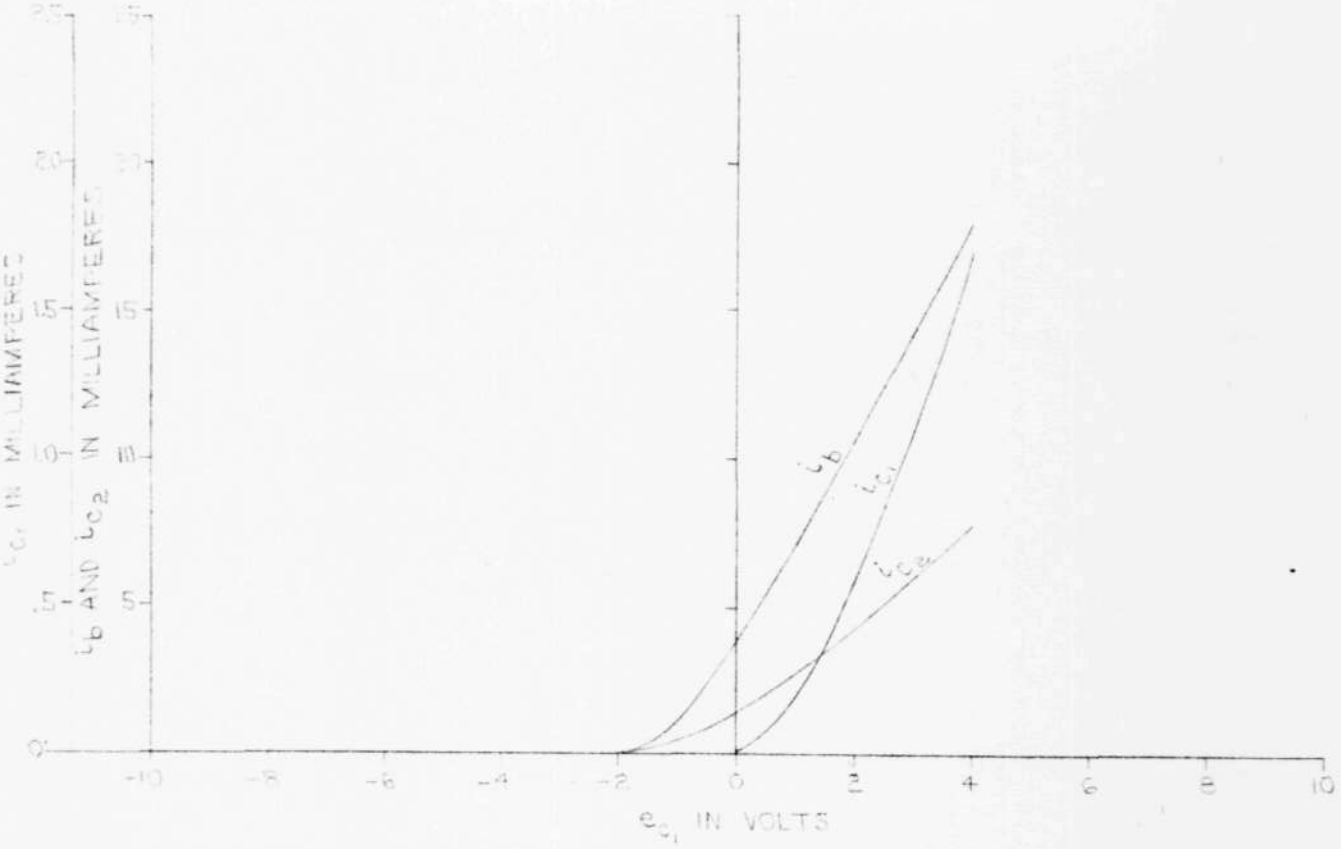
OUTPUT VS. INPUT -
GATED GATE CIRCUIT
E_{bb} = 100V



WAVEFORMS FOR GAGE GATE CIRCUIT - E_{cc_2} = 100V

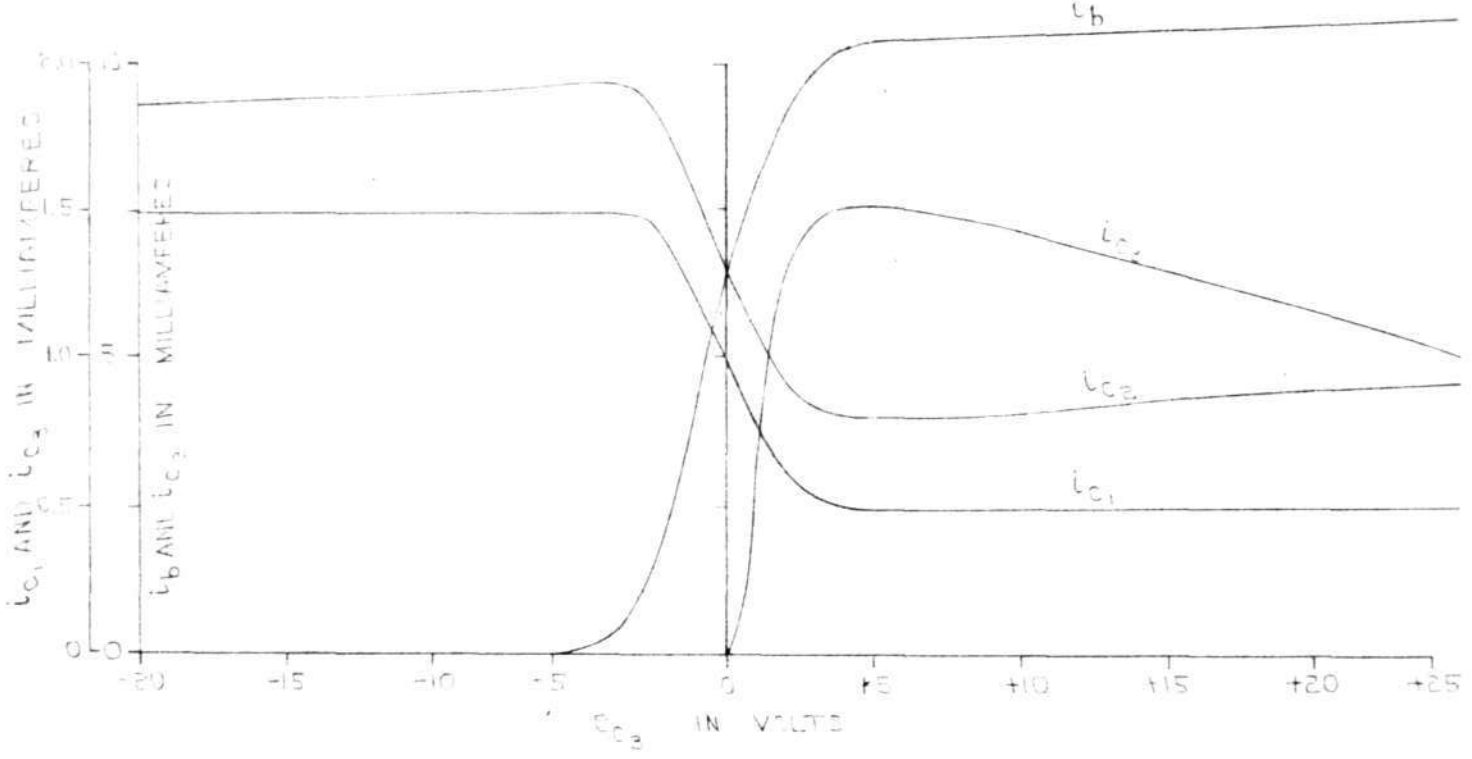
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY

DWG NO.	DR. TL	CK
6345	12/23/46	
ENG. D.R.B.		A-30204



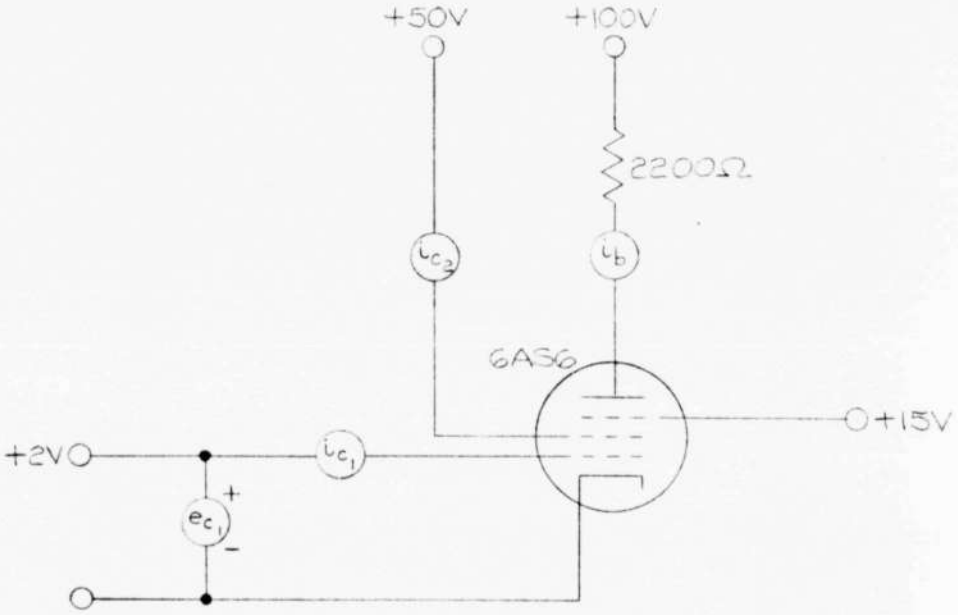
CONTROL-GRID CHARACTERISTIC - GAS6 - E_{cc_2}=50V

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
DWG. NO. 6345	CK. D.L.O. 12/24/46	CK. TL 12/24/46
ENG. D.R.B.	DR.	A-30205



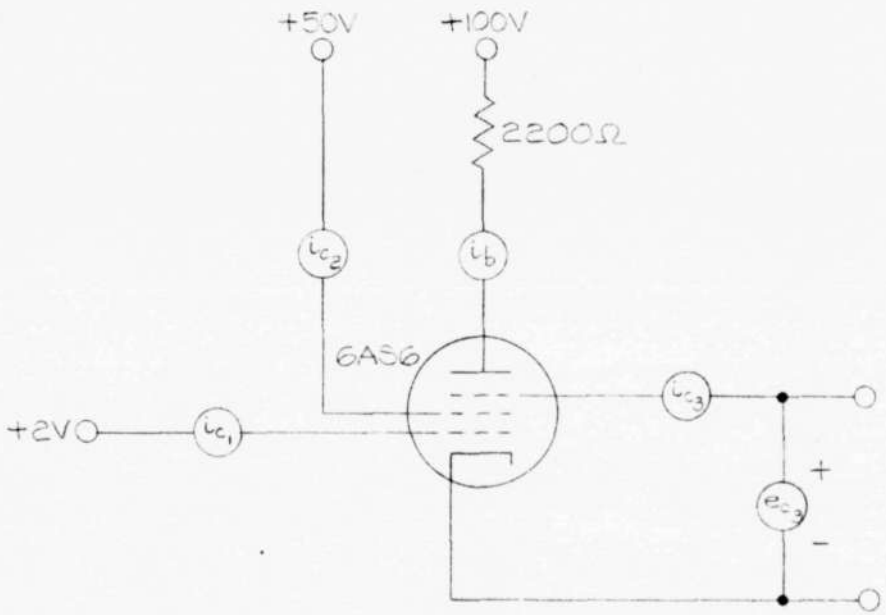
SUPPRESSOR CHARACTERISTIC - $6AS6 - E_{mc_2} = 55.$

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. I. C. NO. 6295	DR. D.L.Q. 12/24/46	CK. TL 12/27/46
ENG. D.R.B.	APP.	A-30206



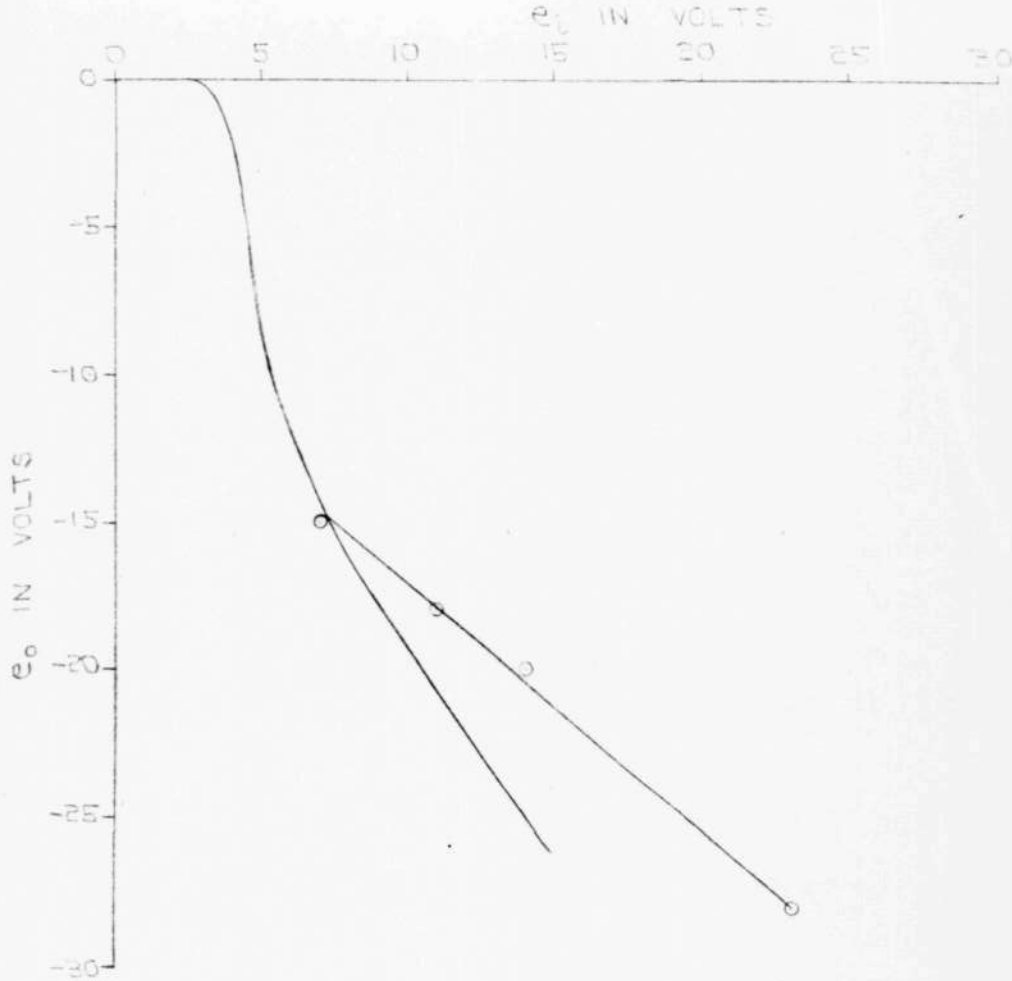
CIRCUIT FOR MEASURING CONTROL-GRID CHARACTERISTIC

6AS6 - E_{cc_2} = 50V



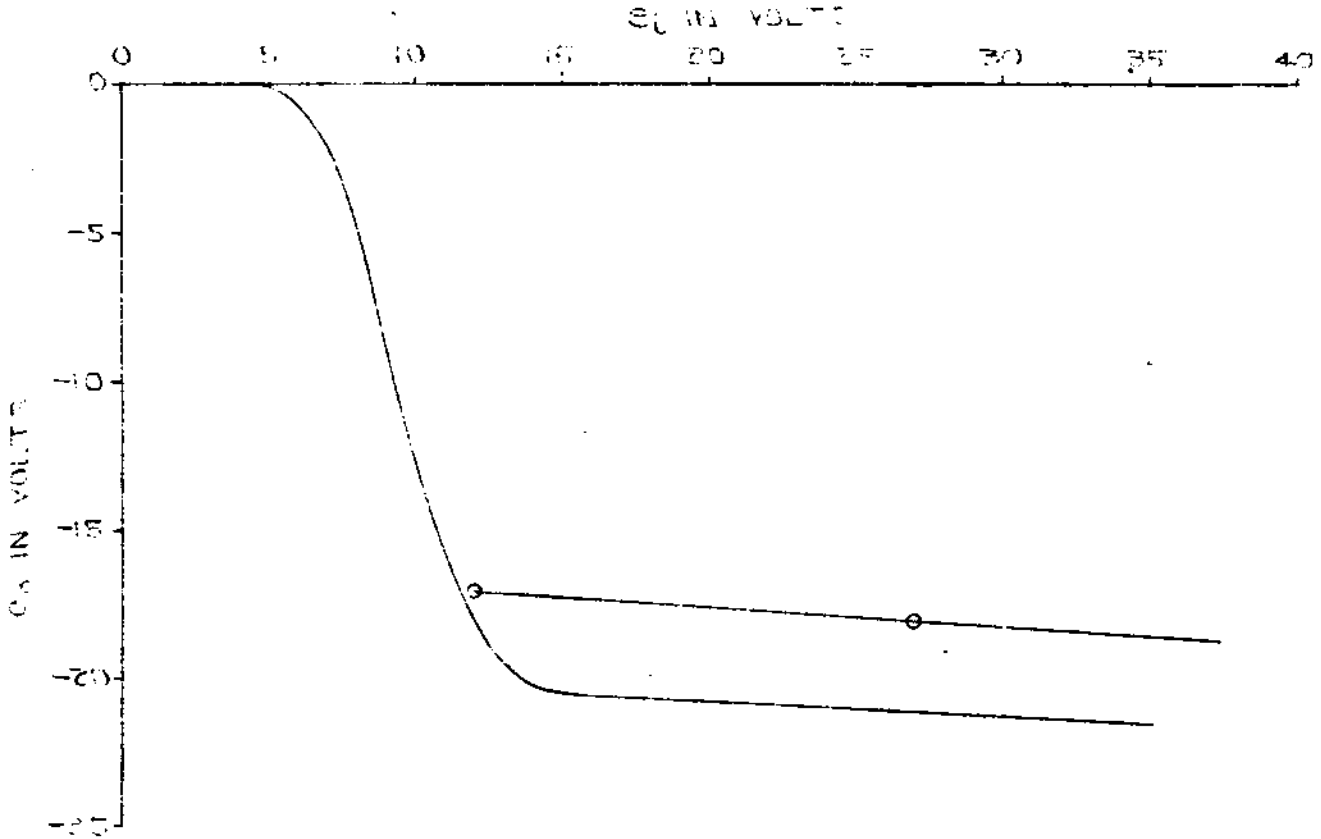
CIRCUIT FOR MEASURING SUPPRESSOR CHARACTERISTIC

6AS6 - E_{cc_2} = 50V

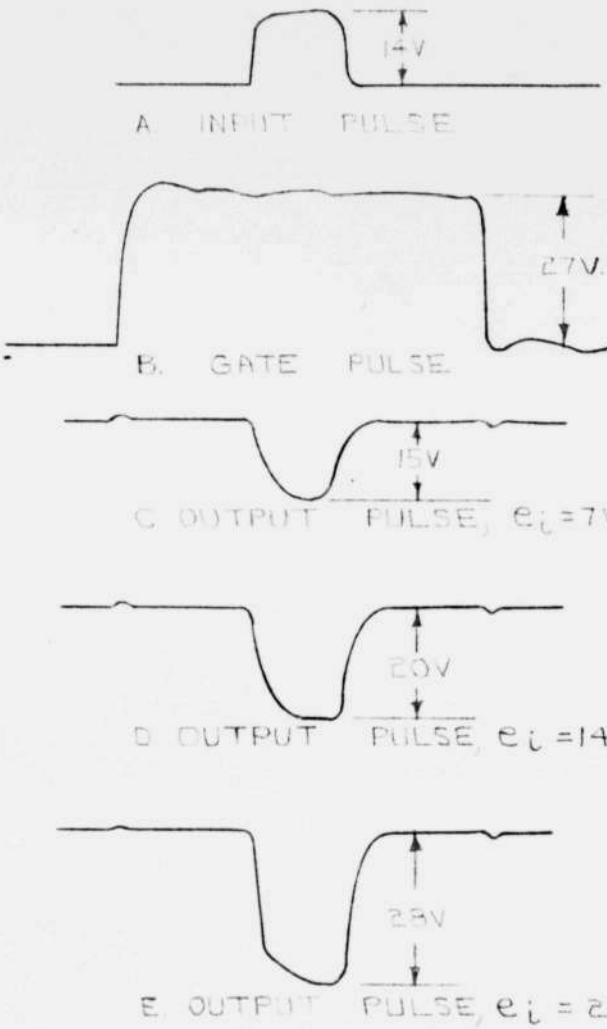


OUTPUT VS INPUT -
6AS6 GATE CIRCUIT -
$E_{cc_2} = 50V$

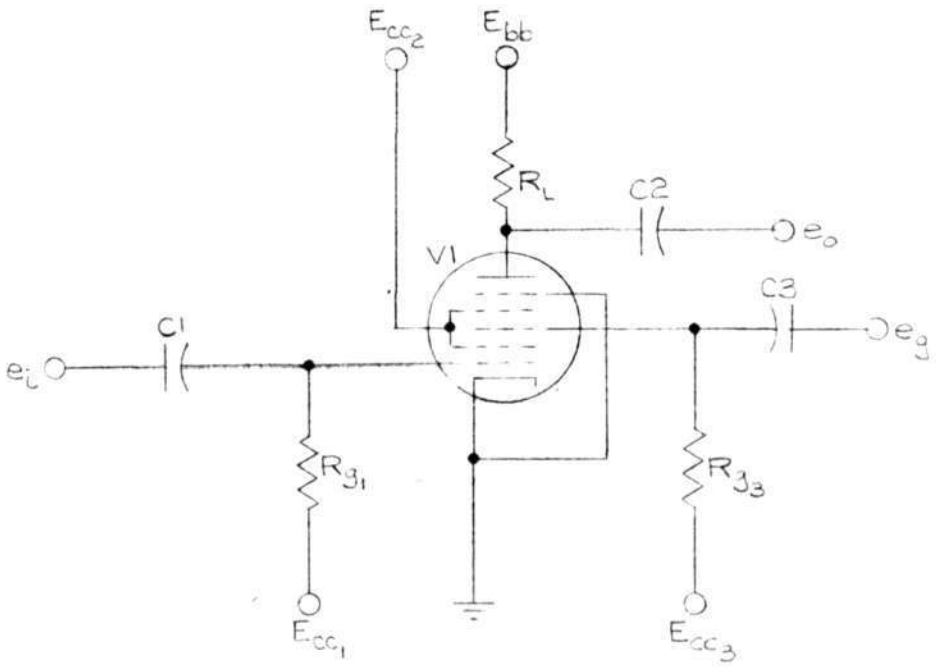
MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. I. C. NO. 6345	DR. D.L.O. 12/26/49	CK. T.L. 12/26/49
ENG. D.R.B.	APP.	A-30209



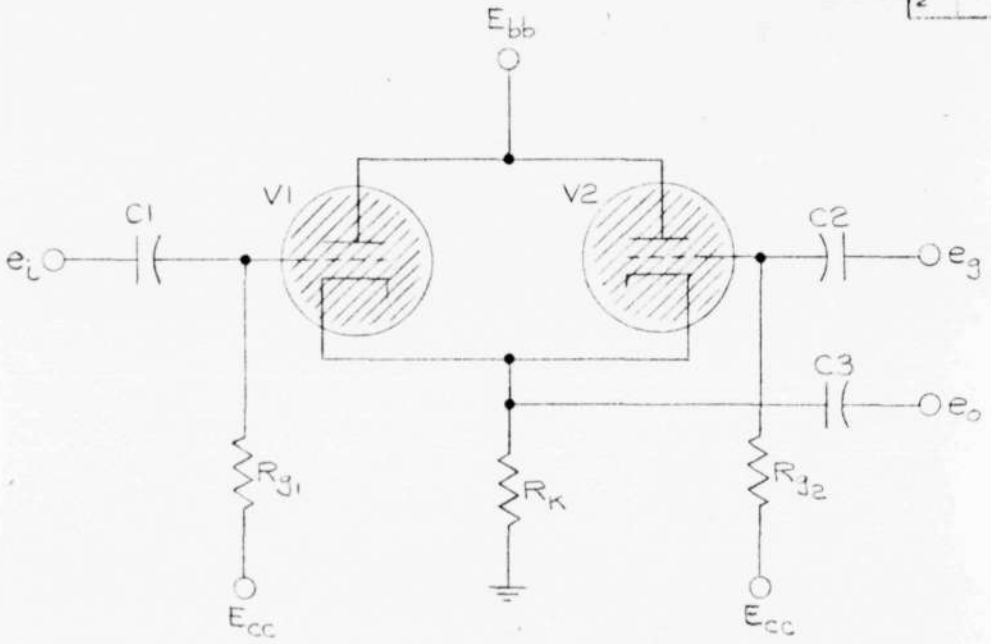
OUTPUT VS. GATE - 6AS7 GATE CIRCUIT - E_{cc_2}=50V



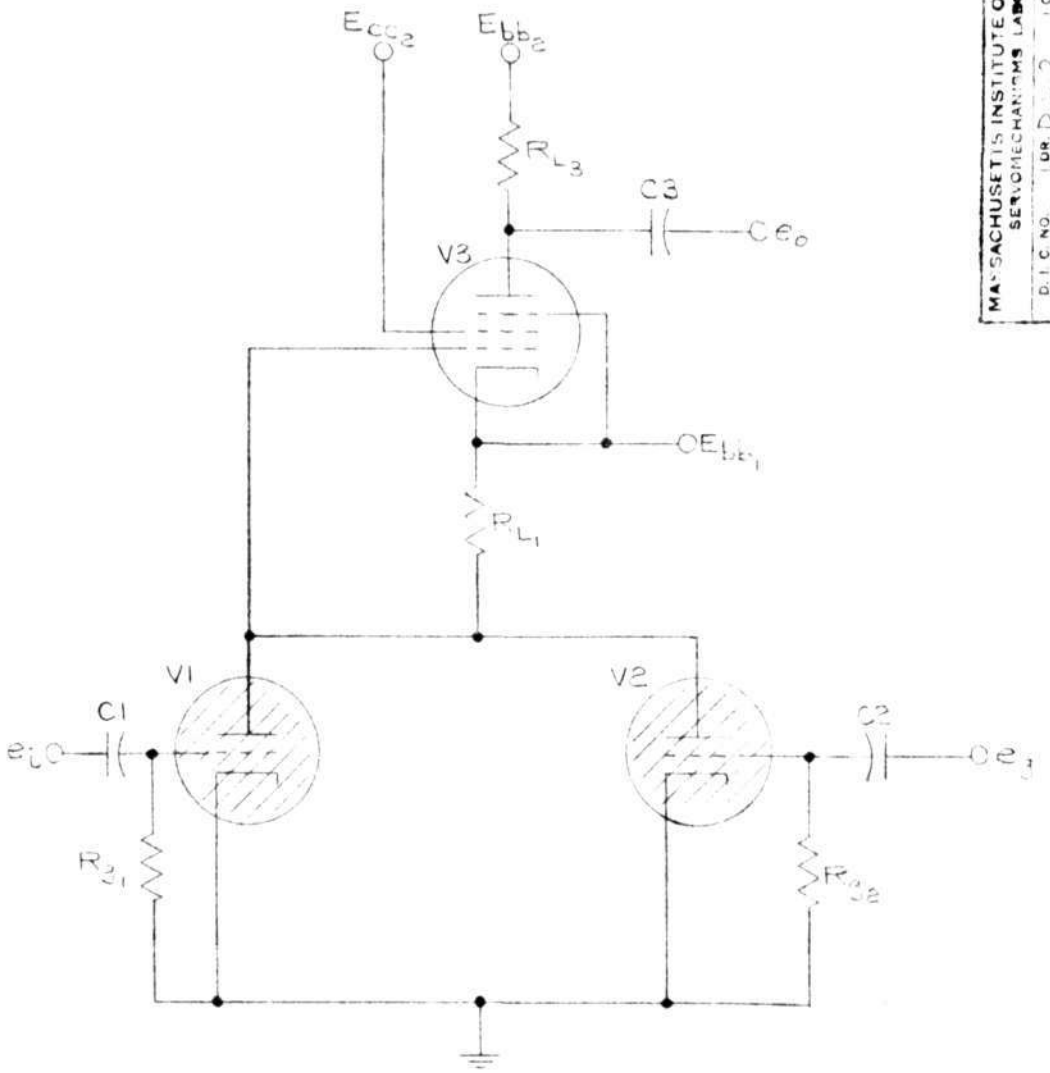
WAVEFORMS - 6AS6 GATE CIRCUIT - E_{cc_2} = 50V



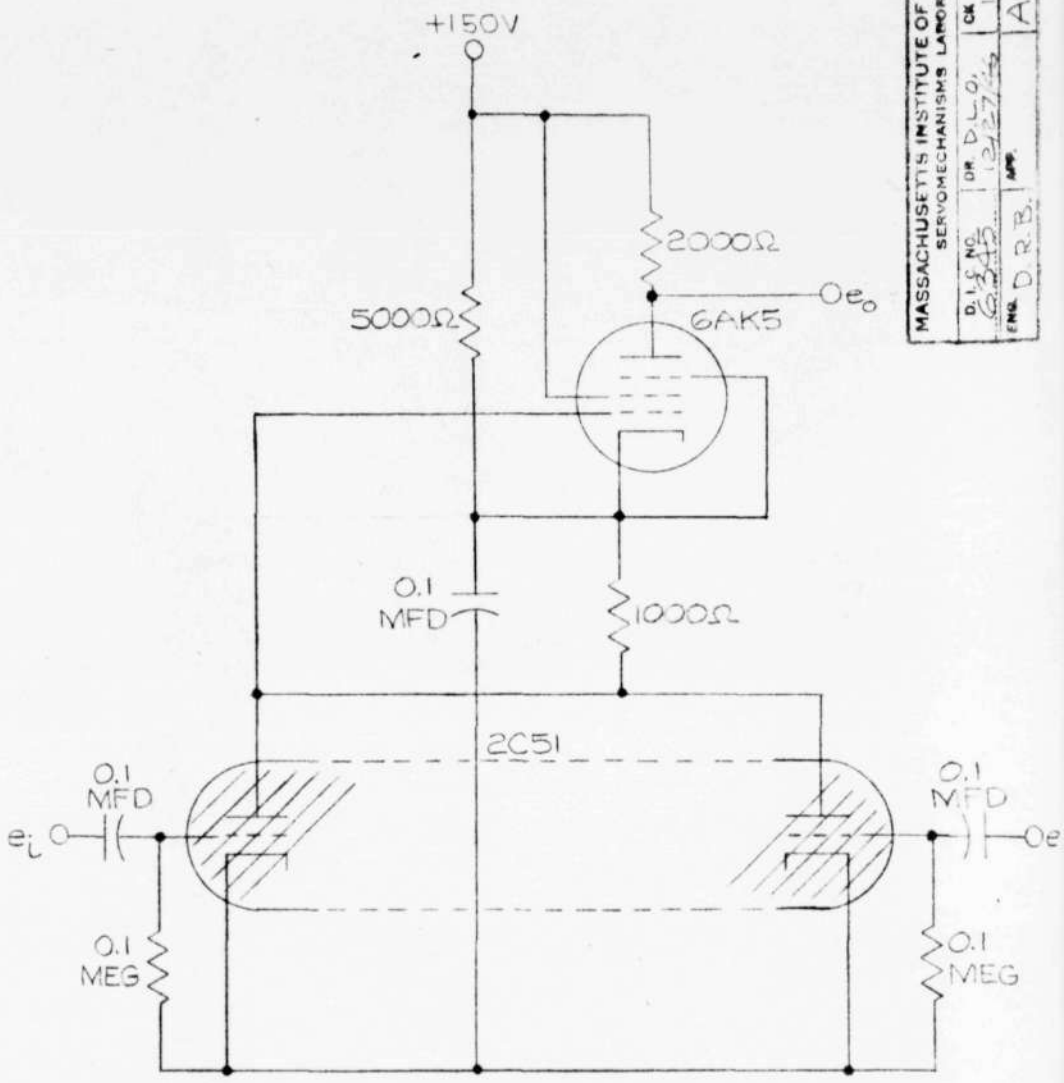
PENTAGRID GATE CIRCUIT



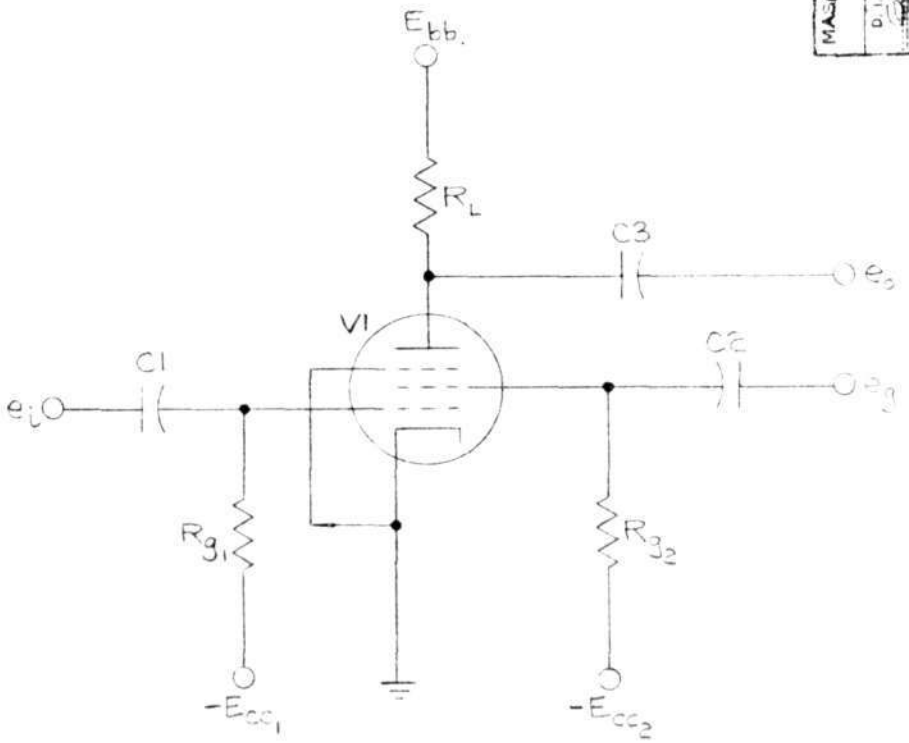
CATHODE-COUPLED GATE CIRCUIT



TWO-TRIODE GATE CIRCUIT



MODIFIED TWO-TRIODE GATE CIRCUIT



SCREEN GATE CIRCUIT

ENGINEERING NOTES NO. E-44

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: 6345 Engineers 6345

FROM: Norman H. Taylor

SUBJECT: Duty Cycle for Various Functions

DATE: July 8, 1947

Using pulses of .05 microsecond duration throughout the system has been proposed as being a desirable change in WWI.

The duty cycle on the attached list of control pulses has been estimated using these .05 microsecond pulses and an estimated time of 12 microseconds as the duration of a cycle of operation and 20 microseconds when multiplication is encountered.

The duty cycles to be encountered are considerably more favorable than has been considered in most cases and may take considerable burden off transformer design and tube dissipation limits if advantage can be taken of this factor.

The question marks on:

A-Register to Accumulator
Shift Right
Shift Left

indicate that some doubt exists as to the duty cycle to which the gate tube is subject. Methods of coupling to improve these three are under discussion.

ESTIMATED DUTY CYCLE OF VARIOUS FUNCTIONS IN WWI

	No. per cycle	Length of cycle	Pulse Length	Ratio off/on
P.C. to Bus	2	12	.05	120/1
P.C. to Check Register	2	12	.05	120/1
Program Register to Bus	1	12	.05	240/1
Read-in Gate C.S.	6	12	.05	40/1
Read-in Gate St. S.	6	12	.05	40/1
Control Switch to Bus	1	12	.05	240/1
Storage Switch to Bus	3	12	.05	80/1
Storage Readout	3	12	.05	80/1
Storage to Check Register	2	12	.05	120/1
Step Counter to Bus	2	12	.05	120/1
Bus to Step Counter	6	12	.05	40/1
Bus to Check	6	12	.05	40/1
Add to Program Counter	3	12	.05	80/1
Start Delay Counter	3	12	.05	80/1
Clear Control Switch	3	12	.05	80/1
Clear Storage Switch	3	12	.05	80/1
Clear A-Register	2X	12	.05	120/1
Clear Program Register	2X	12	.05	120/1
Clear Step Counter	2X	12	.05	120/1
Transfer Check	3	12	.05	80/1
A Register to Accu.	17	20	.05	25/1 ? 1
Accu. to Bus	1	12	.05	240/1
Accu. to Check Bus	1	12		240/1
Accu. to B-Register	1	12	.05	240/1
Carry	1	12	.05	240/1
Roundoff	1	12	.05	240/1
Product Sign	1	12	.05	240/1
Accu. Sign	1	12	.05	240/1
A. R. Sign	1	12	.05	240/1
Multiply	1	12	.05	240/1
Arithmetic Check	1	12	.05	240/1
Compare	1	12	.05	240/1
Shift Left	2			? 1
Shift Right	?			? 1
Shift and Carry	16	20	.05	25/1
Divide	1	12-38	.05	240/1
Special Add	1	12	.05	240/1
Bus to Display	1	12	.05	240/1

Norman H. Taylor

NHT:has

ENGINEERING NOTES NO. E-45

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: Engineers of Project 6345

FROM: David R. Brown

SUBJECT: Time-Pulse Distributor

DATE: June 30, 1947

6345

Illustrations:
SD-39234-1
SD-39233-2
A-30621
A-30622

A two-channel time-pulse distributor has been constructed and tested in the laboratory. The basic method used is that proposed for the eight-channel time-pulse distributor needed in the control of WWI.

Block Diagram

The block diagram of the proposed eight-channel time-pulse distributor is shown in Sketch SD-39234. The distributor is divided into eight sections; each consists of a flip-flop and two gate tubes. Assume that the distributor has been reset. The first seven flip-flops are then zero and the eighth flip-flop is one. The eighth flip-flop holds the two gate tubes in the first section open; all the other gate tubes are closed. The first time-pulse goes through GT09 and appears at output terminal 1. The first time-pulse also goes through GT01, is delayed 0.25 microsecond by DE01, then sets FF01 and resets FF08. The next time-pulse goes through GT10 and GT02, etc. The eighth time-pulse goes through GT08 and is delayed 0.25 microsecond to set FF08 and reset FF07. It is delayed an additional 0.5 microsecond by DE09 and resets the first six flip-flops. This provides an automatic reset each cycle. The flip-flops must switch in 0.5 microsecond for this reset to function. The distributor may also be reset by a pulse from an external source.

Experimental Time-Pulse Distributor

The circuit diagram of the experimental two-channel time-pulse distributor is shown in Sketch SD-39233. The flip-flops employ 2C51 twin triodes and have a switching time of about 0.75 microsecond. The threshold trigger voltage is between two and four volts. A special circuit is used which permits the plate of the "off" tube to return to nearly the plate supply voltage, +10 volts. The gate tubes are then directly coupled to the flip-flops. One of the gate tubes in each section has a delay-line in the plate load circuit. The delayed negative pulse from that gate tube is used to switch the two flip-flops. Note that the gate tube in the first section has a 0.25-microsecond delay and

the gate tube in the second section has a 0.5-microsecond delay. The delay lines are terminated in 820 ohms in series with a 1N34. The other gate tube in each section has a one-to-one inverter transformer in its plate load. This gives a positive time-pulse at the output terminal of each channel. The 10-microhenry choke in parallel with a 1000-ohm resistor prevents ringing at the top of the pulse. The 1000-ohm resistor in series with a 1N34 prevents ringing at the tail of the pulse. A 1N34 from grid to cathode of each gate tube and a 1000-ohm series grid resistor prevent the gate tubes from being overdriven and permit a greater variation in the amplitude of the input pulses.

Waveforms at various points are shown in Drawings A-30621 and A-30622. The output pulses have more overshoot than is expected in service because of the extra capacitance added by the scope when the pulses were photographed. The output pulses with the transformer load removed and replaced by a single 1000-ohm resistor are also shown.

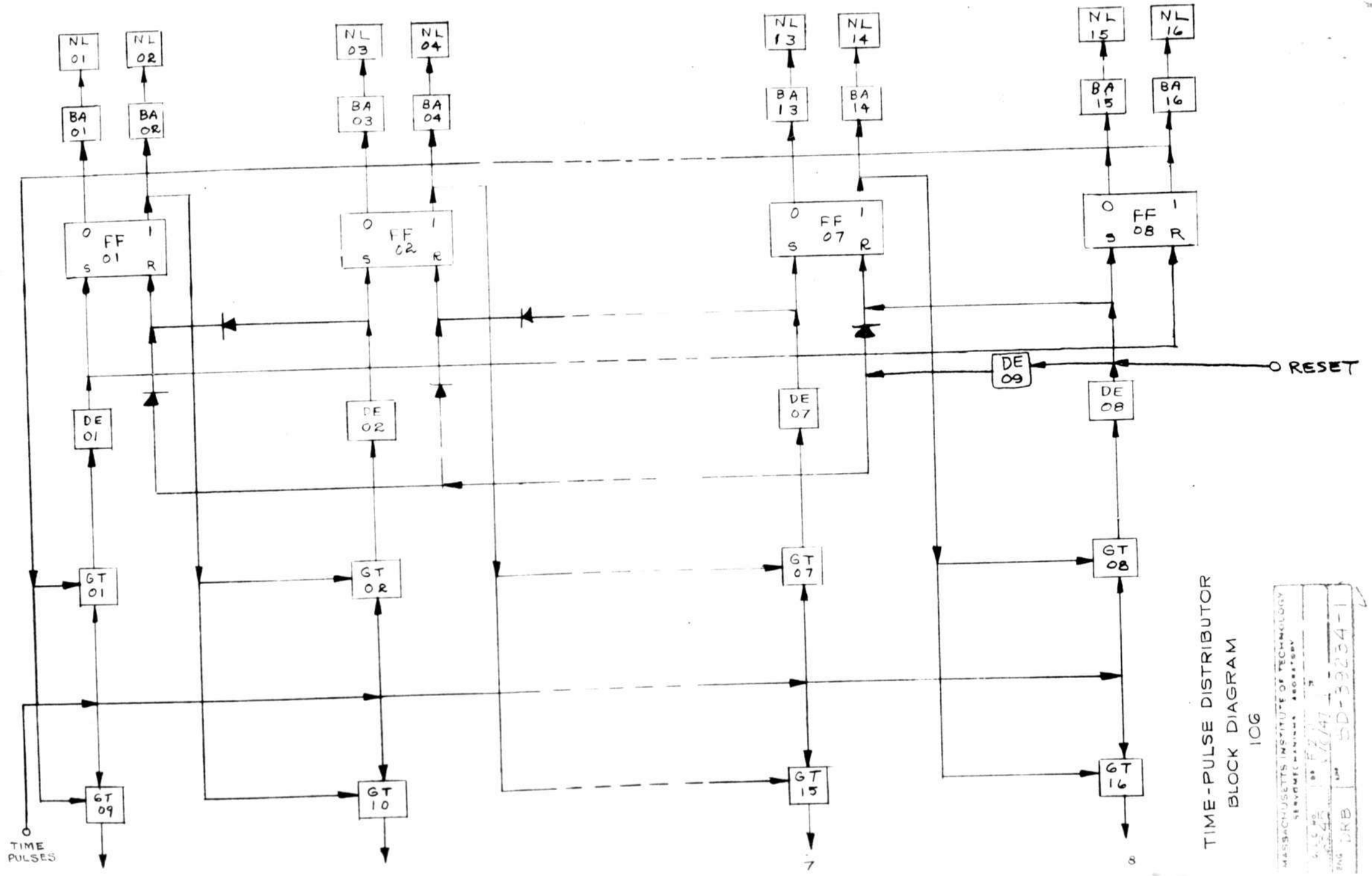
Eight-Channel Time-Pulse Distributor

The proposed eight-channel time-pulse distributor will have a slightly different delay circuit in the last section from that used in the experimental distributor as indicated by the block diagram. As stated previously, the flip-flops must have a switching time of 0.5 microsecond. This is necessary if the automatic reset is to function. A 7F8 flip-flop, or a flip-flop employing two 6AG7's, might be used. If a-c coupling is used between the flip-flop and the gate tubes, a trigger tube will be necessary for each flip-flop. Since the time-pulse distributor will not function during the regular complement-recomplement period, a-c coupling may be used, eliminating the +10V supply.

David R. Brown
David R. Brown

DRB:has:vb
July 2, 1947

SD-39234-1

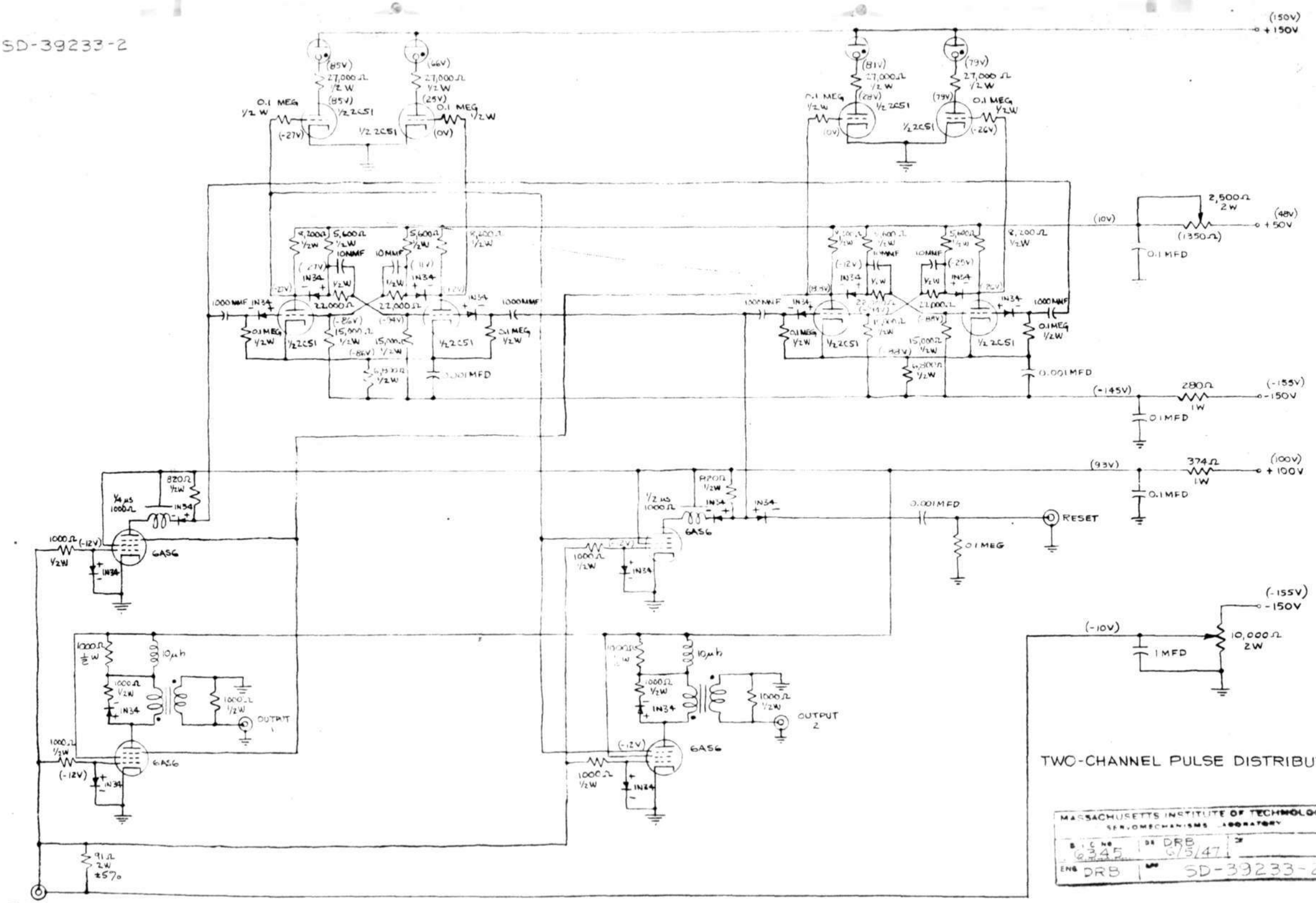


TIME-PULSE DISTRIBUTOR
BLOCK DIAGRAM
IOG

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
LINCOLN LABORATORY

DRN	CRB	SD-39234-1

SD-39233-2

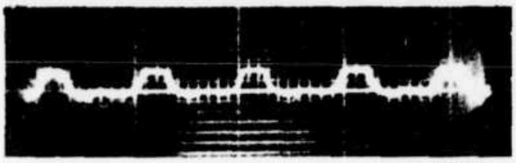


TWO-CHANNEL PULSE DISTRIBUTOR

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY	
B. C. NO. 6345	DR DRB 6/5/47
ENG DRB	SD-39233-2

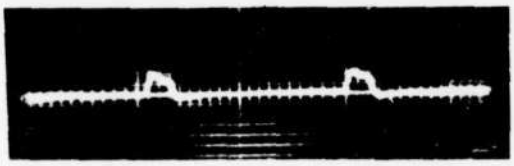
INPUT TIME PULSES

F-118-2



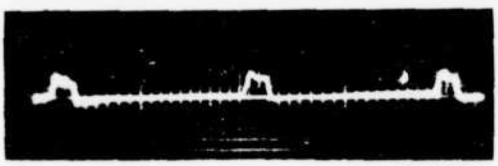
TIME PULSES AT GRID OF GATE TUBE

F-118-4



OUTPUT 1

F-118-5



OUTPUT 2

F-118-6

DELAYED PULSE FROM GATE TUBE IN FIRST SECTION

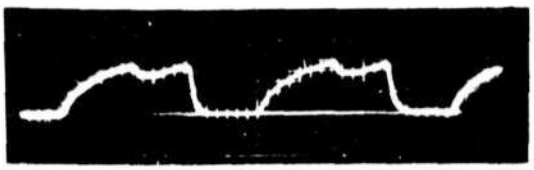
F-118-7

DELAYED PULSE FROM GATE TUBE IN SECOND SECTION

F-118-8

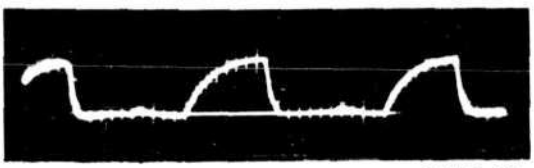
WAVEFORMS OF EXPERIMENTAL TIME-PULSE DISTRIBUTOR

A-30621



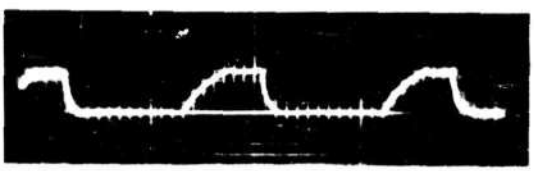
F-118-9

PLATE OF FLIP-FLOP COUPLED TO GATE TUBES IN FIRST SECTION



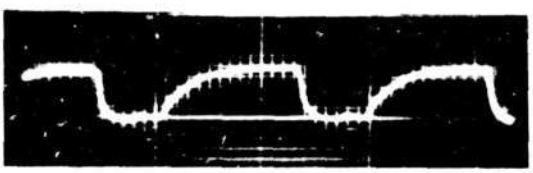
F-118-10

OPPOSITE PLATE OF FLIP-FLOP OF F-118-9



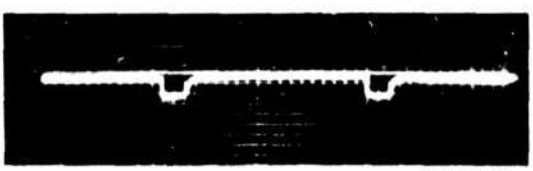
F-118-11

PLATE OF FLIP-FLOP COUPLED TO GATE TUBES IN SECOND SECTION



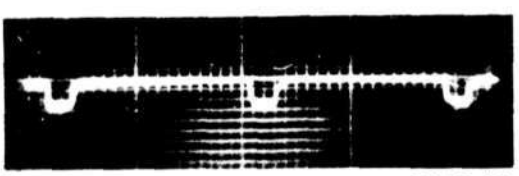
F-118-12

OPPOSITE PLATE OF FLIP-FLOP OF F-118-11



F-118-13

OUTPUT 1 WITH 1000 OHM RESISTOR IN PLACE OF TRANSFORMER LOAD



F-118-14

OUTPUT 2 WITH 1000 OHM RESISTOR IN PLACE OF TRANSFORMER LOAD

WAVEFORMS OF EXPERIMENTAL TIME-PULSE DISTRIBUTOR

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts.

SUBJECT: STEP COUNTER FOR 5-DIGIT MULTIPLIER

Written by: Edwin I. Blumenthal

Date: August 29, 1947

Foreword

This report contains (1) a functional analysis of the step counter and (2) a discussion of the design problems encountered and their ultimate solutions.

Introduction

Binary multiplication and division are processes involving, respectively, successive steps of addition and subtraction. The function of the step counter is to keep track of the number of these steps completed by the machine.

Multiplication in particular involves the performance of the following sequence of operations: examination of the right-most digit of the multiplier, addition of the multiplicand whenever this digit is a one, shifting of both multiplier and partial product to the right one digit, and continuation of these operations until every digit in the multiplier has been used.

The step counter provides the means of counting these operations and stopping the additions when the multiplication is complete. The counter is preset in accordance with the number of digits in the multiplier. Each shift-and-add operation indexes the counter one point. When the counter is full, an overflow (or end-carry) pulse is transmitted to the input, turning off the clock pulses and stopping the multiplication.

Discussion of Block Diagrams

B-37074-2 shows the block diagram of a step counter capable of handling 2^5, or 32, binary digits. When it is desired to read in to the counter, gate tubes GT01 receive control pulses from the bus through the operation of the control and storage switches. Pulses are delivered to these switches via the bus, through gate tubes GT02, whenever the read-out line is pulsed.

Provision is shown for reset pulses, which merely place all flip-flops in a pre-determined position, depending upon which operation, multiplication or division, is to be performed.

During multiplication of 32-digit numbers, pulses enter at the add-to-step-counter input and produce an end-carry output pulse for every 32 input pulses.

Brief Treatment of Modified Counter

The step counter shown in B-30851 and B-30884 has 3 flip-flop stages, since this is the minimum number necessary for a 5-digit multiplier.

For this application, the only inputs necessary are add-to step counter and clear step counter, referred to in the schematic as add-in and clear, respectively; however, provision has been made for the insertion of zeros in flip-flops 1 and 2, and one in flip-flop 3, through push button switches S1, S2, and S3.

(It is appropriate, at this time, to remind the reader that convention has established the interpretation of flip-flop position as follows: when the left-hand tube of the flip-flop is cut off, a zero is stored; when the left-hand tube is conducting, a one is stored.)

Since a-c coupling is used, 100-kc restorer pulses must be fed to each flip-flop in the intervals during which no pulses are present on the add-to-step counter line.

The only output is the end carry, which, for three flip-flop stages, occurs at 1/8 the pulse repetition frequency (prf) of the input pulses.

In the 5-digit multiplier for which this unit was designed, multiplication will take place at a rate of 2 megacycles or more, with tests to 4 megacycles. In the absence of pulses on the add-in line, d-c restoration at a 100-kc rate will be fed to the unit.

For test purposes, we may

1. Feed 2 mc pulses in continually, eliminating the need for paired restorer pulses.

2. Feed in only these paired restorer pulses, and check the unit by adding in single pulses, push-button controlled.

3. Substitute for the manual push button control of (2) a low-frequency pulse source, as is conveniently afforded by the output trigger of a P-5 synchroscope.

This latter scheme is particularly advantageous, since the circuit may then be checked at low frequencies on an ordinary cathode-ray oscilloscope.

Two neon lights are mounted beneath each flip-flop unit. The particular light that is on shows whether zero or one is stored in any one flip-flop.

The sequence of digits stored by the unit for pulses entering on the add-in line is shown below (assuming all flip-flops are initially at zero). Successive pulses do actually add to whatever is stored in the counter.

	FF.No.1.	FF.No.2.	FF.No.3.	Reading
Initial position	0	0	0	0
Pulse No. 1	1	0	0	1
Pulse No. 2	0	1	0	2
Pulse No. 3	1	1	0	3
Pulse No. 4	0	0	1	4
Pulse No. 5	1	0	1	5
Pulse No. 6	0	1	1	6
Pulse No. 7	1	1	1	7
Pulse No. 8	0	0	0	0

The "reading" tabulated is the decimal equivalent of the binary digits, when flip-flop positions are read from right to left. (For example 6 = 110).

It is necessary, in addition to the feature described above, that every eighth pulse, and in particular the pulse which sets all flip-flops to their zero position, pass through to the end-carry output line.

Reference to circuit diagram B-30851 and the waveforms of A-30859 will clarify the following discussion.

Operation of the circuit at 4 mc

Pulses of 1/20-microsecond duration appear at the add-to step-counter input line, at a prf of 4 mc. Assume all flip-flops read zero (left-hand tubes cut off), and consider, in turn, each of a train of these input pulses.

1. Pulse No. 1 finds gate tube V15 closed, since flip-flop No. 1 holds its suppressor below cut off. However, this pulse is delayed 0.05 μsec by DE1 and then triggers flip-flop No. 1 through trigger tube V14.

   Now, flip-flop No. 1 reads 1
   flip-flop No. 2 remains 0
   flip-flop No. 3 remains 0

2. The second pulse arrives after 1/4 μsec, passes on through gate tube V15 (which flip-flop No. 1 has opened), and is delayed by DE1 and DE2. Thus, 0.05 μsec. after the appearance of pulse No. 2, flip-flops 1 and 2 are triggered by their respective trigger tubes V14 and V16. However, this pulse is blocked by gate tube V17, which is still held shut by flip-flop No. 3.

   As a result, flip-flop No. 1 reads 0
   flip-flop No. 2 reads 1
   flip-flop No. 3 remains 0

3. The third pulse therefore finds gate tube V15 closed, and can do no more than trigger flip-flop No.1 after DE1 has delayed it by 0.05 μsec.

Now flip-flop No. 1 reads 1
flip-flop No. 2 remains 1
flip-flop No. 3 remains 0

4. Pulse No. 4 finds gate tubes V15 and V17 open, since both the first and second flip-flops read 1. Therefore, this pulse is simultaneously delayed by all three elements, and triggers all three flip-flops through V14 and V16.

Therefore flip-flop No. 1 reads 0
flip-flop No. 2 reads 0.
flip-flop No. 3 reads 1

5. The fifth pulse, since gate tube V15 is now held closed by flip-flop No. 1, is merely delayed by DE1, and switches flip-flop No. 1 through trigger tube V14.

Now flip-flop No. 1 reads 1
flip-flop No. 2 remains 0
flip-flop No. 3 remains 1

6. Pulse No. 6 finds gate tube V15 open at this time, since flip-flop No. 1 reads 1, but finds gate tube V17 closed, since flip-flop No.2 reads 0. It therefore switches flip-flop No. 1 and flip-flop No. 2 after delay in passing through DE1 and DE2.

Therefore flip-flop No. 1 reads 0
flip-flop No. 2 reads 1
flip-flop No. 3 remains 1

7. Pulse No. 7 is blocked by gate tube V15 since flip-flop No. 1 reads 0, and is merely delayed by DE1 and triggers flip-flop No. 1, through buffer V14.

Now flip-flop No. 1 reads 1
flip-flop No. 2 remains 1
flip-flop No. 3 remains 1

8. Pulse No. 8 now finds both gate tubes V15 and V17 open, and so, after delay by DE1, 2 and 3, simultaneously switches all three flip-flops, inserting 0 in each of them and completing a cycle of operation.

Now flip-flop No. 1 reads 0
flip-flop No. 2 reads 0
flip-flop No. 3 reads 0

A-30859 presents a graphical demonstration of one of these cycles, and simplifies the explanation of how the appropriate end-carry pulse is produced.

The 3-tube mixer, V10, 11, and 12, with inputs from each of the three flip-flops, produces the plate waveform of A-30859. Therefore, the end-carry gate tube, V13, will be open only when all three tubes are cut off.

This condition is fulfilled when each flip-flop reads 1, holding both V15 and V17 open. Therefore pulse No. 8, of the cycle described above, in addition to setting all flip-flops back to zero passes through the open end-carry gate tube.

Development of 3-stage Step Counter

1. Mixer for Restorer Input.

Drawing B-30852 shows the circuit originally used to mix 100-kc restorer pulses and pulses entering via the add-to step-counter line through the delay lines shown. The necessity for a more or less elaborate mixing scheme is due to (1) the danger of restorer pulses passing through CR17, 23, and 26 feeding into the delay lines, and (2) the danger of pulses from the add-in line passing through the delay lines and traversing a short-circuit path to the succeeding flip-flop trigger tube.

The presence of CR17, 23, and 26 discourages the latter phenomenon, while CR18, 24, and 29 prevent the former.

The difficulty experienced with the circuit as shown was solely one of distortion. The trailing edges of the pulses from the delay lines were considerably broadened before reaching the grids of the trigger tubes, so that erratic flip-flop operation resulted. To discharge shunt capacity more rapidly at the negative ends of CR18, 24, and 29, therefore, the 10,000-ohm resistors at these points were reduced to 1000 ohms. B-30851 illustrates this change, and also the addition of crystals 16, 22, and 27 to maintain a clamp at ground.

2. Gate tube Operation.

A-30857 illustrates the design initially proposed and ultimately modified for the operation of gate tubes V15 and V17 and the end-carry gate tube V13. Drawing No. A-30197 of Report No. R-109 shows that with 100 volts applied to plate and screen of a 6AS6 approximately + 15 volts must be applied to the suppressor before the plate current characteristic levels off. To take advantage of this invariance of plate current, the suppressors of gate tubes V15 and V17 were returned to - 15 volts, since the flip-flops were known to have a plate swing of approximately 30 volts (reference B).

However, it was later realized that driving the suppressors to this positive voltage was undesirable, when the suppressor triggers were supplied by flip-flops. During conduction, the suppressor would draw current and shunt a small (about 5000 ohm) resistance across the 1 megohm bias resistor, discharging the 100-$\mu\mu$f coupling condenser and feeding a reflected trigger pulse back to the flip-flop. Therefore the biasing method was modified, as a compromise, so as to drive the suppressor only to ground.

Worthy of note is the fact that this change permitted the use of a single 100$\mu\mu$f coupling condenser from the flip-flop plates to a common crystal clamp to ground, thus eliminating much of the troublesome loading on the flip-flop (cf. B-30851)

The control grid in A-30853 is shown biased to -10 volts through 220,000 ohms, while CR2, 4, and 6 maintain a clamp at ground. (The design of this portion of the circuit was complicated by the presence of the delay elements, 9½ inches of RG-65/U with a characteristic impedance of 1000 ohms.) Difficulties experienced here were the reflections produced along the delay lines, and the fact that at 4 mc a negative bias of the order of 40 volts was produced at the gate-tube grids. (The magnitude of this bias was dependent upon the frequency of the input pulses.)

The next attempt involved the insertion of the resistor network shown in A-30854. This circuit eliminated the undesirable accumulation of bias, and improved the termination of the input ends of the delay lines, yet proved unsatisfactory for reasons discussed below.

Much difficulty was experienced because of the sensitivity of the flip-flops. They frequently were triggered by spurious signals which were barely perceptible on the scope. The last flip-flop, in particular, received such small triggers from the second gate tube V17 that the signal-to-noise ratio was too low for dependable operation.

Furthermore, in this last biasing circuit, it was decided that insufficient protection was given V15 and V13 from being overdriven by clock pulses.

Finally, the second gate tube, V17, was biased too heavily to justify expectations of dependable operation from flip-flop No. 8. As a result, another modification was made which resulted in the final circuit of Drawing B-30851. The important points to be noted are:

1) The bias supply for V15 and V13 has been increased to -15 volts, and CR20 has been added to provide clamping at ground.

2) The second gate tube, V17, has been biased to -10 volts, and advantage taken of the fact that the duty factor at 4 mc for this tube is 1/20, so that screen and plate supply voltage for the tube is now 250 volts.

3. End-Carry Circuit

Drawing A-30855 shows the circuit originally intended to operate the end-carry gate tube. The coincidence of zeros in flip-flop No. 1 and flip-flop No. 2 opens gate tube V1, and produces a gate pulse for V2. V2 gates V3, in turn, when flip-flop No. 3 also reads zero, so that an end-carry pulse may be produced. With this circuit difficulty was experienced in maintaining the amplitude of the output pulse of V2. As is evident from timing diagram A-30859, the suppressor of V3 must be held positive for 0.25 μsec to insure the passage of pulse No. 8.

Transformer T76 was designed as an experimental model in an attempt to judge the feasibility of this scheme. It was found that V1 produced a proper gate for V2, yet the output of V2 was too small to be utilized as a gate for V3.

In contrast with the duty factors of gate tubes V15, V17 and V23 of B-30851 (1/10, 1/20, 1/40 for 1/20- μsec pulses at a 4-mc rate), the duty factors of gate tubes V1 and V2 in drawing A-30855 are unfavorable. As a result, the plate and screen voltages that could be applied to these tubes were limited to the point where the output of V2 was of insufficient magnitude. Another reason for rejection of this scheme was the fact that operation would tend to be marginal during periods of push-button operation. During such times, transformers T76 would be required to pass pulses up to 10 μsec long. When tested, these transformers produced a pulse whose amplitude after 10 μseconds was approximately 65 percent of that at its leading edge.

As a result, 6AG7's were employed in B-30851 (V10, V11, and V12). When any one flip-flop reads zero, one of these three tubes conducts, and lowers the potential at the common plate connection. In other words, only when all three flip-flops read one will the maximum voltage be coupled to the suppressor of the end-carry gate tube, V13. Therefore, the pulse that sets all flip-flops to read one also raises the potential of the suppressor of V13, so that the succeeding pulse not only switches all flip-flops to zero, but also is passed as an end-carry output pulse.

Test Methods

The waveforms of A-30859 were verified by the method shown in drawing A-30856.

For checking the operation of the unit under push button operation, the method of drawing A-30857 was employed. The disadvantage of this method is that the neon indicator lights of the step counter reveal only whether or not operation is correct, but give little assistance in locating troubles.

Drawing A-30858 shows the method employed to check the frequency of the end-carry output pulses. This test procedure revealed the passage of four end-carry output pulses per cycle of eight input pulses, rather than the desired passage of a single pulse per cycle.

At this point, the waveforms of drawings B-30881 and B-30882 were obtained by the test procedure of A-30858, but with a Browning OL-15A oscilloscope instead of the smaller Dumont 224-A.

From these waveforms, it is clear that an end-carry pulse may be expected for any digit involving two one's and a single zero; that is, for the third pulse

(1-1-0), for the fifth pulse (1-0-1), and for the sixth pulse (0-1-1). These outputs will be transmitted along with the desired seventh pulse (1-1-1) of the cycle.

This difficulty was unexpected, since it was prematurely concluded that a circuit sound in principle at high frequencies would be equally valid under application of d-c restoration. The example is important because it is representative of a problem that may well arise in the future.

This particular problem will be studied in preparation for Whirlwind I. However, the circuit diagram, B-30851, was modified as in E-30884 so that the end-carry gate tube operates in exactly the same manner as V15 and V17. In this form, the output pulse is produced in a serial manner, and is therefore delayed by a few hundredths of a microsecond from the time at which the output pulse of B-30851 is produced.

Written by Edwin L. Blumenthal

Approved by J. W. Forrester

References

A. Memorandum M-69, Digital Computer Block Diagrams

B. Engineering Notes E-48, Flip-flop Circuit

C. Report R-109, Gate Circuit

D. Engineering Notes E-47, AC Coupling and 6AS6 Operation

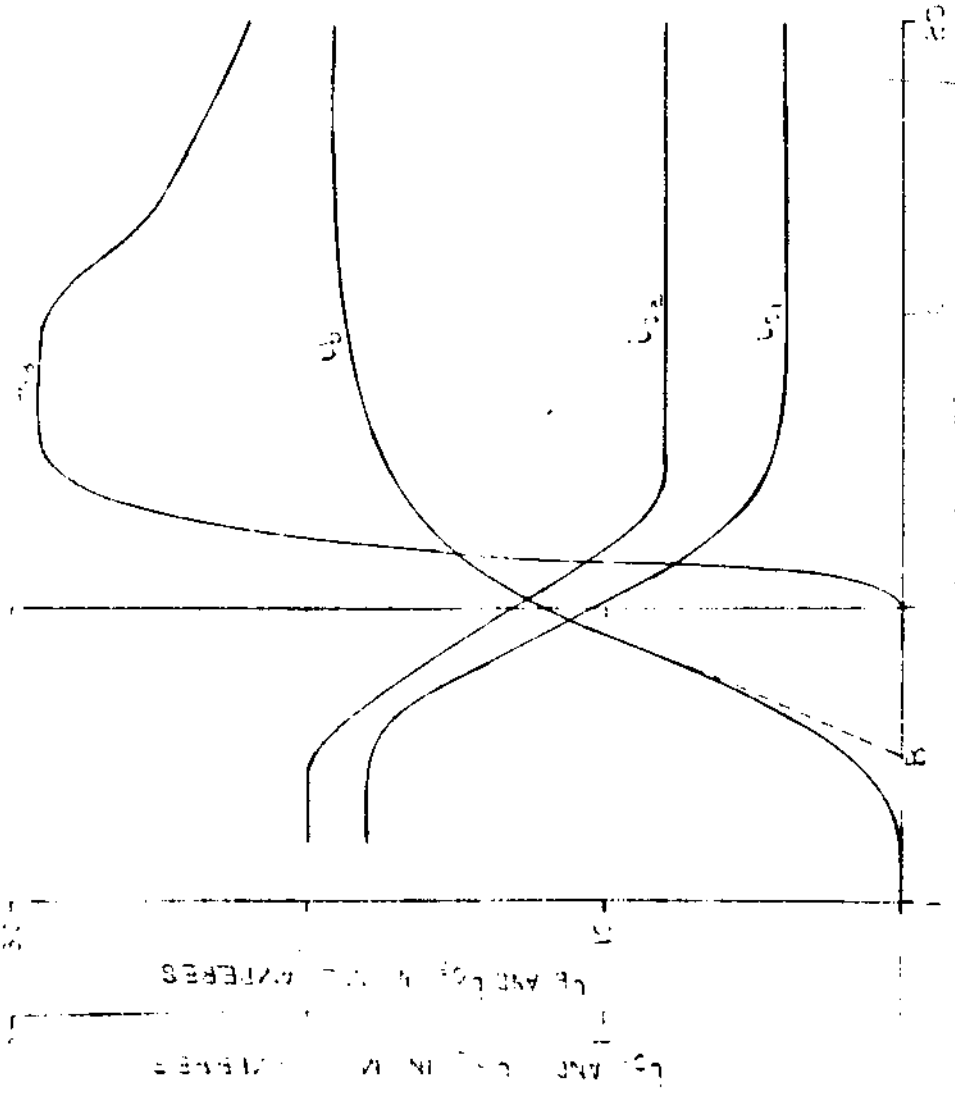
E. Report R-122, Pulse Transformers

F. Report R-127, Whirlwind I Complete Block Diagrams

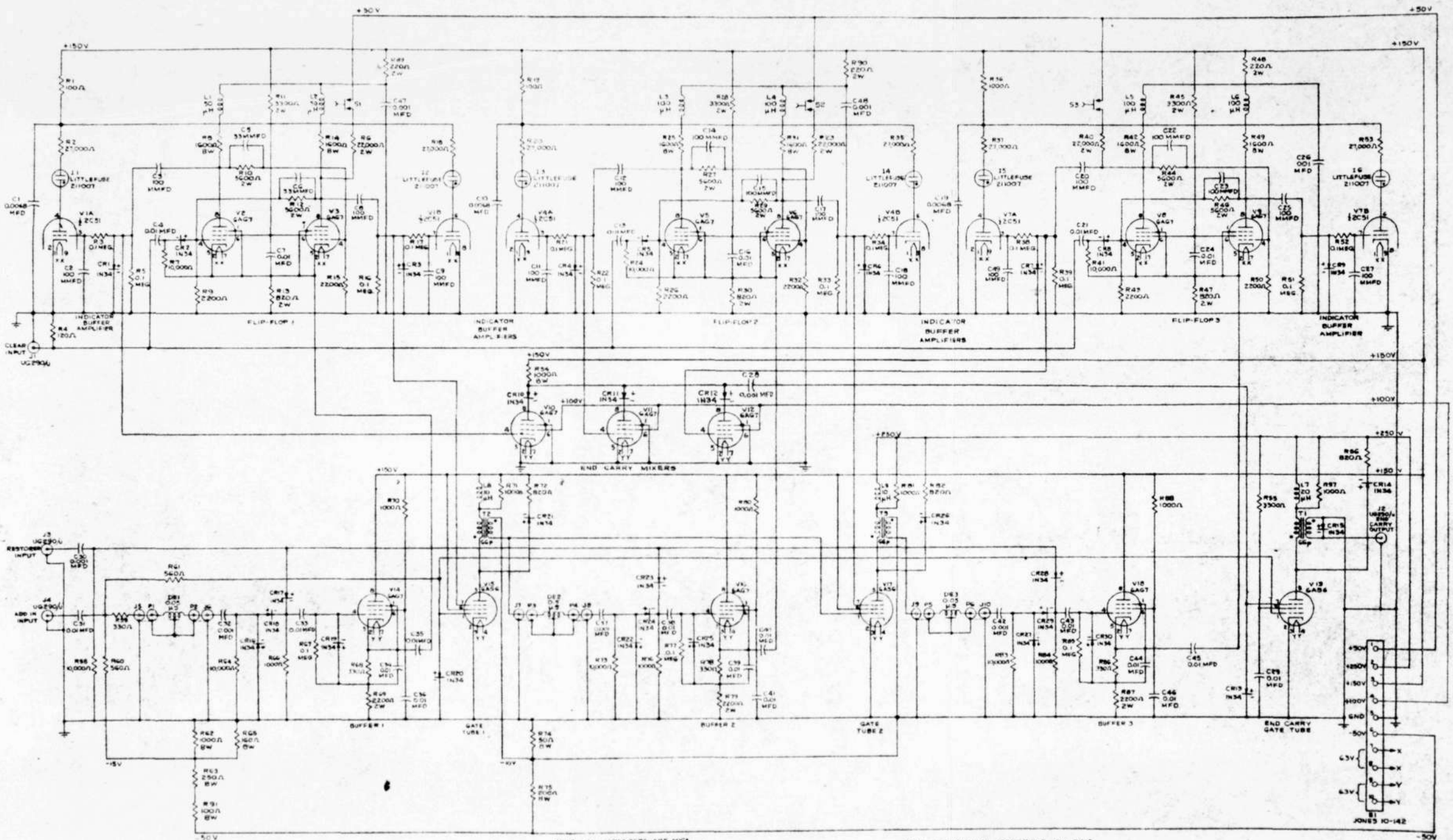
Drawings

A-30197	A-30857
B-30851	A-30858
B-30852	A-30859
A-30853	B-30881
A-30854	B-30882
A-30855	B-30883
A-30856	B-30884
	B-37074-2

EIB:CHC



B-30851



NOTE: ALL CAPACITORS ARE MICA.
ALL RESISTORS ARE 1 WATT ±10% UNLESS OTHERWISE SPECIFIED.
INTER-UNIT SHIELD PINS OF 2C51'S MUST BE GROUNDED.
DE1, DE2, AND DE3 ARE 9½ INCH LENGTHS OF RG65/U CABLE FOR STEP COUNTER SCHEMATIC WITH END CARRY MIXER TUBES (V10, V11, V12) ELIMINATED, SEE B-30884

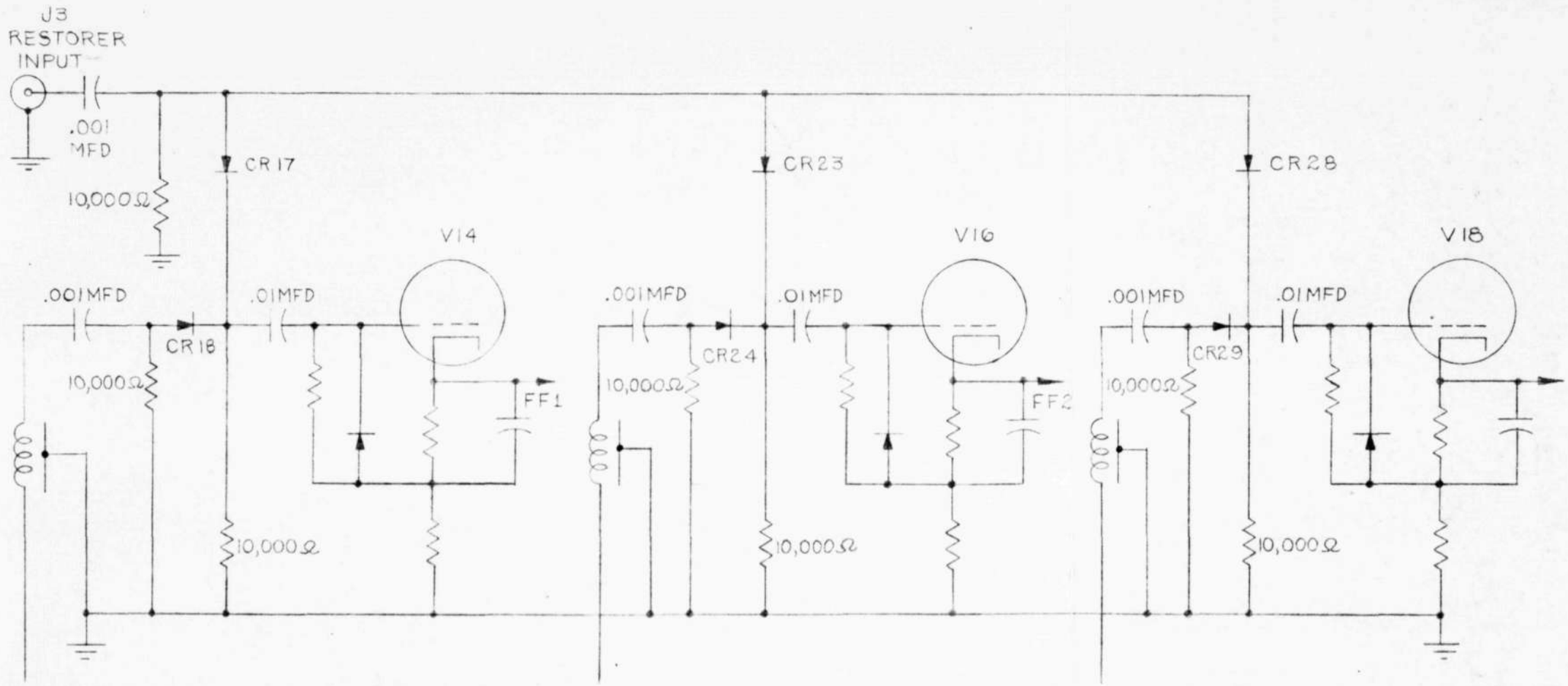
THE ELECTRICAL SYMBOLS ON THIS DRAWING ARE NOT DRAWN TO STANDARD SIZE AND MAY BE DRAWN THUS ONLY BY SPECIAL PERMISSION

STEP COUNTER CIRCUIT SCHEMATIC I

6345 F.B. 10/17/47

USED IN 6345 REPORT R-126

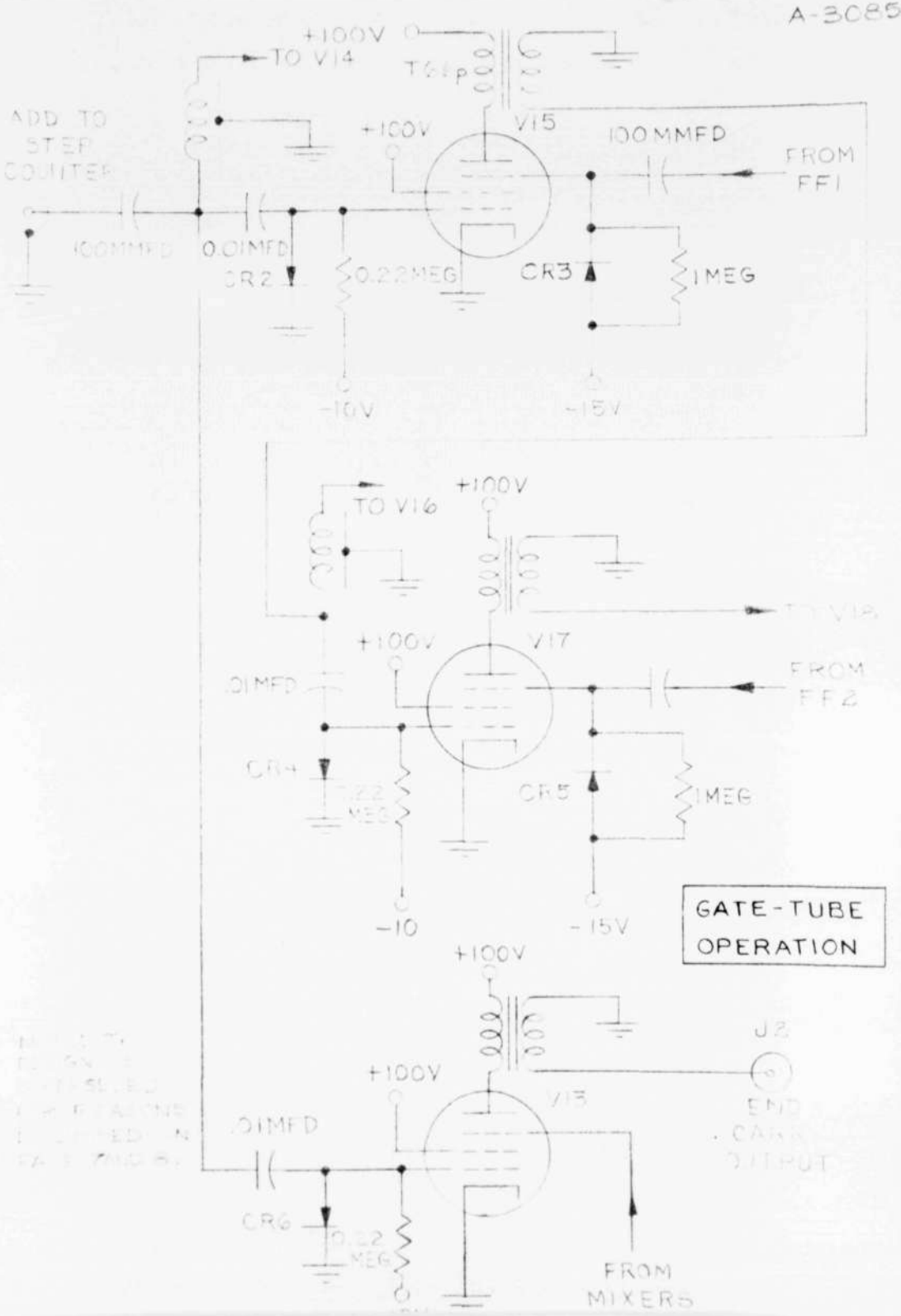
B-30852



RESTORER INPUT CIRCUIT

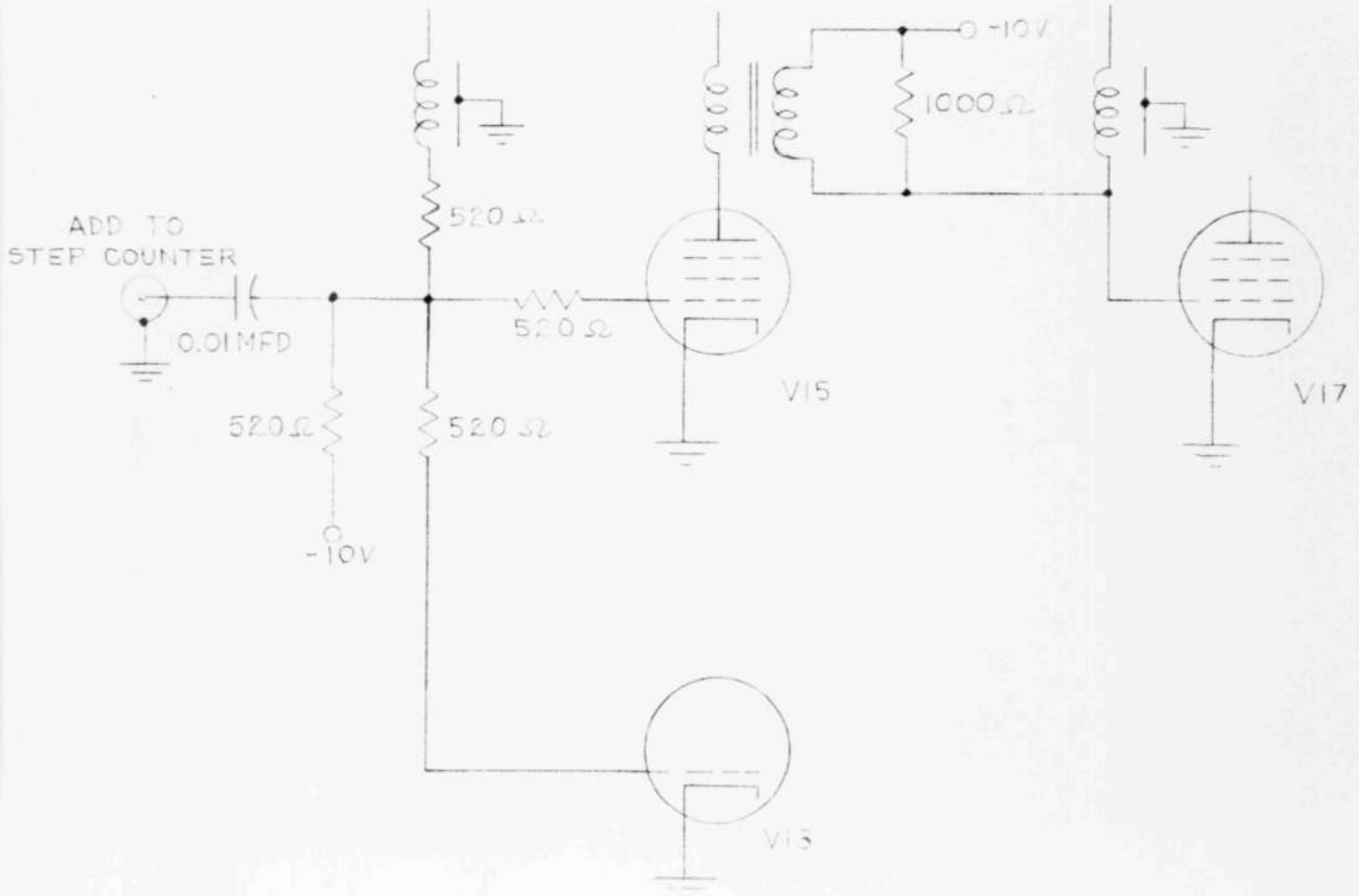
3-30852 USED IN G345 REPORT R-126

A-30853



-30853 - USED IN 6345 RUNOUT R-126

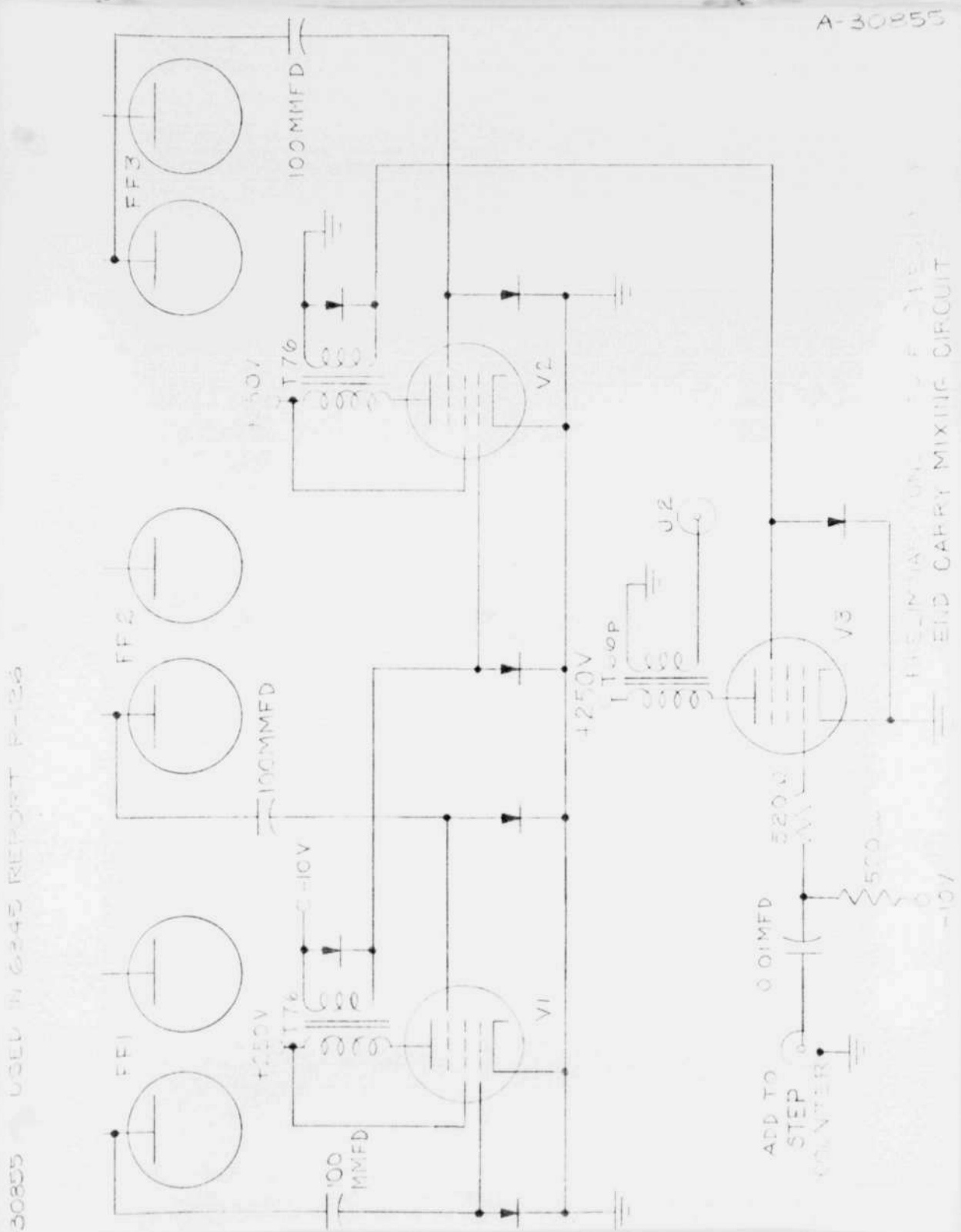
A-30854 USED IN 6345 REPORT R-126



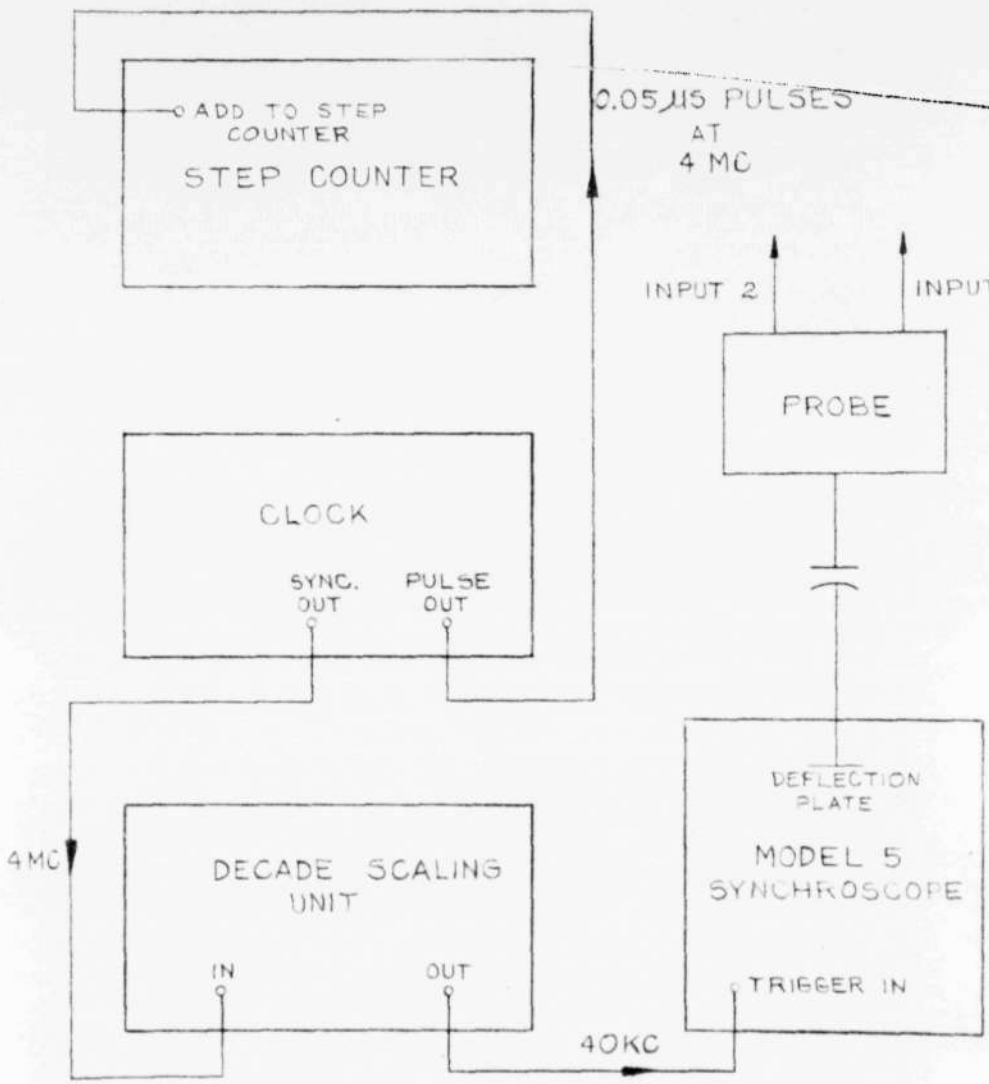
GATE-TUBE OPERATION

NOTE: THIS DESIGN IS GIVEN FOR READING DISCUSSION ON PAGES 8 AND 9

A-30854

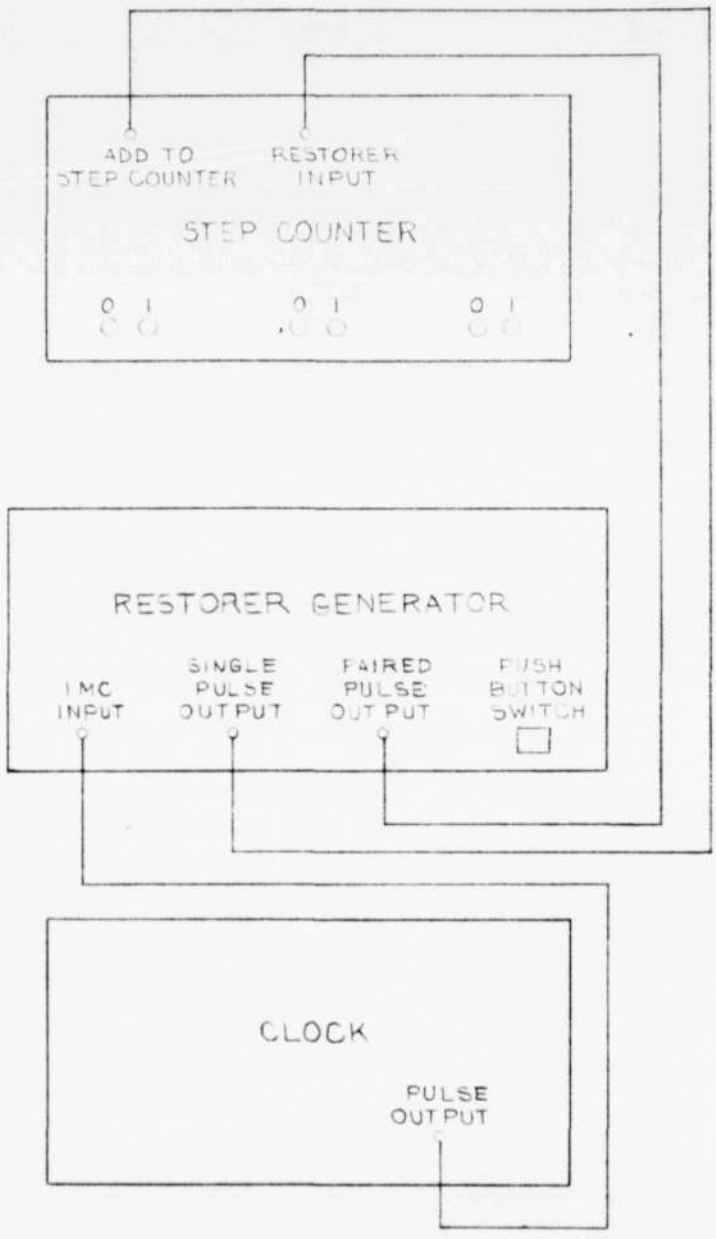


A-30856



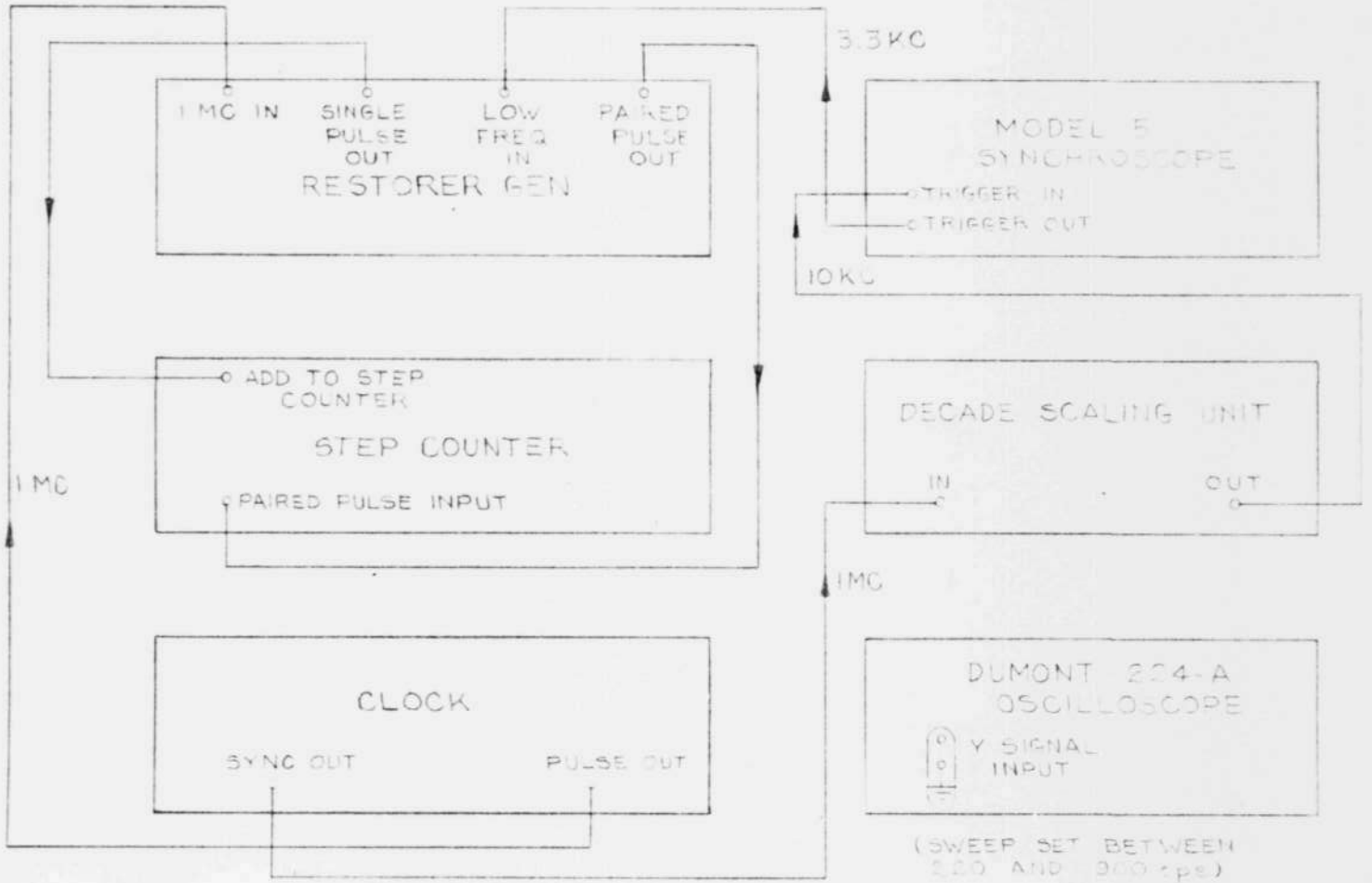
TESTING STEP COUNTER AT 4 Mc

A-30856 USED IN 6345 REPORT R-126



TESTING STEP COUNTER FOR PUSH-BUTTON OPERATION

A-30858 .USED IN 6345 REPORT R-126

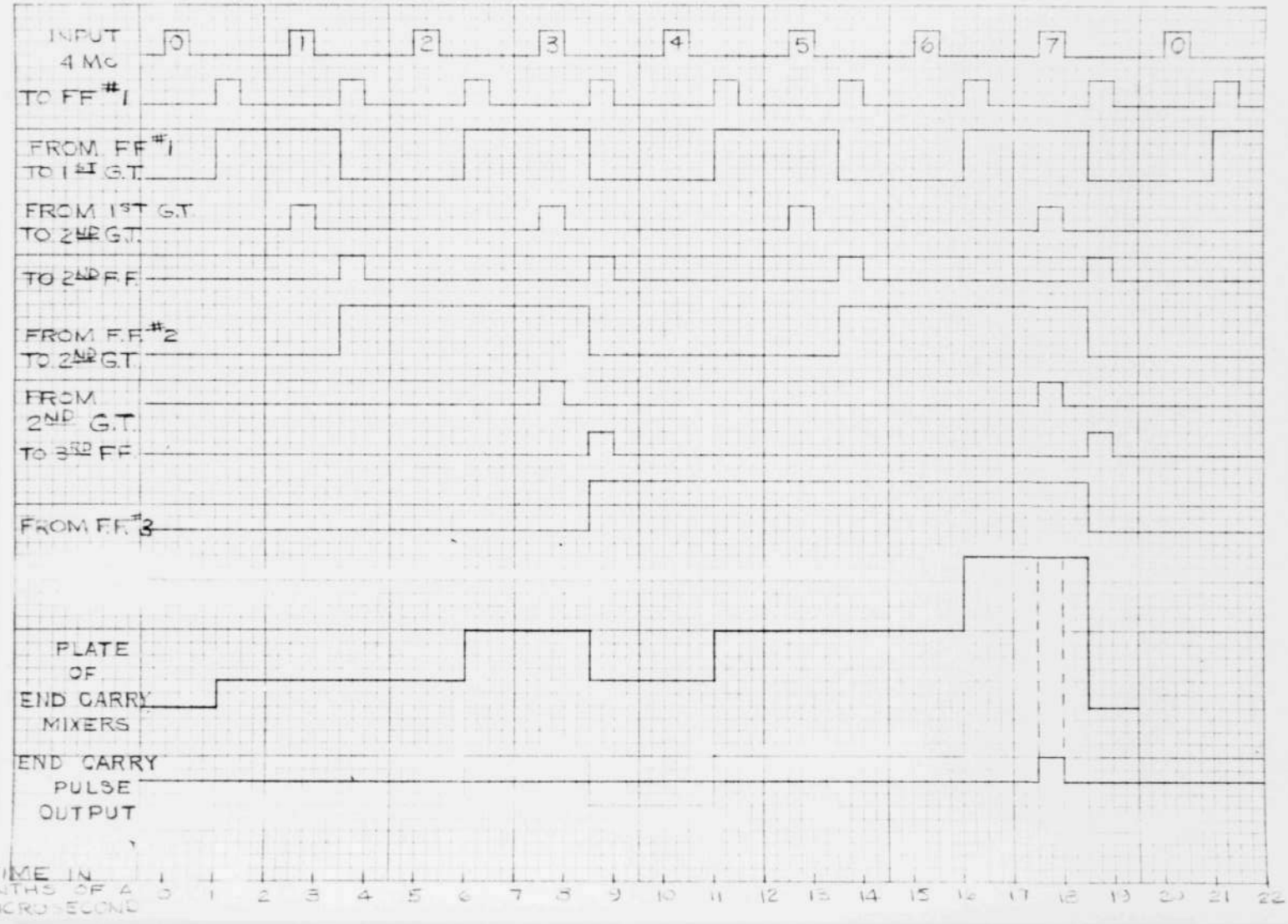


TESTING STEP COUNTER AT LOW FREQUENCY

A-30858

-30859

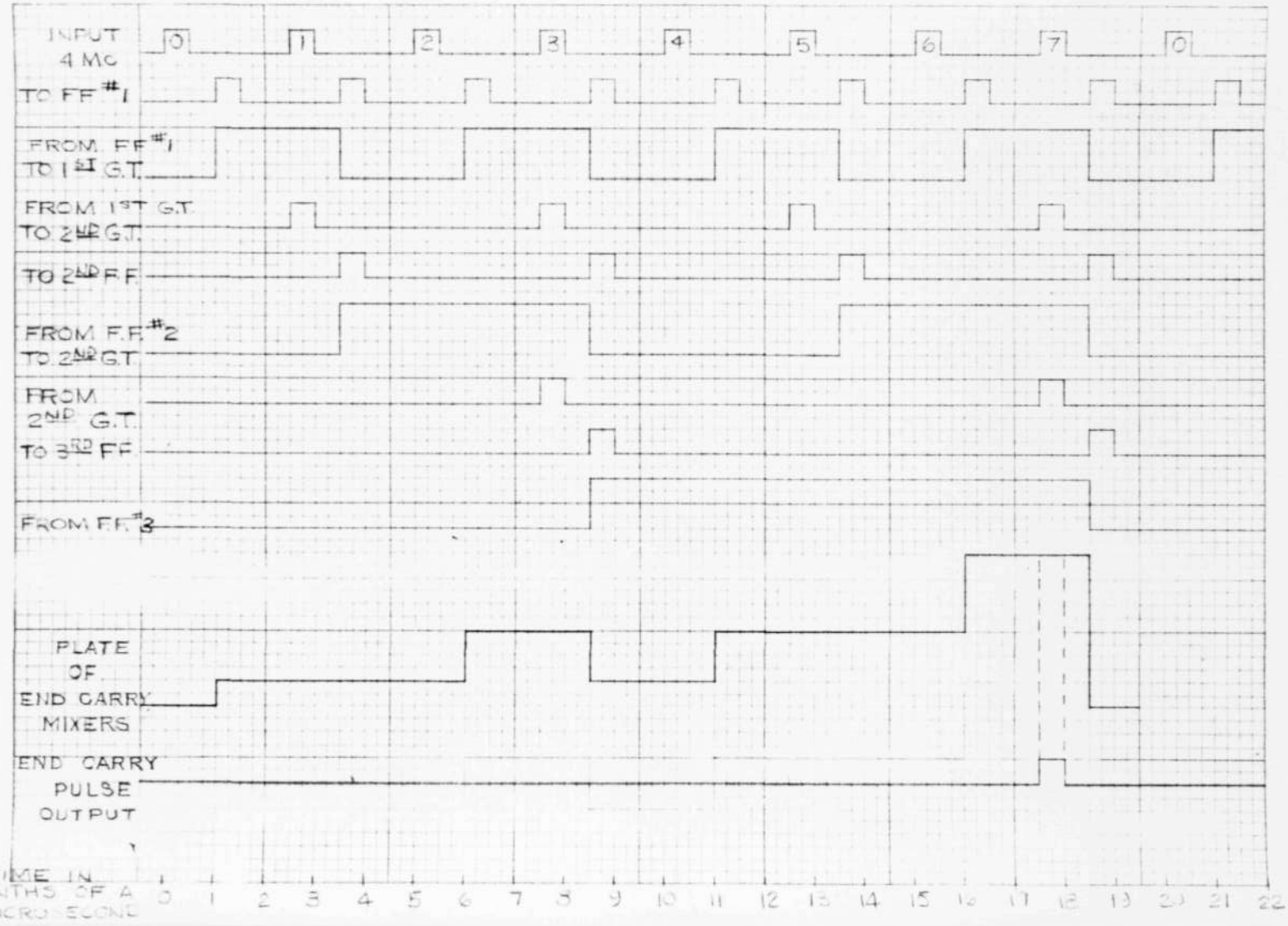
USED IN 6345 REPORT R-126



A-30859

-30859

USED IN 6345 REPORT R-126



A-30859

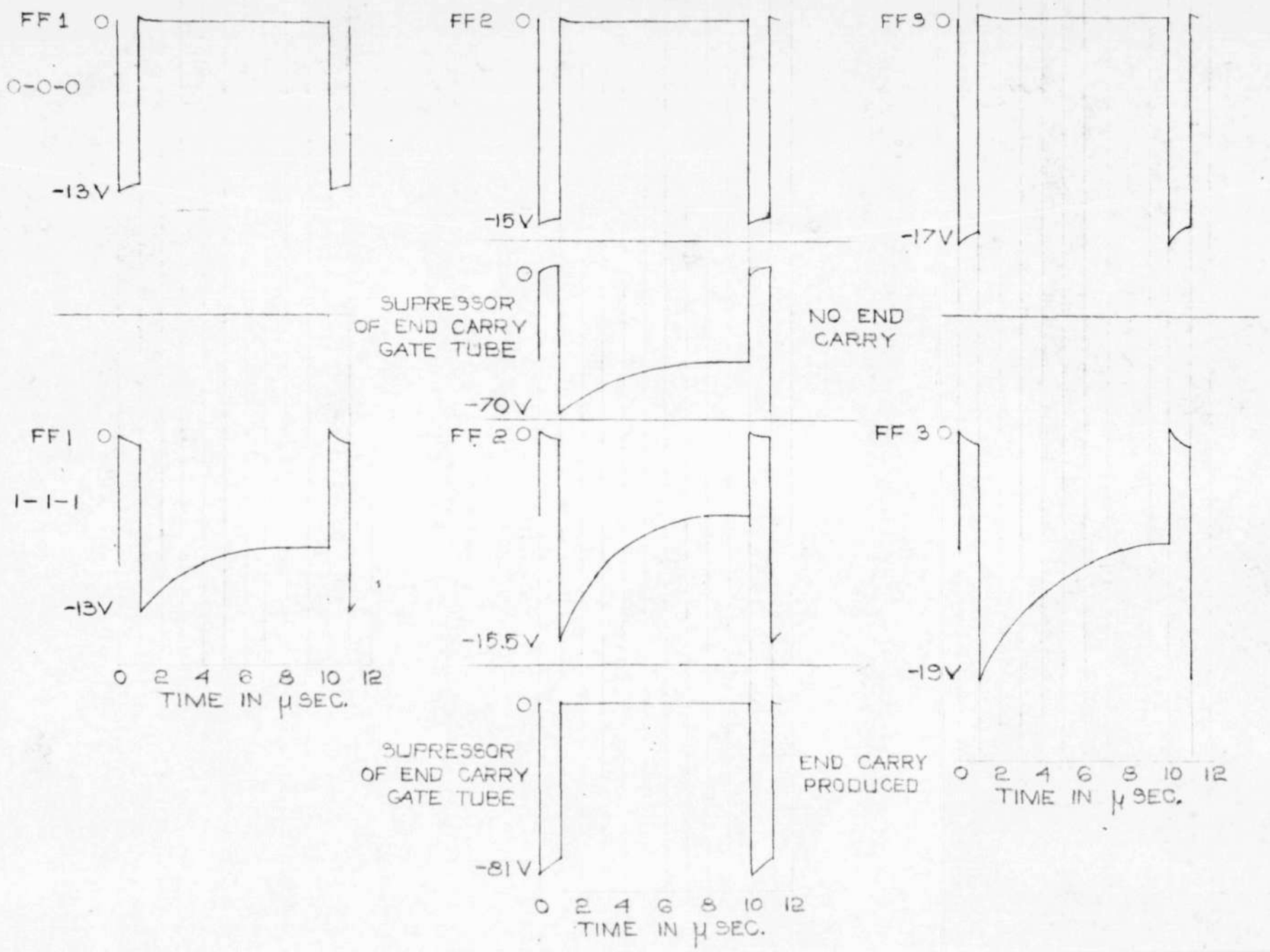
B-30881

B-30881

USED IN 6345 REPORT R-126

6345 RVW 9/15/47 B-30881 E.A.B.

WAVEFORMS OBSERVED
ON BROWNING (MODEL OL-15A)



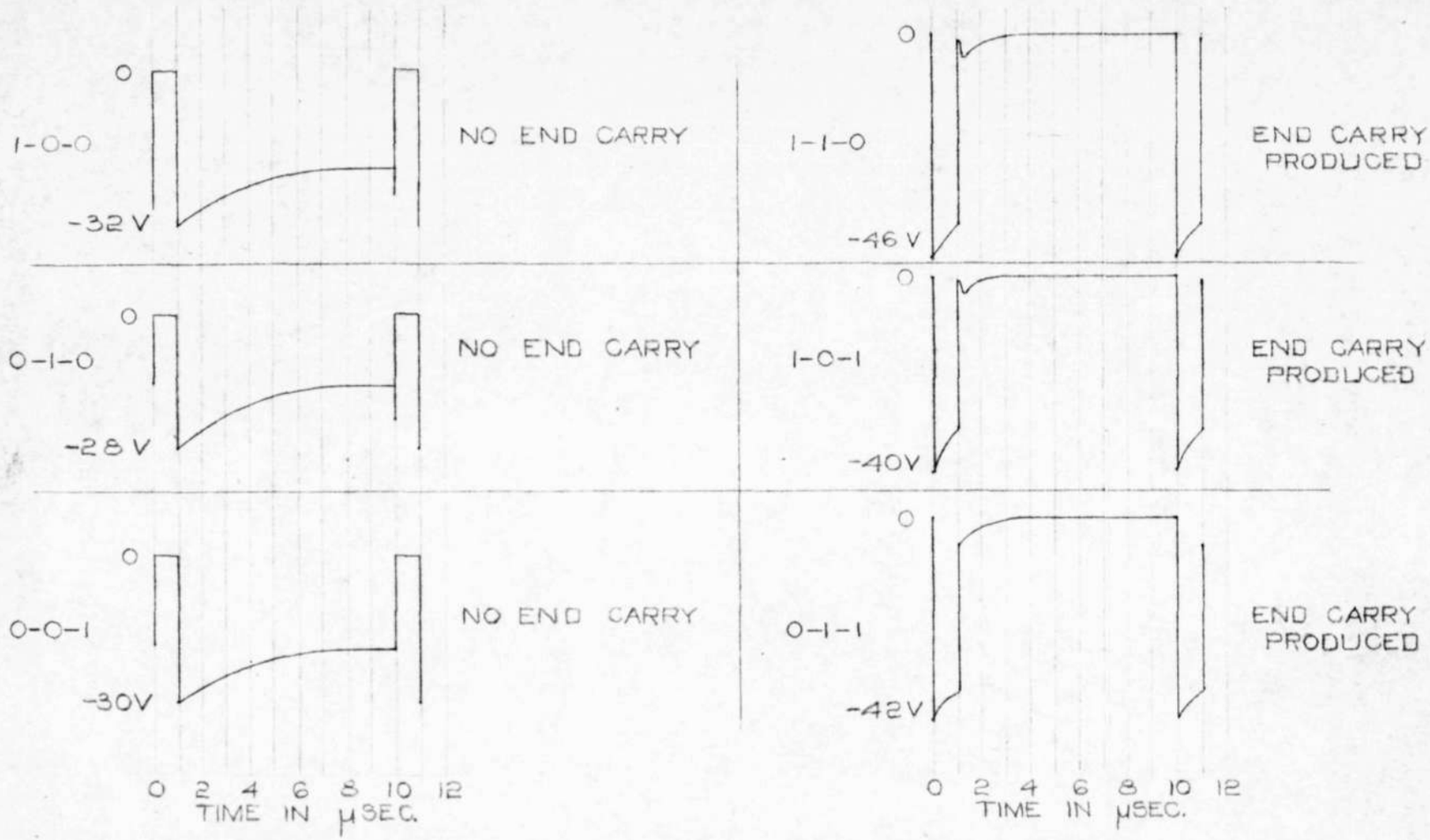
B-30882

B-30882

USED IN 6345 REPORT R-126

6345 RVW 9/15/47
B-30882
E. J. B.

SUPRESSOR WAVEFORMS
AS OBSERVED ON BROWNING (MODEL OL-15A)



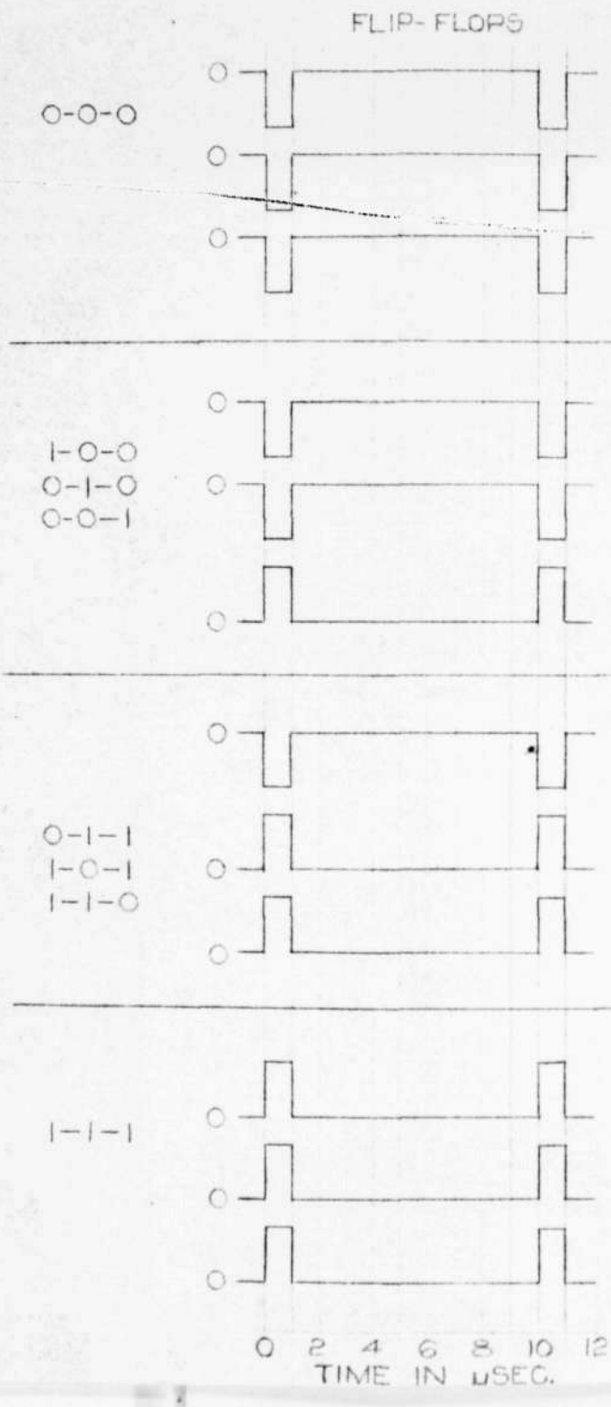
B-30883

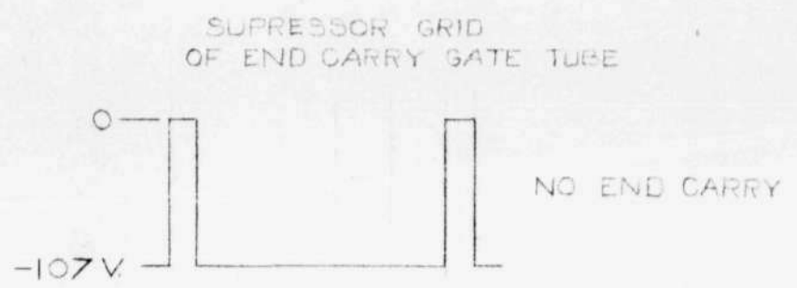
USED IN 6345 REPORT R-126

6345 RVW 9/15/47 B-30883 E.J.B.

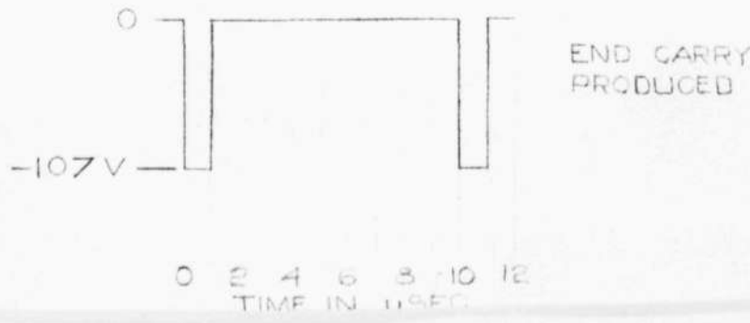
IDEALIZED WAVEFORMS

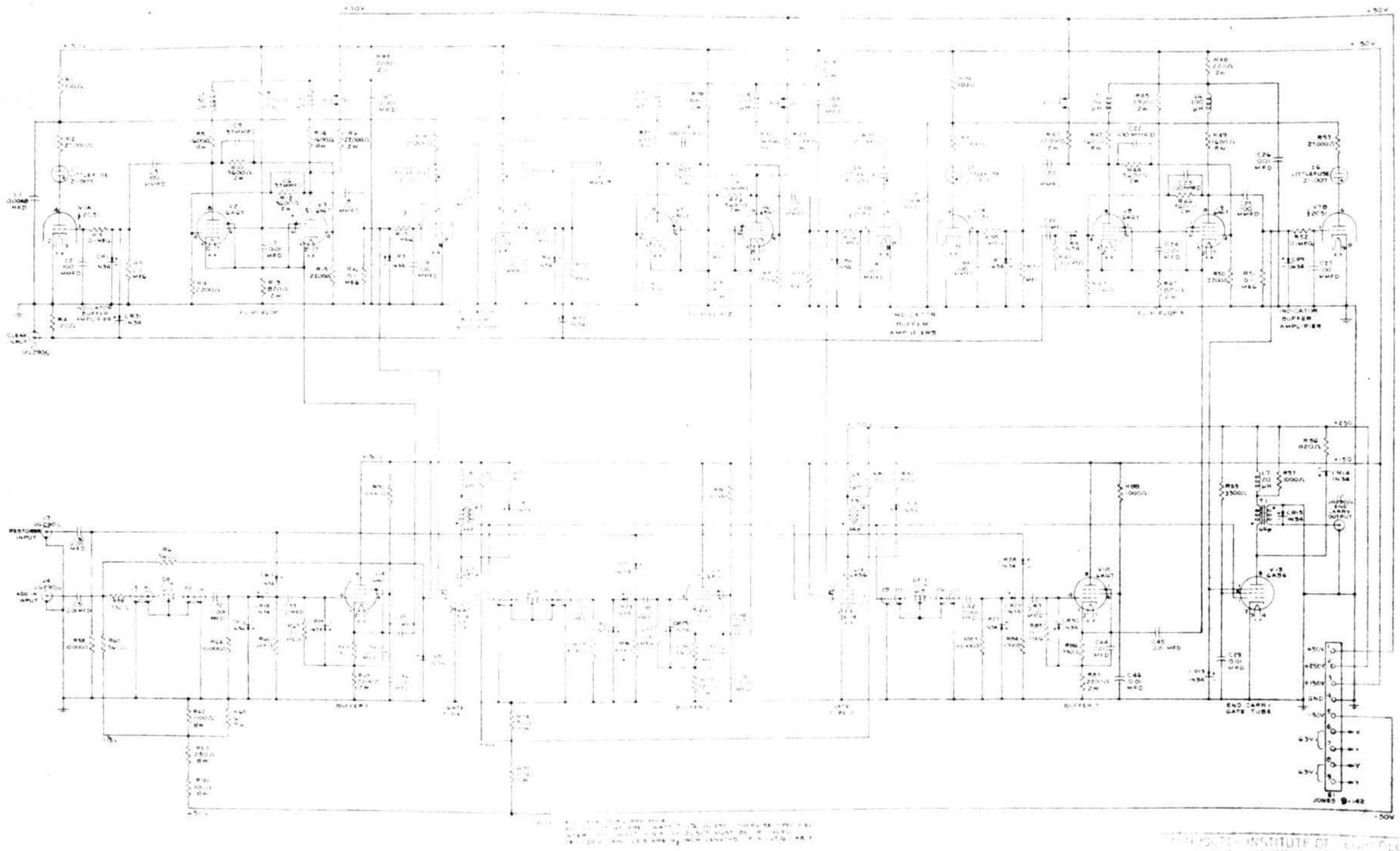
B-30883





NOTE:
VOLTAGES COMPUTED
FROM CHARACTERISTICS
OF 6AG7 (B-38176-G).



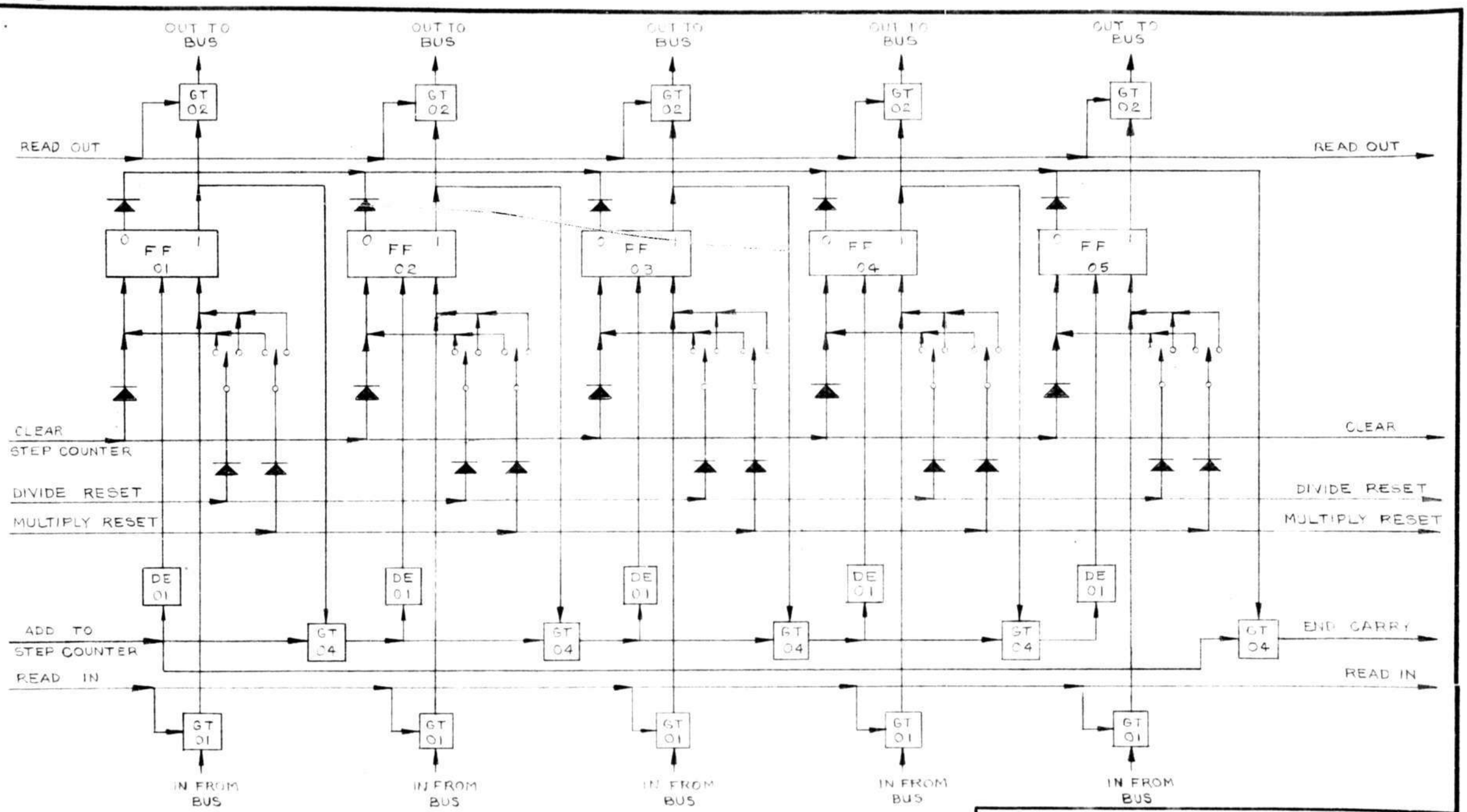


STEP COUNTER CIRCUIT SCHEMATIC II.

6345 F.B. 10/2/47
E.L.B E-30884-1

USED IN 6345 REPORT R-126

B-37074-2



SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

STEP COUNTER WWI 305

SCALE: | DR [illegible] | B-37074-2

ENG. [illegible] 6/5/47 | CK. | APP.

USED IN 6345 REPORT R-126

6345
Report No. R-121

SERVOMECHANISMS LABORATORY
Massachusetts Institute of Technology
Cambridge, Massachusetts

Date of Report: May 9, 1947 Page 1 of 5

Written by: George G. Hoberg Drawings:
A-30478
A-30479
A-30480
B-30481
A-30482
B-30483
A-30484
B-38187-G

Subject: Driver for Digit Transfer Bus

References:
1. Block Diagram Drawing B-37070
2. Report R-106, "Characteristics of Sylvania 1N34 Germanium-Crystal Diodes", Ray L. Ellis
3. 1GGH36-41
4. 1JAD37-56

Objectives:

An attempt is being made to devise a suitable means for applying a quarter-microsecond pulse to a low-impedance bus for transfer between units of the computer.

Assumptions:

Although the requirements are not yet definite, the following suppositions are believed to have considerable justification.

1. A digit transfer bus will consist of one hundred feet or less of coaxial line terminated at both ends in its characteristic impedance.

2. A number of "bus drivers" (for feeding the line) and output gate tubes will be connected to the bus at random intervals. (See Reference 1). Design methods assume six of each, but it seems possible that up to three or four times that number be used.

3. A quarter-microsecond pulse of ten to fifteen volts amplitude will be available as input to the driver, and a similar pulse of at least fifteen volts is desired as output.

4. Tubes and associated components are to be operated within one-half of manufacturers' ratings with dissipation averaged over the duty cycle. The duty factor for each driver will not exceed one-sixteenth.

Discussion of Work

The fact that the bus presents a very low load-impedance to the driver causes a good deal of difficulty. Each driver sees an impedance of only one-half the terminating impedance of the bus, which for the RG-62/U coaxial line used in the experiments is $\frac{93}{2} = 46.5$ ohms. This is reduced by the input capacities of the gate tubes whose grids are connected to the bus, and by the back-impedance of the inactive drivers present. While the former effect has been found relatively unimportant, the latter presents a sizeable problem.

A 46.5-ohm load demands a current flow of 322 milliamperes if a fifteen-volt pulse is to be realized. Currents of such magnitude might be supplied either by a step-down pulse transformer in the plate circuit of a pentode amplifier, or by a cathode follower.

The cathode follower is not, however, well adapted for use here. To prevent undue loading it would have to be kept completely cut off when not actually driving the bus, for when conducting it appears as an impedance of about 150 ohms. The high current requirement makes it necessary to drive even a large tube like an 807 well into the positive grid region, so for the 807 a grid swing of about fifty volts would be required. At least one additional amplifier stage would then be needed to drive the cathode follower, and, since the latter requires a positive pulse, an inverter transformer would have to be used for interstage coupling. Such disadvantages led to complete abandonment of the cathode follower in favor of pulse transformer methods.

The circuit shown in Drawing A-30478 was built up, using T.F. Wimett's pulse transformer T52D4 in the plate circuit of a 6AG7. With 100 feet of 93-ohm line tapped at intervals as shown in Drawing B-30481, the oscillograms of Drawing A-30482 were obtained. The apparently poor low-frequency response and the variations in waveform on the loaded line are inherent in this method, and therefore warrant discussion at some length.

In obtaining the oscillograms referred to, the loading effect of the inactive drivers was simulated by transformers with high-side windings floating. This was justified because the diodes on either side of the primary of each driver transformer (Drawing No. A-30478) effectively isolate that winding from ground and prevent reflection of the plate capacity of the 6AG7 back to the bus. The loading is then entirely dependent upon the design of the transformer which must, however be such as to permit only limited control of the loading.

As analyzed by Wimett, the equivalent load presented by each transformer is shown in Drawing No. A-30480. If the magnetizing inductance is sufficiently large, it can be assumed to draw no current during the pulse. Then the load on the driver is half the characteristic impedance of the line in parallel with an L-C branch; this causes the addition of a damped sinusoidal wave to the pulse. The phase of the distorting wave varies with respect to the leading edge of the pulse from point to point along the bus in a manner which can be predicted accurately for a single loading transformer. Multiple loading results in the addition of a number of these sinusoids which change in phase with respect to the pulse, and to each other, according to position along the line, producing overall results as shown in the oscillograms. The decrease in amplitude which occurs during these pulses is due to the fact that the magnetizing inductance of the transformers cannot be made sufficiently large to prevent current drain if good driving characteristics are to be maintained.

Although fair pulses are attainable in this manner with six or seven drivers present, it does not seem probable that acceptable results will be obtained with many more than that number unless the transformers can be connected to the line through unidirectional diodes. This may appear to be a simple solution, but it is complicated by the need for operating available germanium-crystal diodes in parallel in order to stay within current ratings. Their volt-ampere curves vary to such an extent that, unless the diodes are selected for similarity of characteristics, one of them might take too large a portion of the current and possibly destroy itself. (See Drawing B-38187-B and Reference 2). Selenium rectifiers cannot be used because of their high shunt capacitance, and thermionic diodes capable of supplying the required current would produce too large a voltage drop.

Parallel operation of germanium diodes was at first deemed impractical, but the limitation of the duty factor to one-sixteenth led to its reconsideration. Sylvania 1N34's are rated (conservatively, it is believed) at 200 peak and 22.5 average milliamperes. If two of them can be closely matched at 200 milliamperes, an eighteen-volt pulse can be put on the line when they pass rated peak current and about one-half rated average current.

Results of an investigation of the current distribution near rated peak current show that if a total of 400 milliamperes is to be drawn through two of these diodes, the worst case to be expected would result in one of them passing 300, the other 100 milliamperes. The dispersion could be reduced by the addition of resistance in series of each diode; in the above case, it is reduced to 30% of its original value if forty-ohm resistors are used. (See Drawing No. B-38187-G and Reference 3. Here the abscissae of the volt-ampere curves of the diodes are added to those of a constant resistance, producing a marked reduction in the vertical spread of the resulting curves). This added resistance would, however, cause an

increase in the rise time of the pulse for a given amplitude, so if it is to be used a proper compromise must be achieved. Without the resistance, the Sylvania peak rating will be exceeded by no more than 50% without matching, and considerably less if only fair matching is obtained. Use of more than two in parallel would alleviate this situation, but would again introduce the problem of low back impedance where a large number of drivers must be connected to the bus.

The advantage gained by using diodes is apparent by comparison of the oscillograms in Drawing No. A-30482 with those in Drawing No. A-30484. With a driver circuit as shown in Drawing No. A-30479, the only loading is that of the gate tube capacities, which has been shown to be negligible. The pulse on the bus does not vary to such a great extent from point to point, nor is there undesirable ringing after it. Sufficient amplitude is easily obtained in spite of the fact that the diodes act as a resistance in series with the load. Moreover, because large magnetizing inductances are unnecessary, the transformers may be designed to permit shorter rise times.

In obtaining the distribution of the volt-ampere characteristics shown in Drawing No. B-38187-G, the diodes were subjected to one-microsecond pulses of current up to 500 milliamperes at a repetition frequency of 2000 cycles per second. About 25% of those operated in this region showed a marked decrease in back resistance. Further tests indicated that pulses in excess of 650 milliamperes result in immediate serious reduction of the back resistance of most diodes, although one out of ten successfully withstood pulses up to 900 milliamperes for a short time. Significantly, none of the diodes tested showed a negative-resistance characteristic at pulse currents up to one ampere.

The effect of continuous operation under expected conditions (quarter-microsecond pulses of current between 200 and 300 milliamperes at an average frequency of 250 kilocycles) is currently being ascertained in a life test at 230 milliamperes. The test circuit consists of a free-running biased multivibrator which triggers an R-L-C peaker whose output is clipped in the grid circuit of an 829 amplifier. Six diodes in series with a resistor are capacity-coupled to the plates of the 829, and the peak pulse current is measured by an oscilloscope in terms of the voltage across the resistor. The forward and back resistances of the diodes are checked at frequent intervals on the direct-current-operated Model 1 Crystal Tester. Although many diodes fail to give consistent readings on this tester at -1 and -50 volts, no better criterion of performance is available.

After subjection to the 230-milliampere pulses for two hours, no appreciable change in the resistance readings was noticed. After eighteen hours, two of the test diodes exhibited a rather large decrease in resistance at -50 volts; these two also showed a slow change

in resistance at +1 volt, which increased about 35% after 186 hours. (See Reference 4, p. 56). However, conclusions must be withheld until more data are available. Further results will be reported at a later date.

General Electric germanium diodes have ratings twice as high as Sylvania 1N34's, and if they can be proved capable of actually passing twice as much current, at comparable voltages, they should be a definite solution to the problem. However, none are immediately available for test.

Conclusions:

If a bus is to have only six or seven drivers connected to it, the circuit shown in Drawing No. A-30478 represents a potentially satisfactory driver.

If, however, the number of drivers is to be of the order of twenty-five, the transformers must feed the bus through diodes, as shown in Drawing No. A-30479. No experimental objection to the use of matched diode pairs for this purpose has yet been found, but some doubt exists as to whether they may be operated such as to meet the stringent computer requirements on ratings. Should use of available diodes be adjudged unsatisfactory, the alternative is to develop a better diode, if possible one with ratings sufficiently high to obviate the need for parallel operation. For this the following specifications are suggested peak current capacity, 500 milliamperes at less than 15 volts; average current capacity, 35 milliamperes, back resistance, greater than 25,000 ohms; shunt capacitance, less than 30 micromicrofarads.

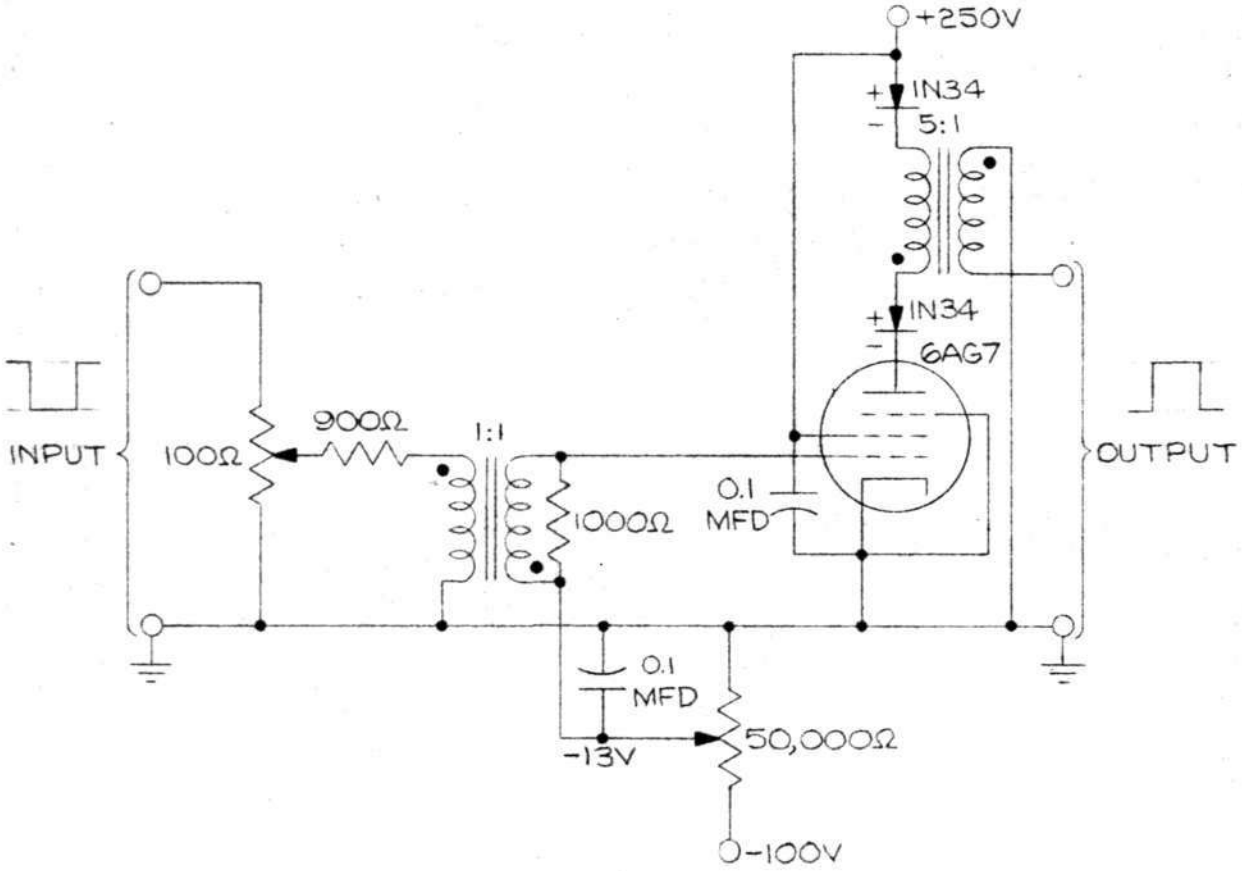
Further investigations of the applicability of germanium diodes to the problem of bus driving, and of means of improving transformer performance to obtain better pulse shape, are in progress.

Engineer: George H. Holberg

Approved:

GGH:bar:mb

A-30478



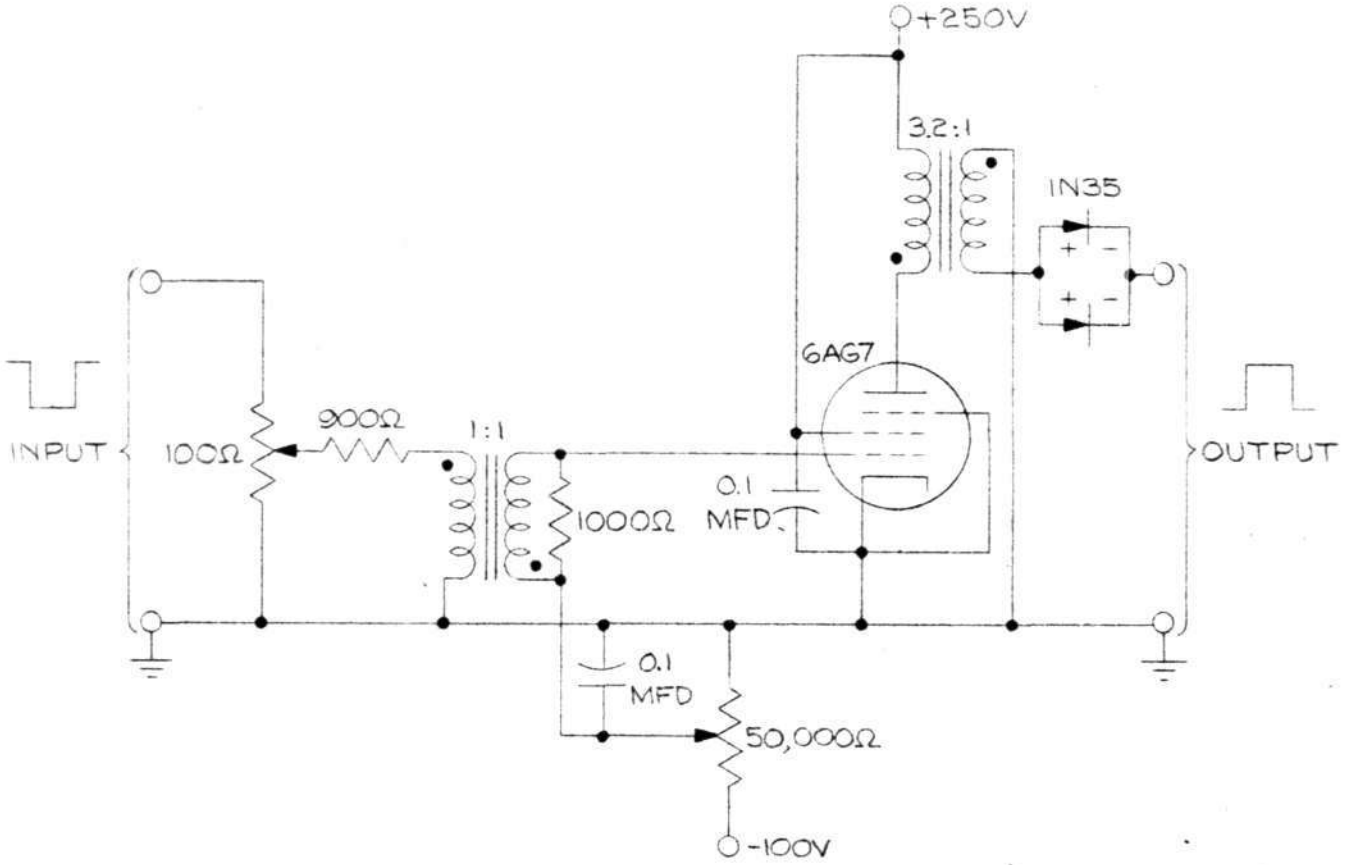
BUS-DRIVER CIRCUIT WITH DIRECT-COUPLED TRANSFORMER OUTPUT

(1:1 INVERTER TRANSFORMER IS OMITTED IF INPUT PULSE IS POSITIVE.)

6345 TL 4/22/47
A-30478

USED IN 6345 REPORT R-121

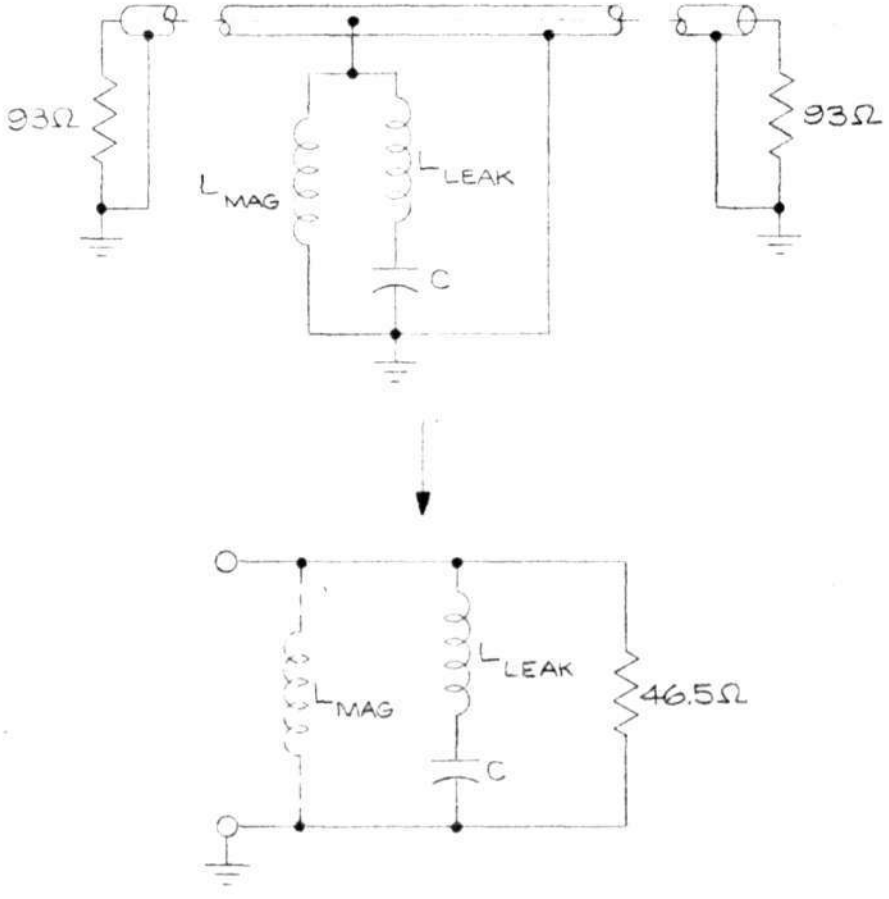
A-30479



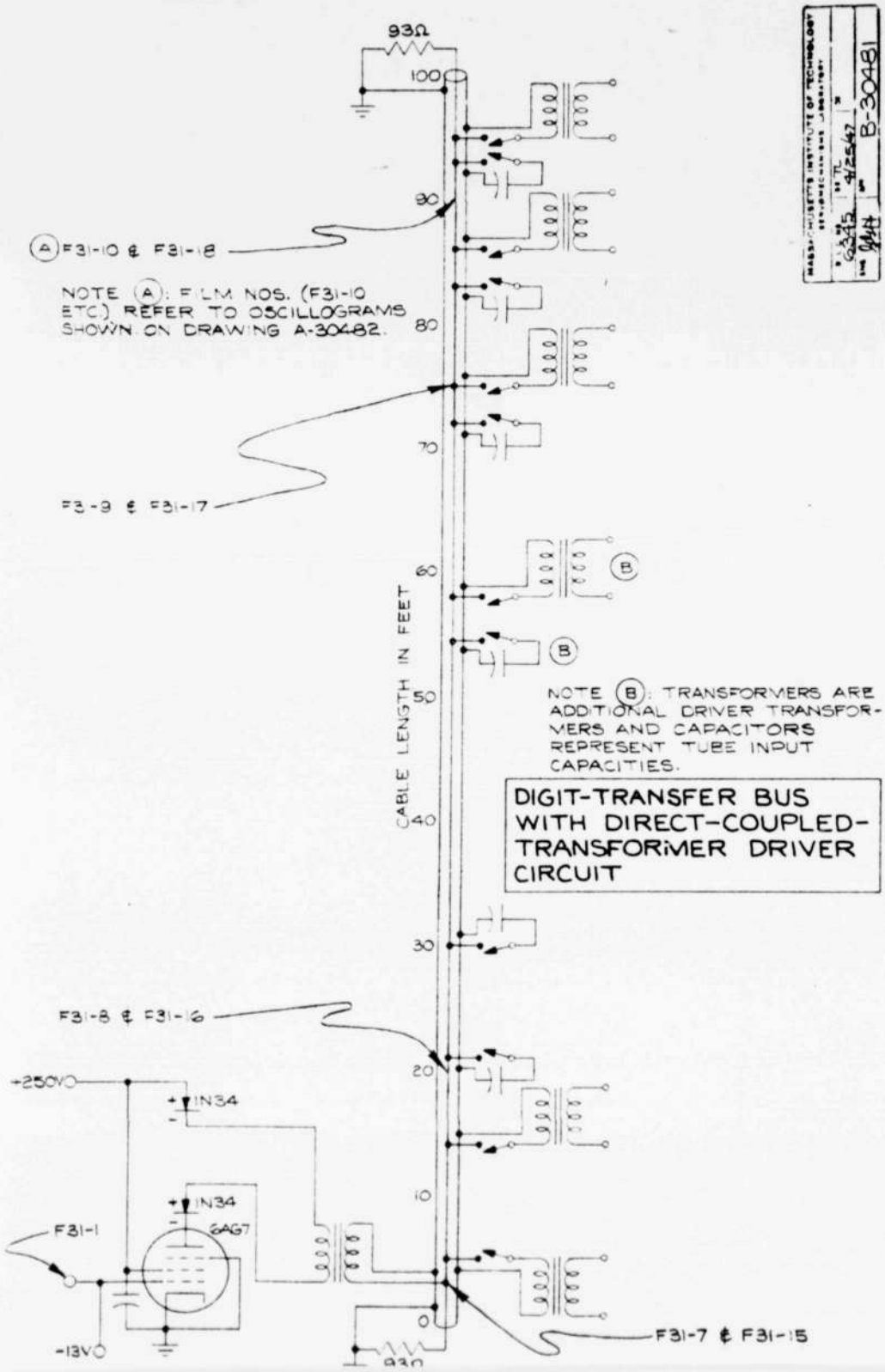
BUS-DRIVER CIRCUIT WITH DIODE-COUPLED TRANSFORMER OUTPUT

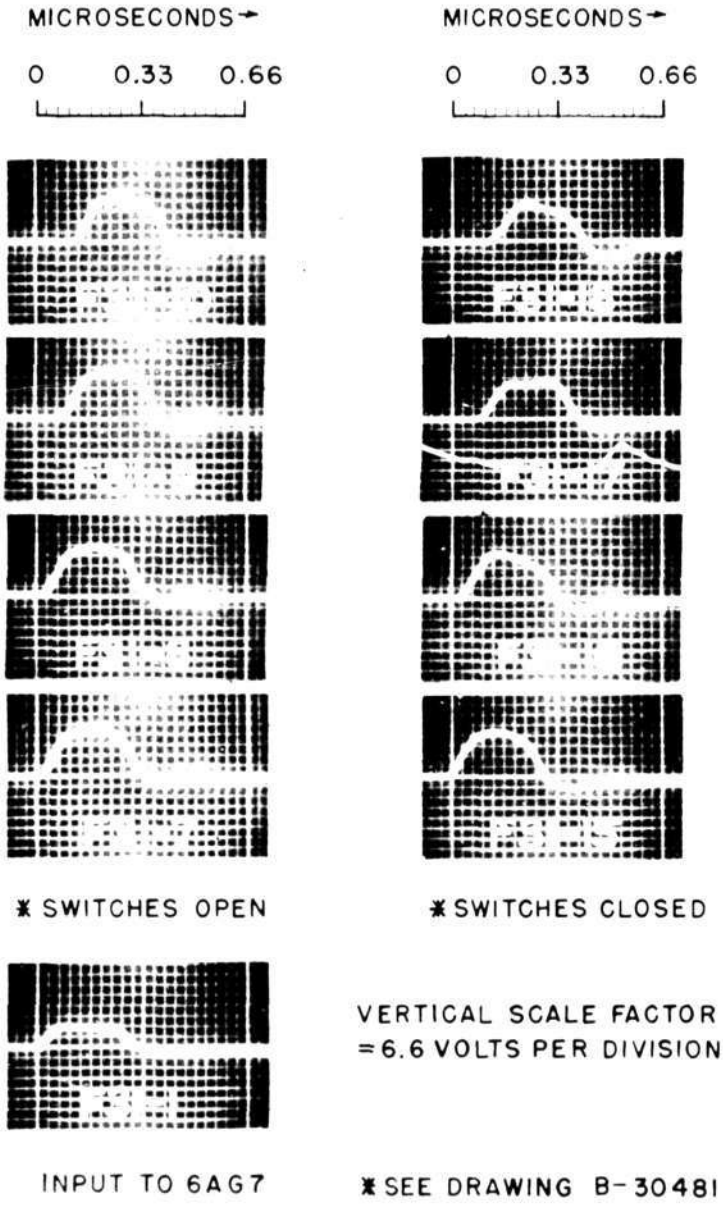
(1:1 INVERTER TRANSFORMER IS OMITTED IF INPUT PULSE IS POSITIVE.)

6345 TL 4/22/47
MH A-30479
USED IN 6345 REPORT R-121



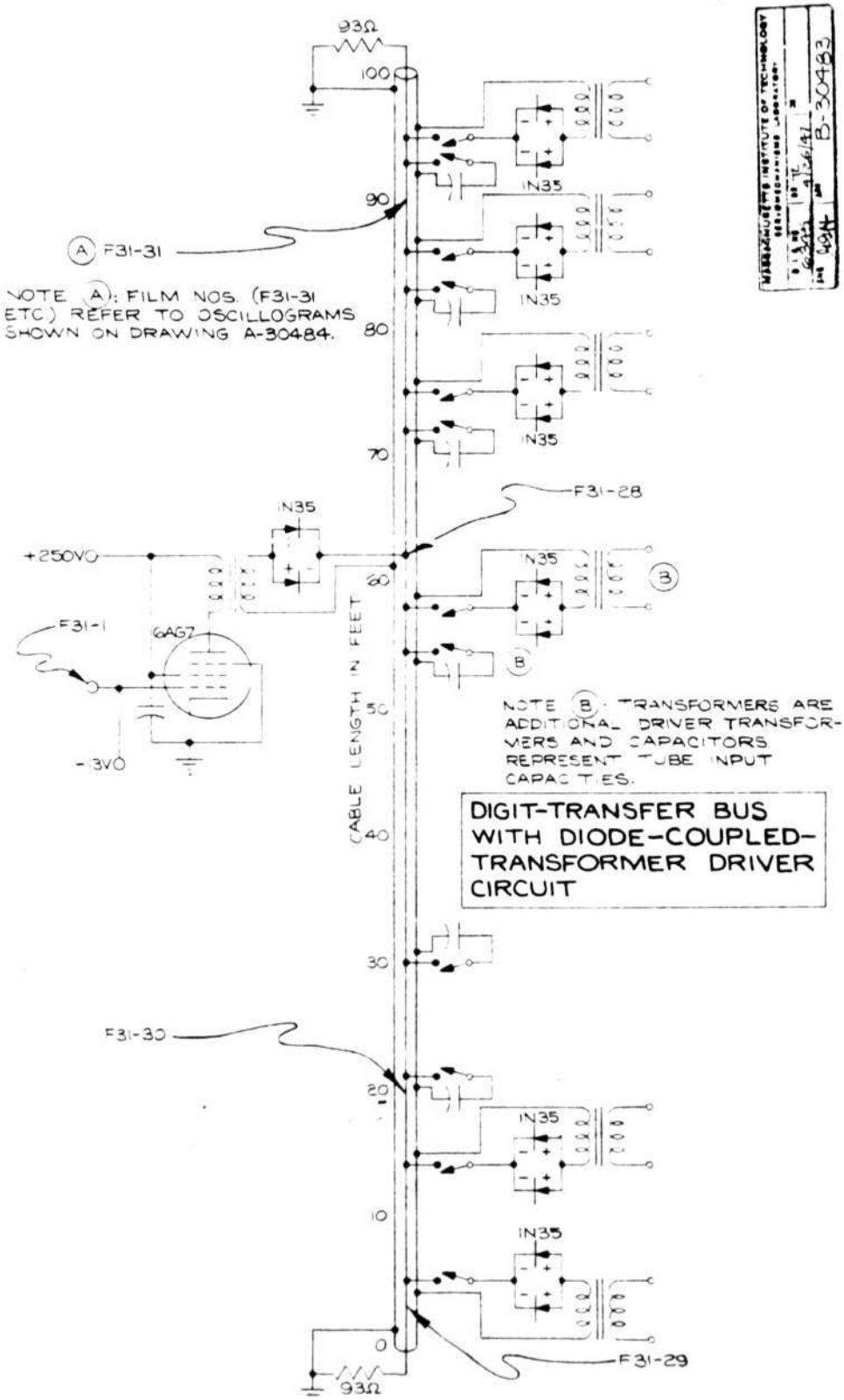
EQUIVALENT CIRCUIT OF LOAD PRESENTED BY INACTIVE DRIVER (DIRECT TRANSFORMER COUPLING)





PULSES ON DIGIT-TRANSFER BUS SHOWING LOADING EFFECT OF DIRECT-COUPLED DRIVER TRANSFORMER

USED IN 6345 REPORT R-121



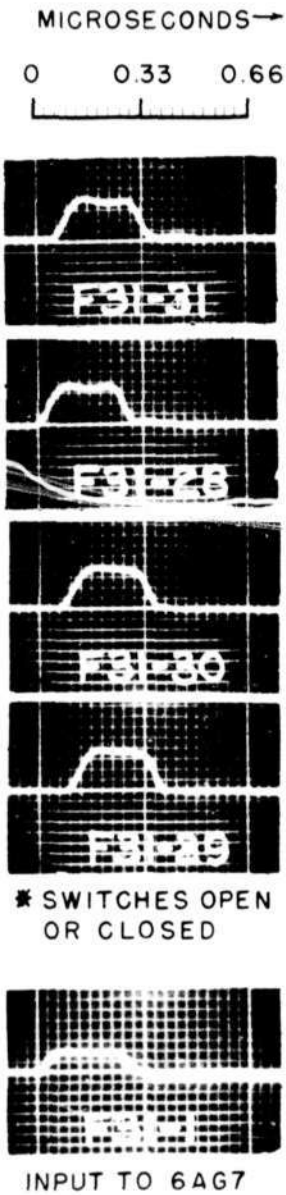
NOTE (A): FILM NOS. (F31-31 ETC.) REFER TO OSCILLOGRAMS SHOWN ON DRAWING A-30484.

NOTE (B): TRANSFORMERS ARE ADDITIONAL DRIVER TRANSFORMERS AND CAPACITORS REPRESENT TUBE INPUT CAPACITIES.

DIGIT-TRANSFER BUS WITH DIODE-COUPLED-TRANSFORMER DRIVER CIRCUIT

B-3048

T-5/2/47
T.H.L. 5/2/47
A-30484
6345



VERTICAL SCALE FACTOR
= 6.6 VOLTS PER DIVISION

* SWITCHES OPEN OR CLOSED

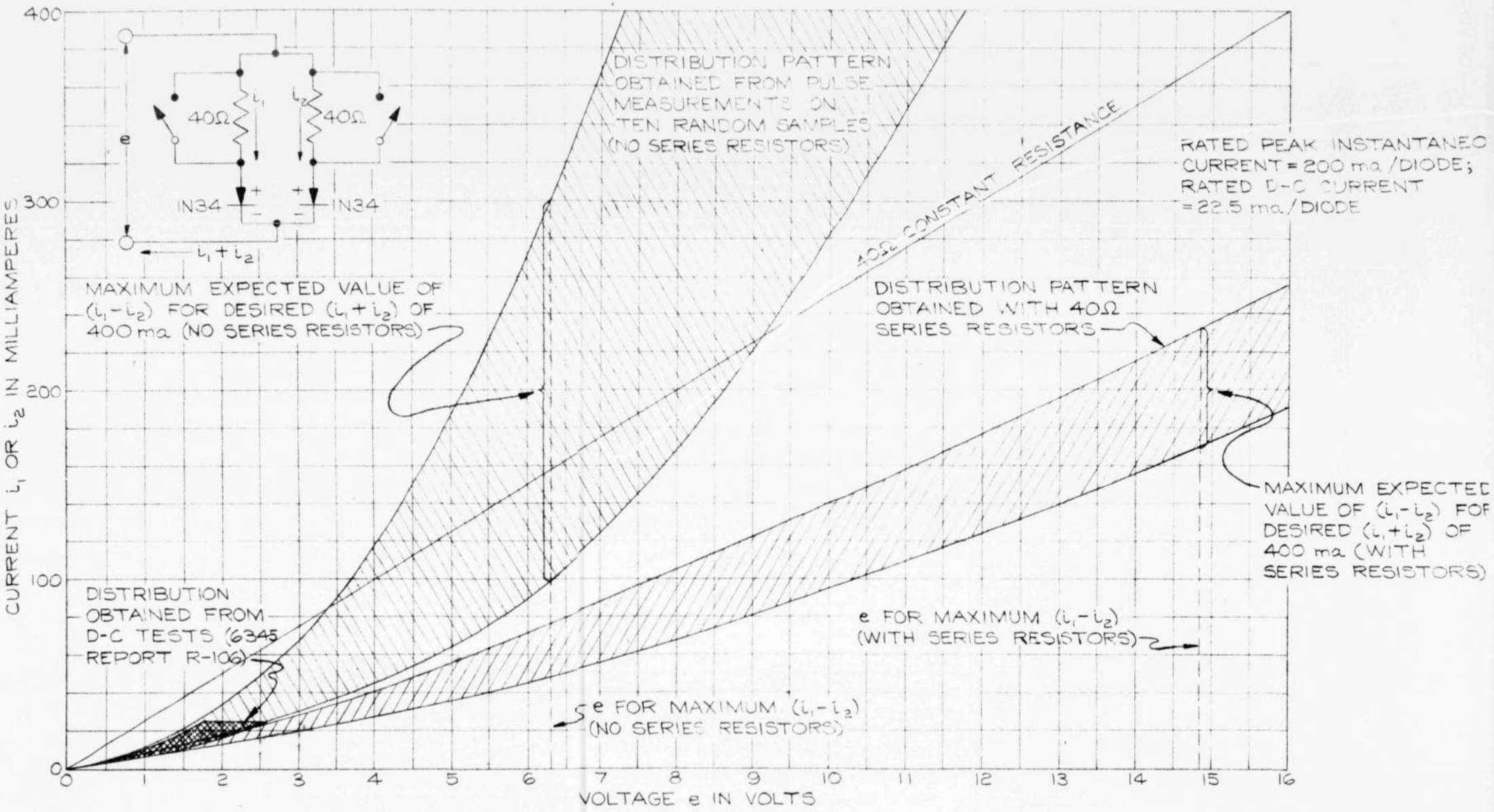
* SEE DRAWING B-30483

INPUT TO 6AG7

PULSES ON DIGIT—TRANSFER BUS WITH DIODE-COUPLED DRIVER TRANSFORMERS; NOTE THAT DRIVERS HAVE NO PERCEPTIBLE LOADING EFFECT

-30484

USED IN 6345 REPORT R-121



DATA FROM WAD 37-50
TESTS BY JAD DATE 4/8/47
ENGINEER IN CHARGE GGH

FORWARD CHARACTERISTICS OF SYLVANIA IN34 GERMANIUM DIODES, SHOWING EFFECT OF ADDITION OF RESISTANCE IN SERIES WITH EACH OF TWO PARALLELED DIODES

NOTE: DATA WAS OBTAINED BY MEANS OF APPLICATION OF 1-μs PULSES, AT 2000-CPS PRF, FROM CONSTANT-CURRENT SOURCE.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY

D. L. S. NO. 6345	DR. TL 5/6/47	CH.
SHT.	APP.	B-38187-G

Engineering Notes E-49

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge Massachusetts

To: 6345 Engineers

From: John O. Ely

6345

Subject: Control-line Calculations

Date: July 21, 1947

I. Introduction

In the WWI and WWII computer a number of types of control pulses must be supplied to the arithmetic and storage elements of the computer in such a manner that one or more gate tubes or flip-flops in each digit-section of the computer will receive each type of control pulse. Examples of such control signals are the shift-and-carry, shift-right, shift-left, clear, read-in, and read-out pulses. Each digit section of the computer probably will be mounted on a single rack with the racks arranged in a line so that the points to be supplied with any particular control signal will be spaced at regular intervals. The length of the interval will be equal to one rack width. It is proposed to use a single RG62/U coaxial line on each control signal with a tee connector and branch line at each load point. This note deals with methods of calculating the impedance at the input end, delay and attenuation in the line, correct value of terminating resistance on the line, and design of line driving amplifiers.

II. Calculations for Non-dissipative Loads

Loads which place a shunt conductance of 10^{-4} mho or less across the line may be considered in this class if it is not necessary to know accurately the attenuation in the line. An example of such a load is the control or suppressor grid of a gate tube having a grid-leak resistance of 10,000 ohms or more. (The grid must not be driven appreciably above cathode potential.)

In this case it is permissible to neglect the shunt conductance and consider the input capacity of the gate tube as if it were distributed along the line. The series inductance of the short branch coaxial line connecting the gate tube to the main line may be neglected and the capacity of this branch line added to the input capacity of the gate tube. Using the characteristic equations of a lossless transmission line, the characteristic resistance of the loaded line and the delay per section are then easily calculated, since the characteristics of the unloaded line are known.

Example:

A group of 6AS6 gate tubes are located on 2" centers. Control grids are to be driven from below cut-off to approximately cathode potential. A grid-leak resistance of 10,000 ohms will be used. The branch line at the tee is to be 6 inches of RG62/U cable. The main line also is composed of RG62/U cable. The following data are needed:

Characteristic resistance of line:	93 ohms
Capacitance of line	13.5 MMFD per foot
Input capacity of tube	4 MMFD (cold)

Series inductance of the line may be computed from the relation:

$$R_o = \sqrt{\frac{L}{C}} \quad ; \quad L = R_o^2 C = (93)^2(13.5)(10^{-12})$$

$$= 1.17 \times 10^{-7} \text{ henry/ft.}$$

Total shunt capacity of loaded line may be estimated:

Input capacity of tube when hot	6 μμfd	(50% greater than cold capacity)
Socket and wiring	4 μμfd	
Branch line and fittings	8 μμfd	
Main line	27 μμfd	
	45 μμfd	

Characteristic resistance of loaded line:

$$R_c = \sqrt{\frac{L}{L}} = \sqrt{\frac{2.39 \times 10^{-7}}{45 \times 10^{-12}}} = 72.1 \text{ ohms}$$

Delay per section of line:

$$T = \sqrt{LC} = \sqrt{2.34 \times 10^{-7}} \times 45 \times 10^{-12} = 3.24 \times 10^{-9} \text{ sec.}$$

This line, then, should be terminated with a 72 ohm resistor (actually 68 ohms will introduce negligible reflections), will present a load of 72 ohms, essentially resistive, to the driving source, and will introduce a delay of .0032 microseconds between each grid and the succeeding one in the line. Measurements on such a setup as this were made in the laboratory using 0.1 microsecond pulses. As measured, the characteristic resistance was 70.7 ohms and the delay per section was 0.0033

microseconds per section. Negligible de-shaping of the pulse occurred, and the attenuation in fifteen sections of line amounted to only about 3%.

III. Calculations for Linear Dissipative Loads

When the loads which are tied into the line have a shunt conductance of more than 10^{-4} mho each it is no longer permissible to neglect the losses in the loaded line. An example of such a load is a group of gate tubes at each load point whose combined grid-leak conductance is less than 10^{-4} mho. It is still permissible to consider the capacitance of the load and branch line as being distributed along the line uniformly, and in addition, the shunt conductance also may be considered as being distributed.

The equations which apply to this case are:

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \qquad \gamma = \sqrt{(R + j\omega L)(G + j\omega C)} = \alpha + j\beta$$

$$\left|\frac{E_0}{E_1}\right| = e^{-\alpha l}$$

$$T = \frac{\beta l}{\omega}$$

It is to be noted that the characteristic impedance and the propagation constant are both functions of frequency and are, in general, complex quantities. Since the systems now being designed will use pulses which resemble half-sine-waves in shape, a satisfactory approximation for Z_0 and γ are obtained by using a frequency whose half-period is equal to the nominal pulse duration. No satisfactory method is available for calculating the de-shaping of a pulse in the line, since such a calculation would require a Fourier analysis of the input pulse, separate calculations on each of the significant components using the above equations, and a synthesis of the results into an output pulse.

Measurements in the laboratory on a sixteen-section line of RG62/U cable with a 2" interval between load points and a load of 50 micro-mircofarads paralleled by 820 ohms at each tap show a delay of 0.07 microseconds for sixteen sections, an attenuation of 34%, and a characteristic resistance of 45 ohms. These figures are within 10% of values calculated using the equations given.

When the resistance at each load point is less than 500 ohms it may be possible in some cases to operate the line unterminated without introducing appreciable reflections. This will give a considerable improvement in the amplitude of the pulse at the gate tubes farthest from the sending end of the line.

IV. Calculations for Non-linear Loads

When the load to be driven is non-linear, as would be the case for a group of gate tube grids which are driven above cathode potential, no simple way of calculating line characteristics has been found. If, however, each non-linear impedance is shunted by a resistance which is low compared to the lowest value of the non-linear impedance a calculation made on the basis of a linear dissipative load equal to the shunting resistor will give accuracy adequate for design purposes.

V. Equalization of Signal at Driven Points

If a number of gate tubes are to be driven, it may be necessary to use some form of equalization at the branch points in order to maintain nearly constant gate tube output from one end of the line to the other. This equlization may take the form of a capacity-compensated L-pad or T-pad attenuator inserted in each branch line, the ratios of the attenuators being adjusted so that all gate tube grids receive the same amplitude pulse.

VI. Driver Amplifier Design

If the loading, pulse amplitude, duration, and duty factor on any control line can be specified a suitable driver amplifier can be designed. Characteristic, attenuation, and delay of the line should be calculated first. Desired pulse amplitude at the end of the line divided by the ratio of output voltage to input voltage gives the required amplitude of the input pulse. Input pulse amplitude divided by characteristic impedance of the line gives the current required form the driving source. This source in all cases will be a tetrode or pentode tube with a step-down transformer in its plate circuit. Transformer turns ratio will be about 3:1 in most cases. The driver-tube plate current will then have to be one-third of the required output current. It is necessary to choose a tube and operating conditions such that the required current may be obtained without exceeding dissipation ratings on the screen or plate of the tube. In addition, it is desirable to avoid plate and screen voltages greater than 300 volts and also to avoid driving control grids appreciably positive. The worst case expected in the WWI and WWII computers will have an input impedance of about 40 ohms and an attenuation of about 15% per section and will require a pulse amplitude of about 30 volts at the end of ten sections with a duty factor of 4%. A type RK4D32 beam tetrode operating with a screen potential of 300 volts, plate supply of 400 volts, control grid bias of -50 volts, pulse input amplitude of +50 volts, and using a 1:10 output transformer ratio can supply sufficient power for this case. For situations which require less power, in fact for most of the control lines in WWI and WWII, one half of a type 3B29 tube operating with 250 volts plate and screen supply and 45 volts bias can supply more than ample power.

JOE:vh

John O. Ely
John O. Ely

Engineering Notes E-59

Servomechanisms Laboratory
Massachusetts Institute of Technology

To: 6345 Engineers, Sylvania (3) 6345

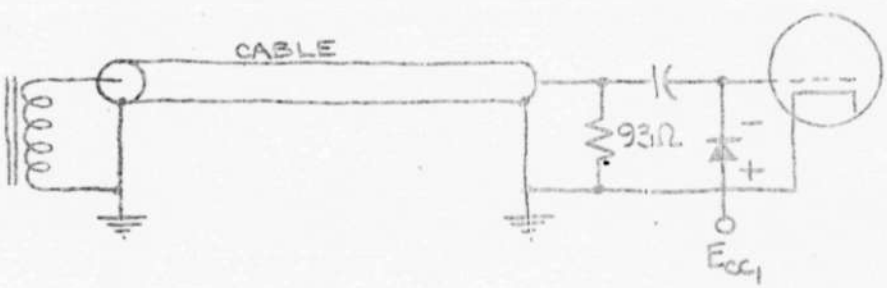
From: David R. Brown

Subject: Point-to-Point Signal-Cable Termination

Date: August 29, 1947

This engineering note proposes a method of using a 93-ohm terminated cable for transmission from point to point. The proposed method is designed to minimize signal bias at the input to the tube at the receiving end.

If only linear elements are used to terminate the cable, the effective bias will be a function of the repetition frequency because the average voltage developed across the secondary of the transformer must be zero. In addition, if the grid is driven positive, the signal bias will be increased because the tube tends to clamp the signal at cathode potential. Both of these effects are minimized by the method shown here:



The signal will be clamped at E_{cc_1} by the crystal rectifier. The time constant of the coupling condenser and the input resistance of the tube must be made long compared to the pulse length and the time constant of the coupling condenser

and the forward resistance of the crystal must be made short compared to the pulse interval.

David R. Brown

David R. Brown

DRB:vh

ENGINEERING NOTES NO. E-60

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

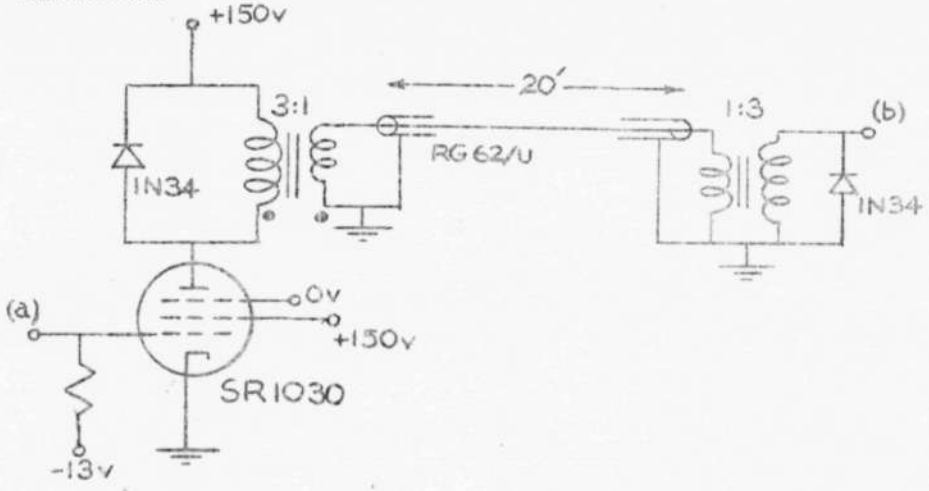
TO: 6345 Engineers 6345

FROM: G. G. Hoberg Page 1 of 2 pages

SUBJECT: Transmission of Gated Signal to Remote Point without Buffer Amplifier

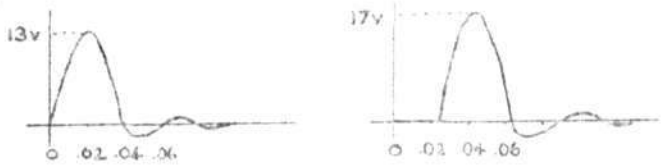
DATE: September 16, 1947

Wherever signals from gate tubes are to be used at points distant from the tubes, present circuit designs require buffer amplifiers to drive 93-ohm transmission lines. It is believed that the method shown below, which follows a suggestion made some time ago by T. F. Wimett, will obviate the need for the line-driving amplifiers if gating is done with tubes of the type being developed to replace the 6AS6. However, there is at present no definite assurance that these tubes will be available for use in Whirlwind I.



This circuit was constructed using standard 3.1 pulse transformers (363 or 72h) and a tube from a sample shipment received from Sylvania. Note that no terminating resistors are used. The crystal rectifiers serve to remove large overshoots which otherwise occurred after the pulses.

Half-sinusoid pulses of .04 μsec. duration at a p.r.f. of one megacycle were applied at (a). The following waveforms were observed:



The output pulses were used successfully to operate a standard flip-flop (Drawing SB-39281) when applied to the grid of its trigger tube.

With the secondary connections of the output transformer reversed, pulses of similar waveform but opposite polarity were obtained at (b), and when applied to the grid of the conducting tube successfully triggered the flip-flop.

Further applications of this general scheme, and in particular of step-up pulse transformers, will be investigated.

G. G. Hoberg

G. G. Hoberg

GGH:hes

ENGINEERING NOTES NO. E-33

TO: 6345 Engineers 6345

FROM: John O. Ely Page 1 of 2 pages

SUBJECT: Flip-flop Used as Variable Frequency Square-Wave Generator Drawing: B-30328

REFERENCE: Engineering Notes Nos. E-31 and E-32

DATE: February 20, 1947

The circuit described in these Notes was designed for use as a source of approximately square waves of variable frequency to be used for testing transient response of video amplifiers. Following characteristics were desired:

1) Balanced output of a magnitude of at least 10 volts across a load of 20,000 ohms shunted by 15 micromicrofarads.

2) Rise time of 1/4 microsecond or better.

3) Substantially flat top on output pulse.

4) Period of square wave determined by frequency of sine wave taken from Model LP-5 Signal Generator and variable from less than 2 to more than 10 microseconds.

Drawing No. B-30328 is a schematic of the circuit constructed. One of the standard flip-flops developed by John J. O'Brien was chosen for the output stage, since this easily meets the output requirements and already had been engineered and tested. In order to allow triggering of the flip-flop from the LP-5 Signal Generator, it was necessary only to provide two stages for amplification and shaping, plus a clipping diode. A breadboard was constructed following this circuit and was used successfully. In operation a sine wave of any frequency from about 150 kc to 1.2 mc and of approximately 1/2 volt r.m.s. amplitude is fed into the input jack. The input voltage is stepped up by a ratio of approximately 3:1 in the input auto-transformer and applied to the grid of the first amplifier. This amplifier is slightly overdriven and the waveform at its plate is a sine wave clipped somewhat on both negative and positive swings. The second amplifier is considerably overdriven and its grid current helps to flatten the waveform at its grid. In the plate circuit of the second amplifier is a pulse transformer connected for a 2:1 step up with polarity reversal. A bias of about +10 volts is supplied to the low side of the transformer output winding and the high side of the winding is connected through a clipping diode to the common cathode resistor of the flip-flop. Since a bias of about +30 volts is developed across this resistor by plate and screen current through the flip-flop, only a small portion of the top of the waveform at the plate of the clipping diode appears at the cathodes of the flip-flop.

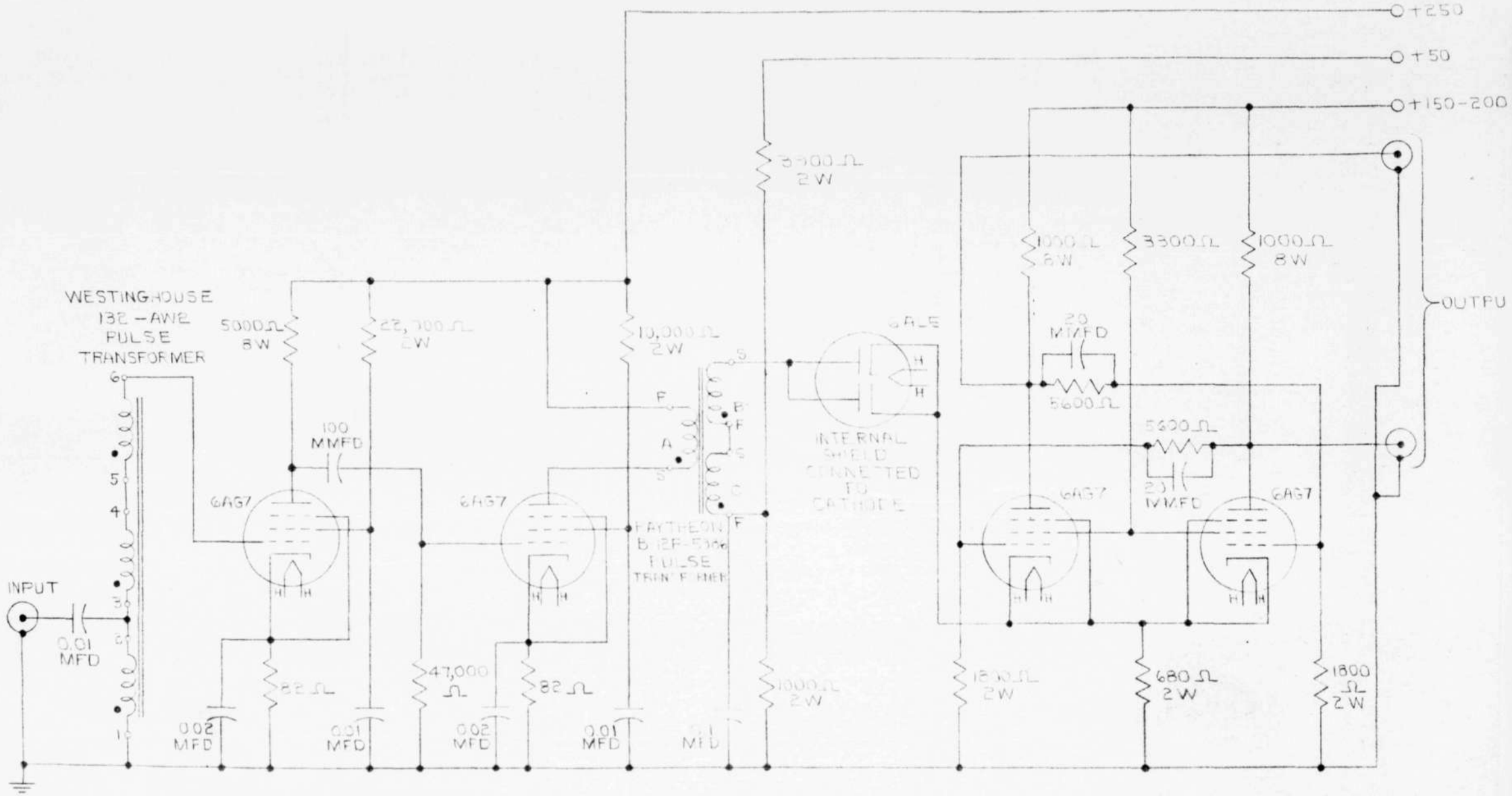
The voltage which does appear is sufficient to trigger the flip-flop. The flip-flop switches once for each trigger, therefore, the period of the square-wave output is twice the period of the sine wave input. Although the diagram shows output taken directly from the flip-flop plates such connection will work only for high impedance load. Low impedance loads may be driven at lower voltages by isolating them from the flip-flop plates by means of a parallel R-C combination of not less than 5000 ohms resistance and not more than 5 microniorofarads capacitance.

Examination of the waveforms in the completed breadboard show that minor circuit modifications in the clipping stage probably would lead to considerably better performance. Polarity of the secondary of the pulse transformer feeding the clipper should be changed to utilize the inductive overswing on the tail of its output pulse rather than the pulse itself. A pair of 1N34 crystal diodes in series should be shunted across the secondary of the transformer to allow faster build-up of primary current when the second amplifier tube conducts. The 6AL5 clipping diode should be replaced by a single 1N34 crystal diode to reduce the capacity shunting the pulse transformer and to secure a lower forward resistance. Some adjustment of the bias on the clipping diode anode will be necessary if the other changes are made.

John O. Ely

John O. Ely

JOE:has



VARIABLE – FREQUENCY SQUARE–WAVE GENERATOR

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. WG. NO. C243	DR. DLG 2/7/47	CK. TL 2/7/47
ENG. [illegible]	APP. B-30328	

ENGINEERING NOTES NO. E-33

TO: 6345 Engineers 6345

FROM: John O. Ely Page 1 of 2 pages

SUBJECT: Flip-flop Used as Variable Frequency Square-Wave Generator Drawing: B-30328

REFERENCE: Engineering Notes Nos. E-31 and E-32

DATE: February 20, 1947

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1) Balanced output of a magnitude of at least 10 volts across a load of 20,000 ohms shunted by 15 micromicrofarads.

2) Rise time of 1/4 microsecond or better.

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4) Period of square wave determined by frequency of sine wave taken from Model LF-5 Signal Generator and variable from less than 2 to more than 10 microseconds.

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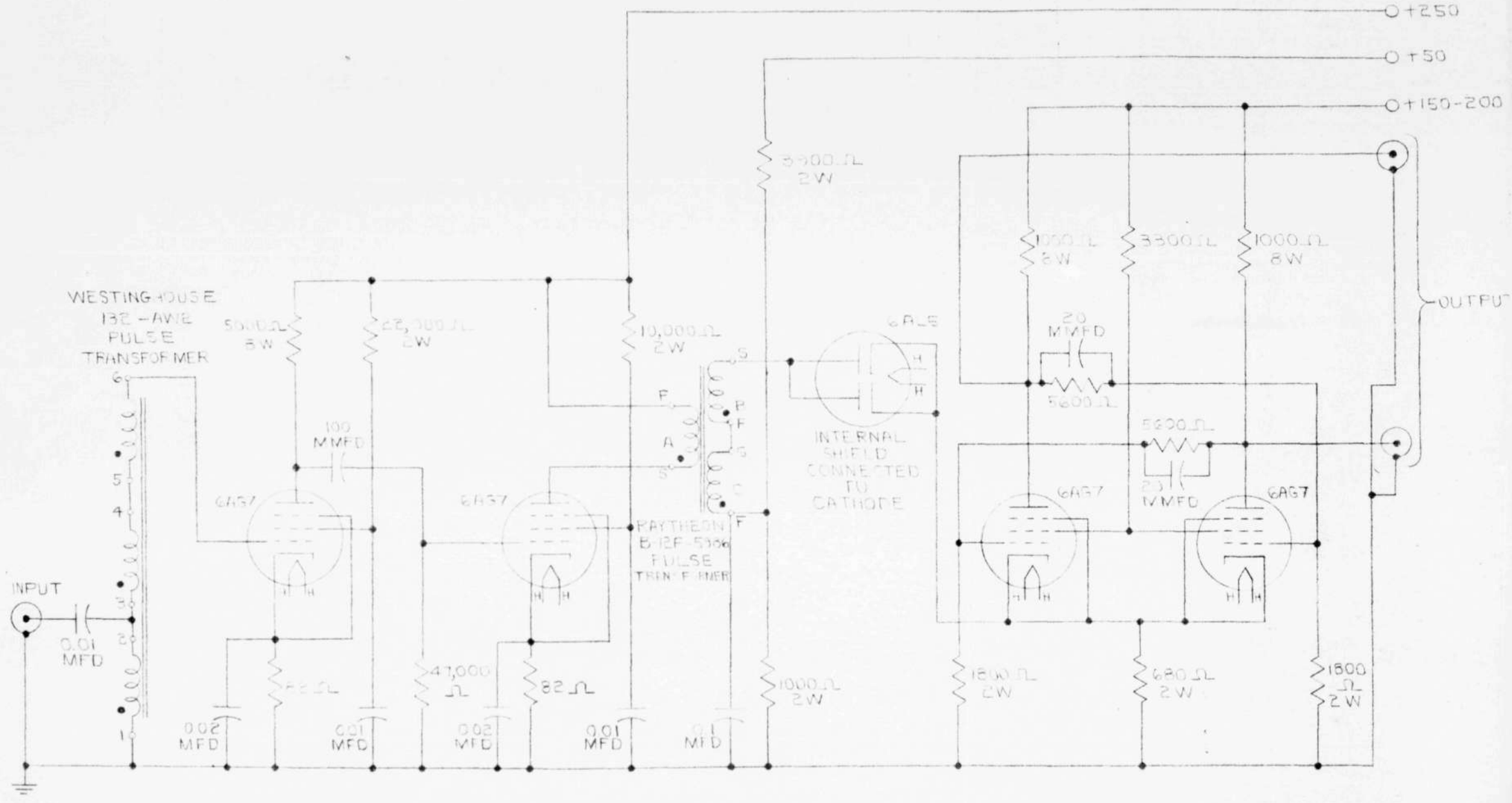
Examination of the waveforms in the completed breadboard show that minor circuit modifications in the clipping stage probably would lead to considerably better performance. Polarity of the secondary of the pulse transformer feeding the clipper should be changed to utilize the inductive overswing on the tail of its output pulse rather than the pulse itself. A pair of 1N34 crystal diodes in series should be shunted across the secondary of the transformer to allow faster build-up of primary current when the second amplifier tube conducts. The 6AL5 clipping diode should be replaced by a single 1N34 crystal diode to reduce the capacity shunting the pulse transformer and to secure a lower forward resistance. Some adjustment of the bias on the clipping diode anode will be necessary if the other changes are made.

John O. Ely

John O. Ely

JOE:hns



VARIABLE - FREQUENCY SQUARE-WAVE GENERATOR

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY

DWG. NO. 6248	BY DLG 2/7/47	DR. TL 2/7/47
ENG. JS.	APP.	B-30329

ENGINEERING NOTES NO. E 54

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: 6345 Engineers 6345

FROM: J. O. Ely

SUBJECT: Feedback Applied to Gated Amplifiers Drawings: SA-39313

DATE: August 13, 1947

Recently several persons have suggested the possibility of applying feedback to gated amplifiers used in WWI circuits. This note is intended to bring the proposals so far advanced to the attention of all interested persons in order that any pertinent comments and suggestions may be elicited.

Three principle benefits have been suggested as being obtainable from the use of feedback. First, a considerably larger gain may be achieved if regenerative feedback is applied from output to input. Second, application of a large amount of regenerative feedback in a properly arranged circuit will make the shape, amplitude, and duration of the output pulse substantially independent of input amplitude. Third, either positive or negative feedback may be used to increase the input impedance of the gated tube. Since negative feedback decreases the gain of the stage by the same factor that it increases the input impedance use of degeneration has not been considered desirable.

Drawing SA-39313 is one possible type of gated amplifier circuit with regenerative feedback applied. In this case feedback is applied from the secondary of a 1:1 inverter pulse transformer in the plate circuit of the gate tube to the grid of the tube. Two type IN-4 crystal diodes are used in the grid circuit to provide isolation between input and output. The following points should be noted in connection with this circuit:

1. A pulse transformer is required for operation even if negative output pulses are desired.

2. No regenerative action is secured unless

   a. The input pulse exceeds a certain threshold amplitude, namely the amplitude at which the input and output pulses are of equal amplitude, and

   b. The gain around the feedback loop is greater than unity when condition a is satisfied.

3. An inherent delay in the feedback loop exists because the feedback voltage is derived from the secondary of the pulse transformer. This means that the output pulse will be of somewhat larger duration than the input pulse in general.

4. The shape of the output pulse will depend more on the characteristics of the pulse transformer used and the loading of this transformer than on the shape of the input pulse.

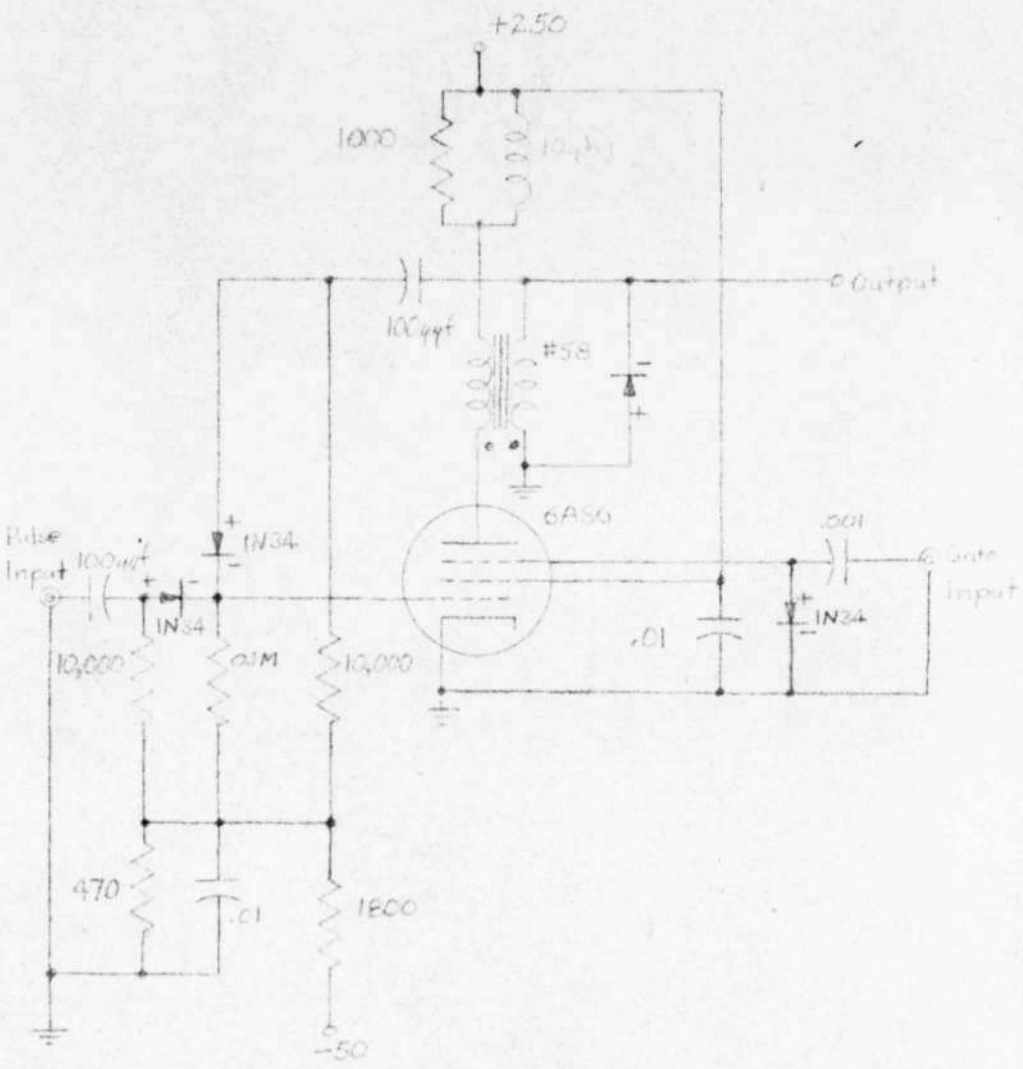
A breadboard of the circuit of Drawing SA-39313 was constructed and operated in the laboratory. Operation on 1/20 microsecond pulses was satisfactory except that abnormally high plate and screen voltages were necessary to meet the condition 2a above. This may be due to the characteristics of the pulse transformer used, as this transformer was designed for an entirely different application.

Numerous other circuit arrangements are possible but have not been investigated.

John O. Ely

JOE/rp

SA-39313



GATED
REGENERATIVE AMPLIFIER

MASSACHUSETTS INSTITUTE OF TECHNOLOGY SERVOMECHANISMS LABORATORY		
D. C. NO. 6345	DR J.P.E. 5/6/47	SI
ENG J.C.L.	MP SA-39313	

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: SYMPOSIUM ON PRINTED CIRCUITS

To: 6345 Engineers

From: D. R. Brown

Date: October 17, 1947

A technical Symposium on Printed Circuits under the sponsorship of the Aeronautical Board with the cooperation of the National Bureau of Standards was held in Washington, D. C., on October 15, 1947. Since complete proceedings of the symposium will be available in about two months, no effort to describe the symposium in detail will be made here. Also, the Bureau of Standards has prepared a pamphlet entitled "Printed Circuit Techniques" which is available from the Superintendent of Documents. Several interesting points were made at the symposium and will be mentioned here.

An advantage of printed circuits, even greater than the advantage of small size, is adaptability to mass production. It is this advantage which has held the interest of the military. Small size is a big advantage; but in many cases, the heat dissipation rather than component size puts the limit on the size of the equipment. Another advantage of printed circuits is their adaptability to plug-in units. Hermetically-sealed, plug-in units have been produced for some military applications. The military is very interested in obtaining long-life units for operation of unattended stations and is pushing the development of long-life tubes, stable resistors, etc. The big disadvantage of printed circuits at the present time is an inability to obtain accurate components. This is particularly true of resistors. Very few organizations have been able to print resistors satisfactorily. Extremely elaborate production controls must be set up in order to print the resistors, and the few manufacturers who are doing this work are keeping the details secret. The Bureau of Standards has published some material on printed resistors, however.

No work has been done on video amplifiers. Dr. Brunetti feels that there is no reason that printed circuits cannot be used for video amplifiers. He suggests starting with conventional layout dimensions and gradually reducing the size of the circuits as more and more printed-circuit techniques are introduced.

Signed D. R. Brown
D. R. Brown

DRB/sp

ENGINEERING NOTES NO. 55

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

TO: 6345 Engineers, Sylvania (3), Walter Cook, Hal Mercer — 6345

FROM: David R. Brown — Page 1 of 4

SUBJECT: Register Panel — Drawings: SA-39292-1

DATE: August 14, 1947

ENCLOSURE: List of Drawings (SA-39292-1)

The drawings listed in the enclosure show the present state of development of the register panel for WWI. The design, although incomplete, has been carried far enough to be taken over by Sylvania. This Engineering Note discusses the design, showing where it is incomplete or subject to change.

Check Register

The block schematic, SB-39280-1, is all right except that a buffer amplifier may be placed between the flip-flop and the gate tube. A decision will be made by August 27.

The circuit schematic, SD-39282-2 may have the following changes.

1. A buffer amplifier may be necessary between the flip-flop and the gate tube.

2. Tube V101 may be replaced by a special gate tube. The decision may be made as late as November 1.

3. Tubes V105 and V106 may be replaced by a single special gate tube.

4. The pulse length may be changed thereby changing the pulse-transformer type and possibly a few components in the plate-load circuits of V101, V105, and V106.

A decision will be made by August 27.

5. The input circuit to V102 may have to be revised. The revision may be little more than changing the values of the components. A decision will be made by September 3.

6. The tube type for V107 may be changed. A decision should be made by August 27.

7. L-C filters will have to be added for decoupling. This should be done by August 27.

8. Precision resistors, as yet unspecified, will be used in the flip-flop. No date can be specified.

The sub-panel layout, D-30798, is all right for the present circuit schematic. Revisions in the circuit schematic will be reflected in the sub-panel layout. Also, a change in the pulse-transformer mounting, indicated in the sub-panel layout for the program register, has been made.

Program Register

The block schematic, SB-79289-1 is all right except that a buffer amplifier may be placed between the flip-flop and the gate tube. A decision will be made by August 27.

The circuit schematic, SD-79283-2 may have the following changes:

1. A buffer amplifier may be necessary between the flip-flop and the gate tube.

2. Tube V201 may be replaced by a special gate tube. The decision may be made as late as November 1.

3. Tubes V205 and V206 may be replaced by a single special gate tube.

4. The pulse length may be changed thereby changing the pulse-transformer type and possibly a few components in the plate-load circuits of V201, V205, and V206. A decision will be made by August 27.

5. The tube type for V307 may be changed. A decision should be made by August 27.

6. L-C filters will have to be added for decoupling. This should be done by August 27.

7. Precision resistors, as yet unspecified, will be used in the flip-flop. No date can be specified.

The sub-panel layout, D-30799, is all right for the present circuit schematic. Revisions in the circuit schematic will be reflected in the sub-panel layout.

Program Counter

The block schematic, SB-39291-1, is all right except that a buffer amplifier may be placed between the flip-flop and the gate tubes. A decision will be made by August 27.

The circuit schematic, SD-39284-2, may have the following changes:

1. A buffer amplifier may be necessary between the flip-flop and the gate tubes.

2. Tube V301 may be replaced by a special gate tube. The decision may be made as late as November 1.

3. Tubes V305 and V310 may be replaced by a single special gate tube.

4. Tubes V306 and V311 may be replaced by a single special gate tube.

5. Tubes V309 and V308 may be replaced by a single special gate tube.

6. The pulse length may be changed thereby changing the pulse-transformer type and possibly a few components in the plate-load circuits of V301, V305, V306, V308, V309, V310, and V311. A decision will be made by August 27.

7. The tube for V307 may be changed. A decision should be made by August 27.

8. L-C filters will have to be added for decoupling. This should be done by August 27.

9. Precision resistors, as yet unspecified, will be used in the flip-flop. No date can be specified.

10. The mixing circuit at the input to V302 may be revised. The revision may be little more than changing the values of the components. A decision will be made by September 3.

The sub-panel layout, D-30800, is all right for the present circuit schematic. Revisions in the circuit schematic will be reflected in the sub-panel layout.

Register Panel

The block schematic, D-30773, is based upon the three block schematics for the check register, program register, and the program counter. Any changes in those three block schematics must also be made in the register-panel block schematic.

The panel layout, R-30797, is still in the design stage. A tentative cable layout has been made. However, no power cables have been indicated and none of the connections to the operator's desk are shown.

David R. Brown
David R. Brown

DRB/rp

REGISTER PANEL

LIST OF DRAWINGS

REGISTER PANEL

BLOCK SCHEMATIC	D-30773
MAIN PANEL & CABLE PLAN LAYOUT	D-30797

CHECK REGISTER

BLOCK SCHEMATIC	SB-39288-1
CIRCUIT SCHEMATIC	SD-39282-2
DRILLING TEMPLATE & ASS'Y	D-30798

PROGRAM REGISTER

BLOCK SCHEMATIC	SB-39289-1
CIRCUIT SCHEMATIC	SD-39283-2
DRILLING TEMPLATE & ASS'Y	D-30799

PROGRAM COUNTER

BLOCK SCHEMATIC	SB-39291-1
CIRCUIT SCHEMATIC	SD-39284-2
ASSEMBLY	D-30800

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: REGISTER PANEL SCHEMATIC CHANGES (SD-39282-3, SD-39283-3, SD-39284-3)

To: Jay W. Forrester, H. Fahnestock, D. R. Brown, R. Best, J. A. O'Brien and Sylvania (3 copies)

From: David J. Crawford

Date: September 25, 1947

Changes have been made in the register panel circuits. Most of these changes consist of the substitution of 1N34 crystal diodes in place of grid resistors so that clamping action will tend to keep the baselines of the waveforms at a fixed bias. Most of these changes are in addition to those specified in Engineering Notes No. E-55, August 14, 1947.

The following is the list of changes:

SD-39282-3 Check Register Schematic

CR108 replaces R101
CR109 replaces R104
CR110 replaces R105
CR111 replaces R106
CR112 replaces R107
CR113 replaces R125

R132 and R133 added to reduce the signal amplitude from the flip-flop, thereby causing the lights to be brighter.

V107 changed from 2051 to 6SN7.
Connection shunting R131 eliminated.

SD-39283-3 Program Register Schematic

CR207 replaces R201
CR208 replaces R204
CR202 replaces R220

R206 eliminated.

R229 and R230 added to brighten lights.

"R215, 1600 Ω, 2W, WW", changed to read,
"R215, 1600 Ω, 8W, WW".

"R226, 3300 Ω, 2W" changed to read,
"R227, 3300 Ω, 2W".
V207 changed from 2C51 to 6SN7.

SD-39284-3 Program Counter Schematic

CR314 replaces R301
CR315 replaces R302
CR316 replaces R328
CR317 replaces R331
CR318 replaces R309
CR319 replaces R319
CR320 replaces R320

CR321 and CR322 added for damping purposes.

R341 and C324 added.

R310, CR301, C307, and DR301 eliminated.

R308 changed from 0.1 MEG to 10,000 Ω.

"R325, 1,000Ω." changed to read, "R326, 1,000 Ω."

"CR306, 1N34", at grid of V304, changed to read "CR305, 1N34".

Bias of CR318 and CR319 made the same as that of R308. (This change makes the mixing circuit similar to that used in the Check Register Schematic, SD-39282-3).

C315 changed from 0.01 MFD. to 0.001 MFD.

R339 and R340 added to brighten the lights.

Connection between C303 and C319 eliminated.

Connection between CR309 and ground eliminated.

V307 changed from 2C51 to 6SN7.

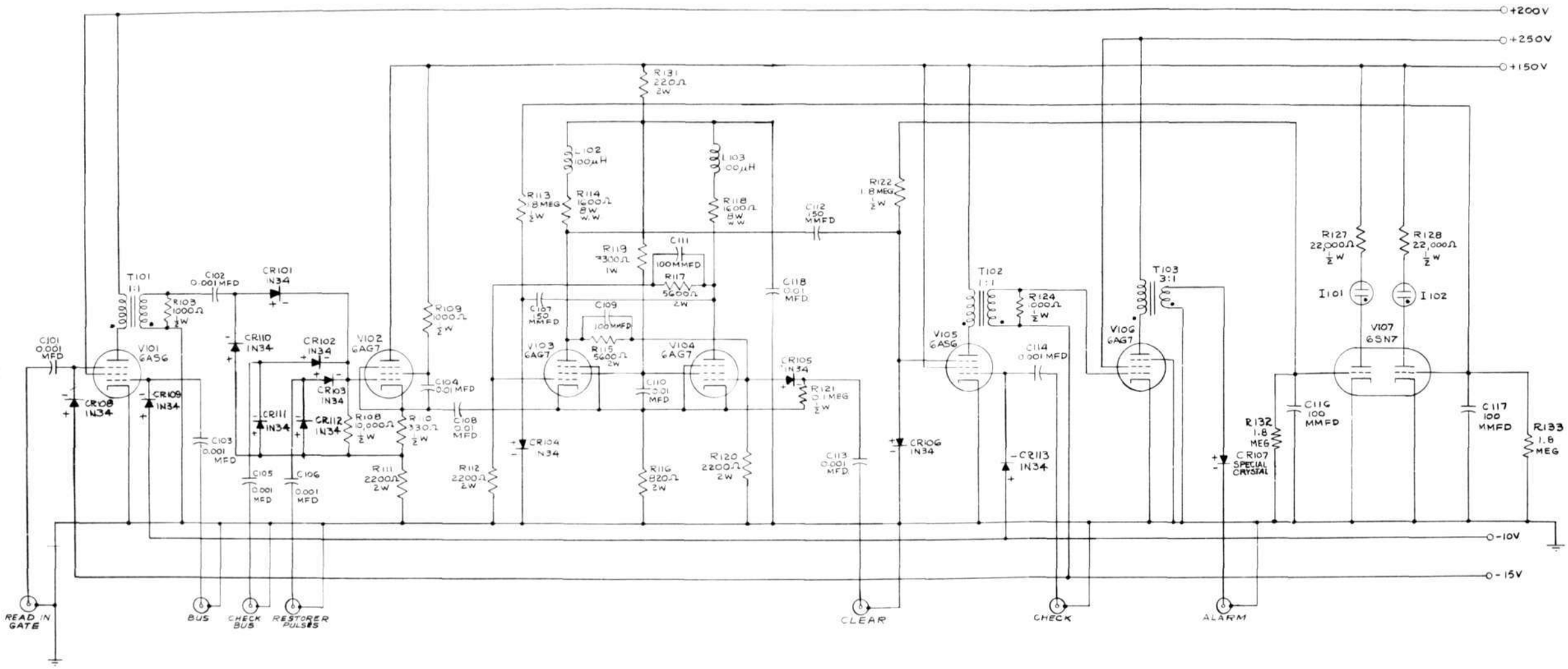
There probably will be a two-section R-C delay circuit added between the flip-flop and grid 3 of V309 to fulfill the function of DM301. A decision is being withheld pending further work on the circuit.

References: Engineering Notes No. E-55, August 14, 1947.

Signed: David J. Crawford
David J. Crawford

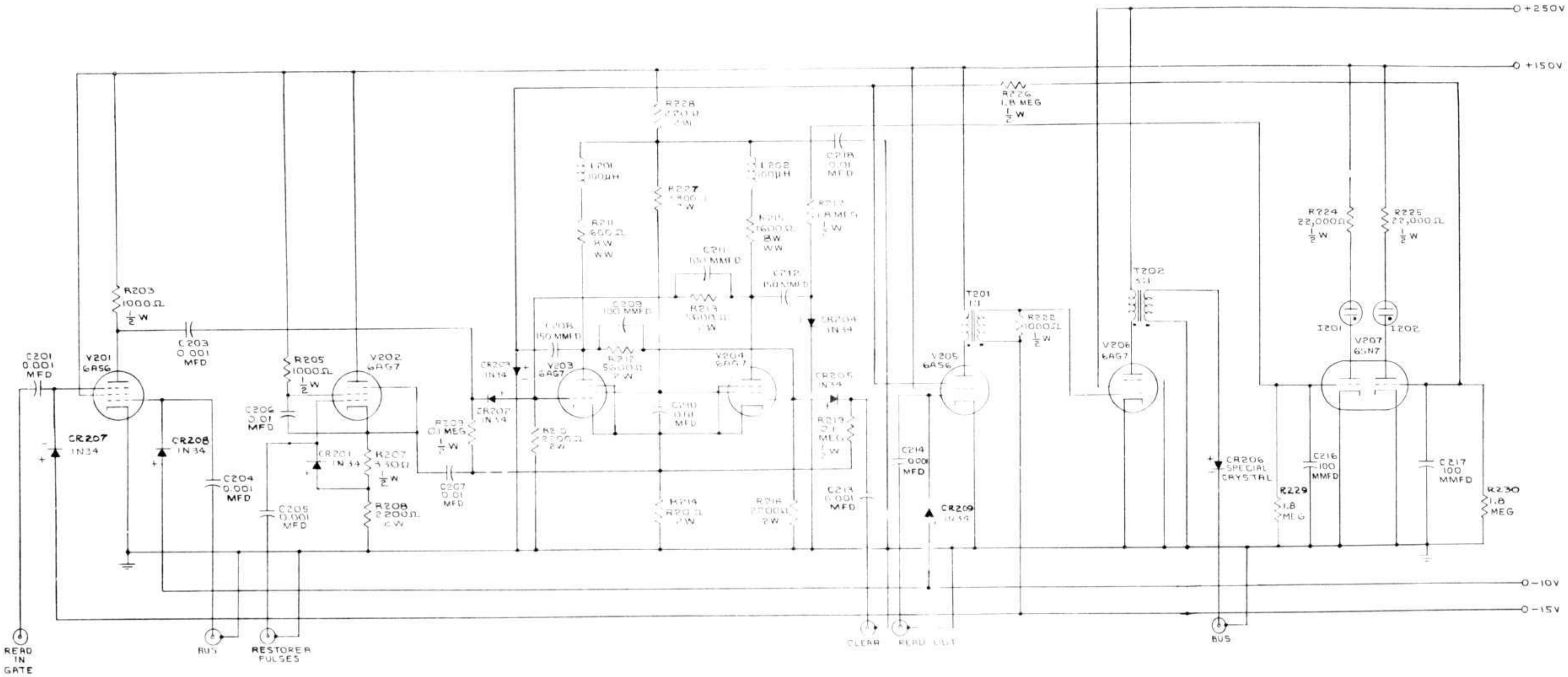
Approved: NH Taylor
for David H. Brown

DJC:vh



CHECK REGISTER
CIRCUIT SCHEMATIC

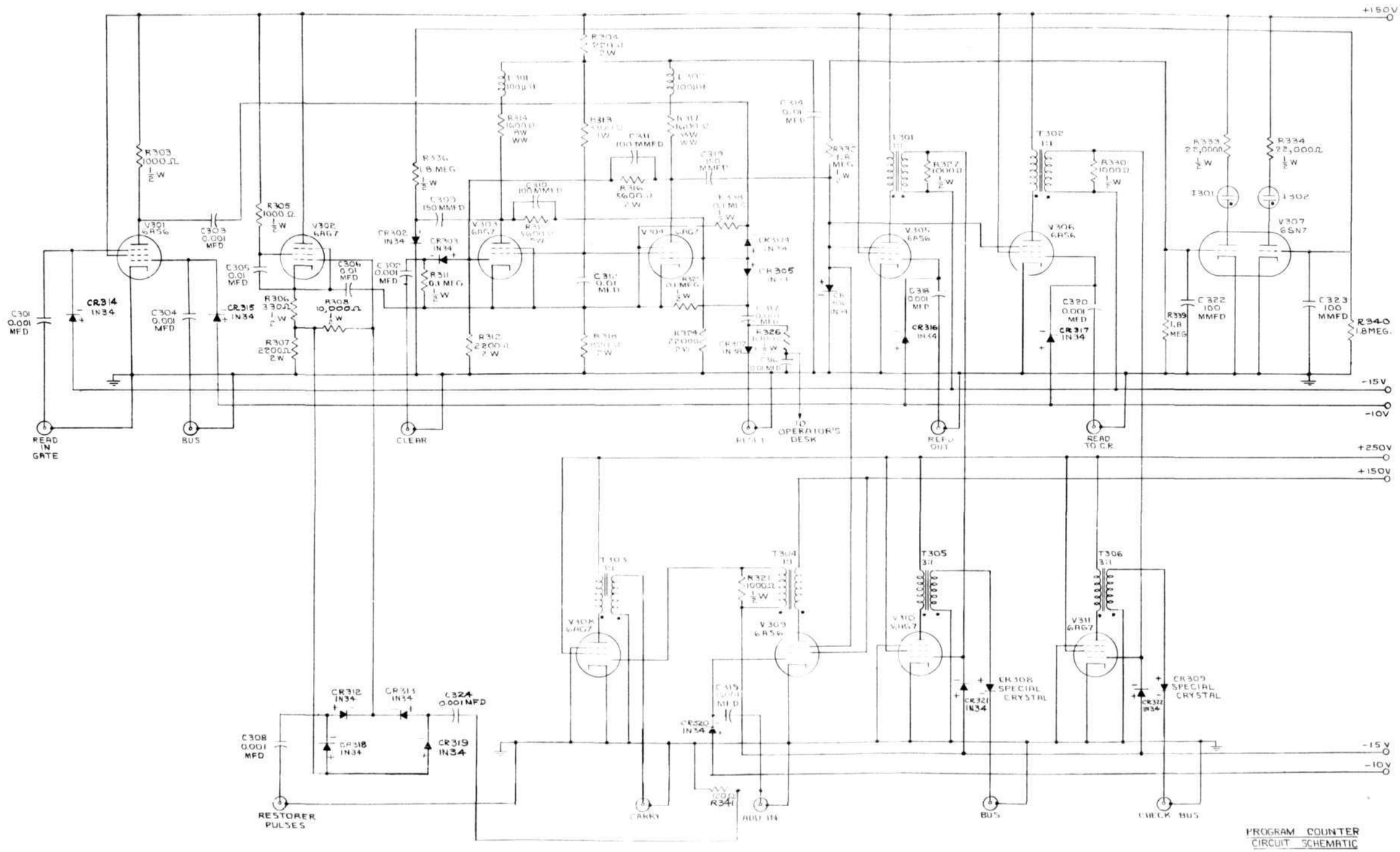
MASSACHUSETTS INSTITUTE OF TECHNOLOGY	
D.C.L. 6.345	J.F. BRUNNING 8-14-47
(DWG.)	MIT CT-392B2-3



PROGRAM REGISTER CIRCUIT SCHEMATIC

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

SD-39283



PROGRAM COUNTER
CIRCUIT SCHEMATIC

SD-39294-3

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: FLIP-FLOP STORAGE, POSSIBLE CHANGES

To: J.W. Forrester, H. Fahnestock, R.R. Everett, D.R. Brown, N.H. Taylor, J.A. O'Brien, C.W. Watt, R. Best, Sylvania (3)

From: D. J. Crawford

Date: October 3, 1947

The drawings listed in SA-39365 show the present state of the flip-flop storage panel for WWI. The design, although not complete, is sufficient to be developed by Sylvania. This Engineering Note describes possible changes in the design that may be necessary.

SD-39277-1, Storage, General Arrangement

"Complement" will be changed to read, "Restorer Pulses".

The drawing numbers of the block schematics of the units will be added inside the blocks representing the units.

SD-39278-1 Flip-Flop Storage-Block Schematic

"Complement" will be changed to read, "Restorer Pulses".

The method of feeding the restorer pulses will probably be changed. Either one tube will feed the flip-flops of each digit, or one tube will feed the flip-flops of one number. The decision will be made when further investigation has been completed.

SD-39285-3 Flip-Flop Register-Circuit Schematic

V404 and V405, type 6AS6, may each be replaced by a special type gate tube.

The number 3 grids of V404 and V405 may be connected together and have a single input from the storage switch.

V401 trigger tube may be replaced by a connection from a trigger tube common to each digit, or a trigger tube common to each number.

R423 and C416 decoupling network will probably be replaced by an L-C decoupling network. Similar networks may be necessary in the plate circuits of V401 and V404.

Precision resistors may be used in the flip-flop circuit.

Connections will be added to the indicating light circuits to provide for remote indication at the operator's desk.

D-30872 Flip-Flop Register Assembly and E-30900 Flip-Flop Register Panel Assembly

At present these drawings are in conflict with SD-39285-3. However, it serves to indicate a general scheme of layout, the minor discrepancies causing little distraction to this purpose. It will probably not be brought up to date until the design work has reached a more concrete stage.

SD-39286-3 Flip-Flop Storage Output-Circuit Schematic

V903, V904, and V905, type 6AS6, may each be replaced by a special type gate tube.

A trigger tube may be added to feed restorer pulses to the flip-flops of that particular digit.

L-C filters may be added to some or all of the plate circuits for decoupling purposes.

The pulse length may be changed. This would possibly result in changing the transformer type and perhaps the terminating circuit of the transformer.

D-30879 Flip-Flop Storage Output-Assembly and E-30976 Flip-Flop Storage Output-Panel Assembly

At present these drawings conflict with SD-39286-3. Remarks under D-30872 also apply here.

Drawing: SA-39355 - Flip-Flop Storage Panel-List of Drawings

David J. Crawford
David J. Crawford

David R. Brown
David R. Brown

DJC/rp Approved by:

TL 10/3/47 SA-39355

6345 BJC

FLIP-FLOP STORAGE PANEL
LIST OF DRAWINGS

STORAGE-GENERAL ARRANGEMENT	SD-39277
FLIP-FLOP STORAGE-BLOCK SCHEMATIC	SD-39278
FLIP-FLOP REGISTER-CIRCUIT SCHEMATIC	SD-39285
FLIP-FLOP REGISTER-ASSEMBLY	D-30872
FLIP-FLOP REGISTER-PANEL ASSEMBLY	E-30900
FLIP-FLOP STORAGE OUTPUT-CIRCUIT SCHEMATIC	SD-39286
FLIP-FLOP STORAGE OUTPUT-ASSEMBLY	D-30879
FLIP-FLOP STORAGE OUTPUT-PANEL ASSEMBLY	E-30976

NOTE: USE LATEST REVISION OF EACH DRAWING

A-3935

6345
Memorandum M-107

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND I RESEARCH AND CLEAN-UP ASSIGNMENTS

To: Jay W. Forrester, H. R. Boyd, S. H. Dodd, L. R. Everett, D. R. Brown, N. Taylor

From: H. Fahnestock

Date: September 30, 1947

At a meeting today between Brown, Fahnestock and Taylor the Whirlwind I assignments made September 3 were reviewed and modified. The jobs assigned September 3 are followed by engineers' names in parenthesis after which modifications are given.

1. GATE TUBE AND AMPLIFIER PLATE LOADS (Hoberg, Sard) - This will be extended to include an investigation of tubes saved in the system by using step up transformers and an evaluation and decision on the relative merits of half sine wave pulses versus square pulses. Brown will specify the program to be carried out by Hoberg, Kerosian and Sard.

2. FLIP-FLOP STABILITY (Horton, J. J. O'Brien) - To continue. Horton's flip-flop test rack to be modified to represent a digit rack receiving restorer pulses from a source for that digit. Evaluation and direction by Brown and Taylor.

3. FLIP-FLOP RISE TIME AND COUPLING (Kerosian) - Deferred by 2 mo PRF.

4. LINE DRIVERS (Ely, Hoberg) - Hoberg will break in Watt on video problems.

5. TEST EQUIPMENT (Ely, Kerosian) - Ely and Maynard working on improved scope and wide band amplifier.

6. BASIC FLIP-FLOP RESEARCH (J. J. O'Brien) - Secondary to other responsibilities of O'Brien's.

7. BLACK-OUT EFFECT (Sard) - To continue.

S. CORRELATION OF TUBE CHARACTERISTICS WITH CIRCUIT PERFORMANCE (Crawford) - Deferred. To be carried on later by Crawford and/or Best.

Other work in progress or to be undertaken shortly:

MULTIPLIER - Testing by Taylor and Sumner with assistance as needed from Kenosian and J. J. O'Brien. Brown and Taylor to discuss extension of 5-digit multiplier control to provide additional functions. Kenosian to supervise and debug step counter.

STORAGE - J. A. O'Brien to review the entire storage picture to be sure it includes latest thinking. Crawford working with Sylvania on flip-flop storage registers and outputs. J. A. O'Brien to extend 32-position switch work.

PULSE TRANSFORMERS - Rowland to understudy Moberg.

INPUT AND OUTPUT - Fahnestock to check necessary electronic circuitry with Everett and Forrester.

ELECTROSTATIC STORAGE - Meeting planned to insure tie in of ES storage with WWI. Brown, Todd, Everett, Fahnestock, J. A. O'Brien, Nolan, Taylor.

NEW GATE TUBE - Brown and Taylor as needed.

H. Fahnestock

HF:has