

**PROJECT
WHIRLWIND**

Contract N5ori60

SUMMARY REPORT NO. 2

VOLUME 6

REPORT R-127

**WHIRLWIND I COMPUTER
BLOCK DIAGRAMS**

VOLUME 2 OF 2 VOLUMES

**SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY**

September 4, 1947

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SPECIAL DEVICES CENTER

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**PROJECT
WHIRLWIND**
(DEVICE 24-X-3)

REPORT R-127
**WHIRLWIND I COMPUTER
BLOCK DIAGRAMS**

VOLUME 2 OF 2 VOLUMES

Submitted to the
SPECIAL DEVICES CENTER
OFFICE OF NAVAL RESEARCH
Under Contract N5ori60

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Cambridge 39, Massachusetts

Project DIC 6345

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FOREWORD

This report is a description of the Whirlwind electronic digital computers under development at the Servomechanisms Laboratory of M. I. T. for the Office of Naval Research. The arithmetic nature and the physical nature of the computers are covered briefly, and the block diagrams for the prototype computer WWI are discussed in some detail.

The report consists of two volumes: Volume 1 contains the text and Volume 2 the drawings.

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31	A-30432	Accumulator
32	A-30685	Shift and Carry
33	A-30684	Shift Left
34	C-37099	Clear and Add
35	C-37100	Add
36	A-30682	Arithmetic Check
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38	C-37102	Subtract
39	C-37103	Multiply and Roundoff
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44	C-37108	Conditional Program
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LIST OF DRAWINGS

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50	B-37058	Master Clock
51	B-37062	Program Counter
52	B-37067	Program Register
53	B-37066	Control Switch
54	C-37077	Operation Matrix I
55	C-37078	Operation Matrix II
56	B-37076	Time Pulse Distributor Control
57	B-37068	Pulse Distributor
58	B-37075	Program Timing Matrix
59	C-37064	Storage Chassis Arrangement
60	B-37057	Flip-flop Storage Section
61	B-37060	Storage Output Section
62	B-37061	Flip-flop Storage Control
63	C-37072	Arithmetic Element
64	B-37056	Section of A-Register
65	C-37063	Accumulator Sections
66	C-37096	Accumulator Sections
67	B-37069	B-Register Sections
68	B-37097	B-Register Sections
69	B-37074	Step Counter
70	B-37065	Check Register
71	A-30874	Program Timing
72	B-37080	Timing for Add
73	B-37081	Timing for Clear and Add
74	B-37082	Timing for Subtract
75	B-37083	Timing for Clear and Subtract
76	B-37084	Timing for Multiply and Roundoff
77	B-37085	Timing for Multiply and Hold Full Product
78	B-37094	Timing for Divide
79	B-37086	Timing for Transfer to Storage
80	B-37088	Timing for Shift Right
81	B-37089	Timing for Shift Left
82	B-37090	Timing for Subprogram
83	B-37091	Timing for Conditional Program
84	B-37092	Timing for Transfer Digits
85	B-37093	Timing for Special Add
86	B-37087	Timing for Store & Display
87	B-37001	Parallel Digit Computer Codes

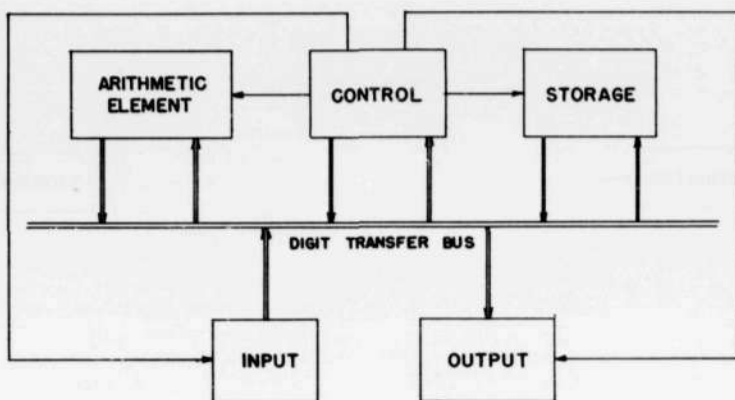


Figure 1
GENERAL BLOCK DIAGRAM

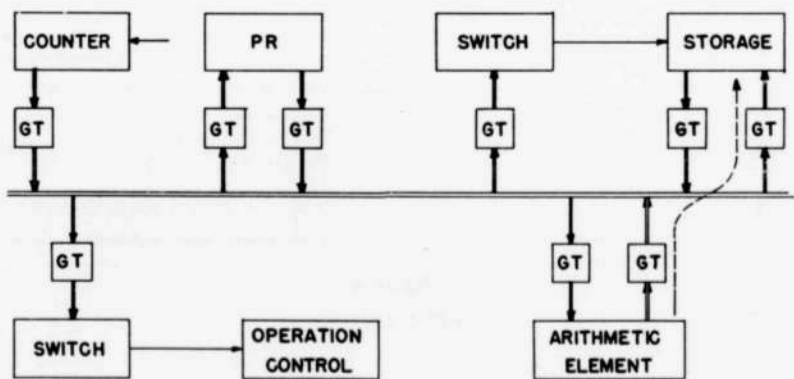


Figure 2
STORE RESULT

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ORIGIN OF ORDERS



Figure 3
ORIGIN OF ORDERS

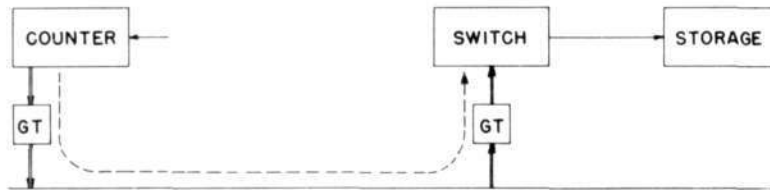


Figure 4
SETUP ORDER

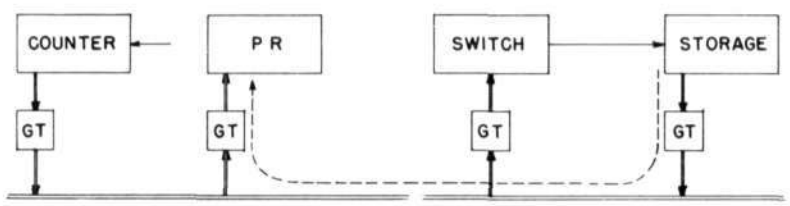


Figure 5
READ OUT ORDER

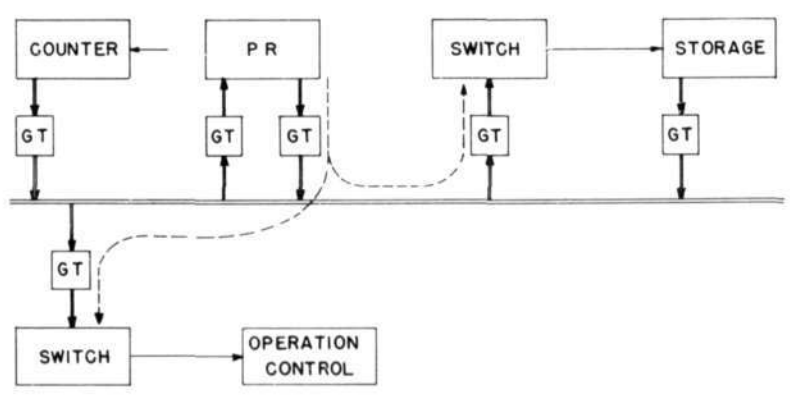


Figure 6
SETUP OPERATION

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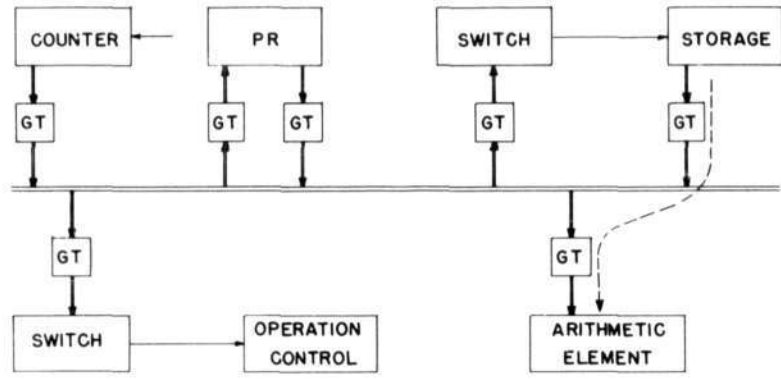


Figure 7
PERFORM OPERATION

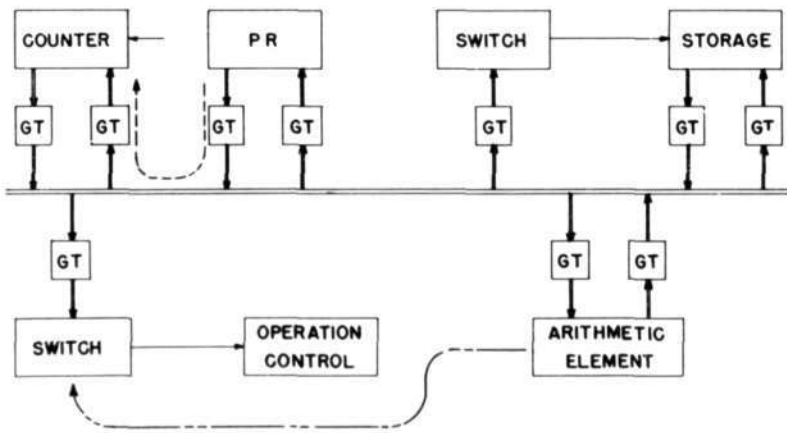


Figure 8
SUBPROGRAM

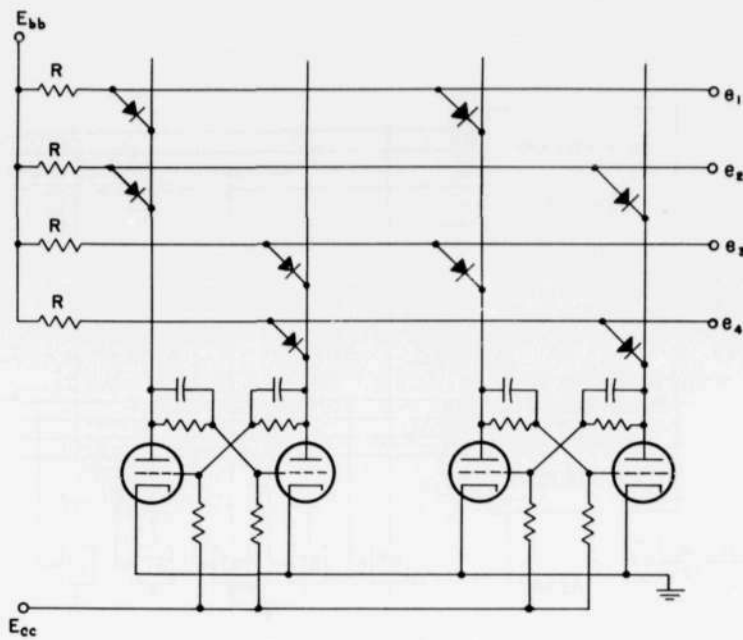


Figure 9
ELECTRONIC SWITCH

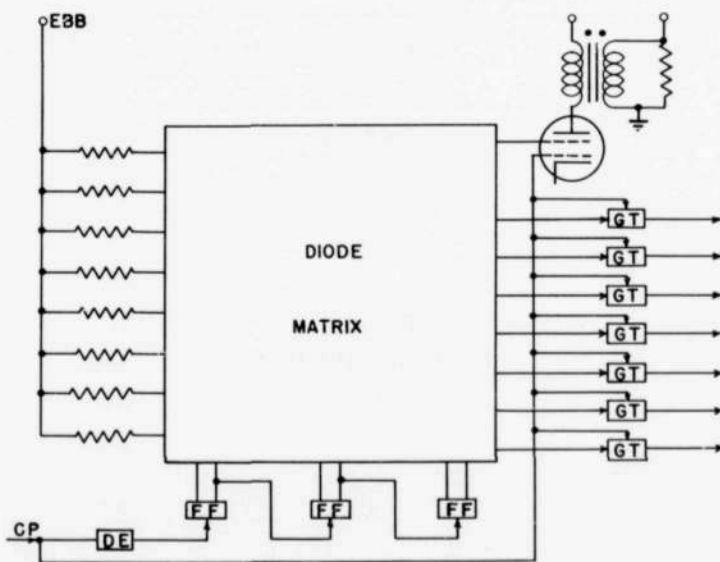


Figure 10
TIME PULSE DISTRIBUTOR

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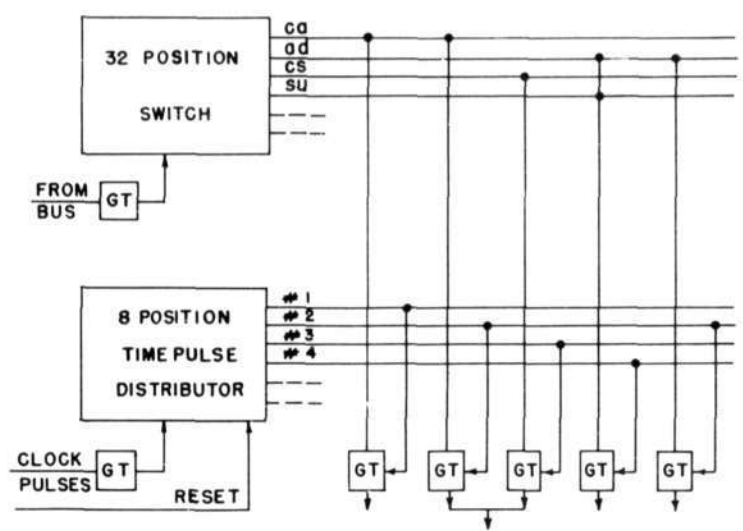


Figure 11
CONTROL

$$\begin{array}{r}
 3546 \\
 1371 \\
 \hline
 4817 \\
 +1 \\
 \hline
 4917
 \end{array}$$

Figure 12
DECIMAL ADDITION

```
  11011010
  10110110
  -----
  1 1 1
  01101100
  -----
  1 1
  101001000
  -----
  1 1
  100000000
  -----
  1 1
  110010000
```

Figure 13
BINARY ADDITION

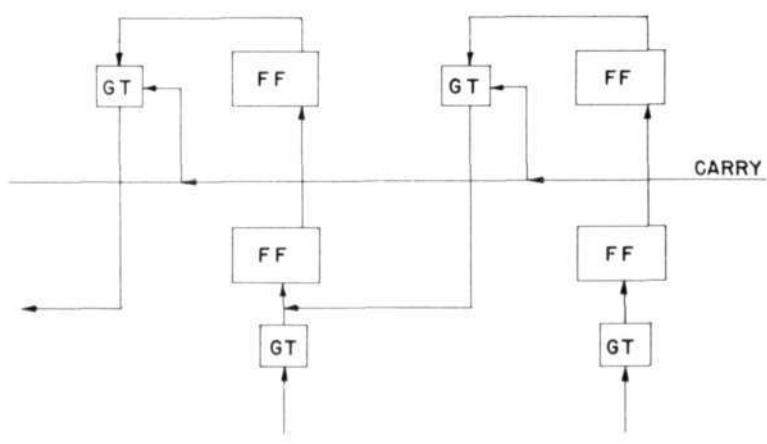


Figure 14
A BINARY ADDER

60mbs: rine

	DECIMAL	BINARY
POSITIVE NUMBER	223	11011111
NEGATIVE "	- 223	- 11011111
10'S COMPLEMENT	1777	100100001
9'S "	1776	100100000

Figure 15
NEGATIVE NUMBERS

BINARY		DECIMAL
+010110110	- N_1	- 182
-011010010	-- N_2	-- 210
		- 28
010110110	- N_1	
100101101	- $2^n - N_2 - 1$	
111100011	- $2^n - (N_2 - N_1) - 1$	
-000011100	- $N_1 - N_2$	- - 28
010110110	- N_1	- 182
-010010010	- N_2	-- 146
		+ 36
010110110	- N_1	
101101101	- $2^n - N_2 - 1$	
100010001	- $N_1 - N_2 + 2^n - 1$	
END AROUND CARRY		
+1		
000100100	- $N_1 - N_2$	- + 36

Figure 16
SUBTRACTION USING 9'S COMPLEMENTS

3 5 6	MULTIPLICAND
<u>6 2 7</u>	MULTIPLIER
4 2	
3 5	
<u>2 1</u>	
2 4 9 2	PARTIAL PRODUCT
1 2	
1 0	
<u>6</u>	
9 6 1 2	PARTIAL PRODUCT
3 6	
3 0	
<u>1 8</u>	
2 2 3 2 1 2	PRODUCT

Figure 17
DECIMAL MULTIPLICATION

REPRESENTS POWERS OF 2

MULTIPLICATION TABLE:

1 x 1 = 1
1 x 0 = 0
0 x 0 = 0

ADDITION:

1 + 1 = 10
1 + 0 = 1
0 + 0 = 0

BINARY COLUMNS $\approx 3\frac{1}{3} \times$ DECIMAL COLUMNS
ONLY DIGITS 1 AND 0 REQUIRED IN EQUIPMENT

Figure 18
BINARY NOTATION

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10110	MULTIPLICAND	22
10011	MULTIPLIER	19
10110		198
10110		22
1000010	PARTIAL PRODUCT	418
00000		
1000010	PARTIAL PRODUCT	
00000		
01000010	PARTIAL PRODUCT	
10110		
110100010	= 418 PRODUCT	

Figure-19
BINARY MULTIPLICATION

STEP 1	10110	MULTIPLICAND	22
	10011	MULTIPLIER	19
	10110	PARTIAL PRODUCT	198
STEP 2	10110	MULTIPLICAND	
	1001	SHIFTED MULTIPLIER	
	10110	SHIFTED PARTIAL PRODUCT	
	10110		
	1000010	PARTIAL PRODUCT	
STEP 3	10110	MULTIPLICAND	
	100	SHIFTED MULTIPLIER	
	1000010	SHIFTED PARTIAL PRODUCT	
	00000		
	1000010	PARTIAL PRODUCT	
STEP 4	10110	MULTIPLICAND	
	10	SHIFTED MULTIPLIER	
	1000010	SHIFTED PARTIAL PRODUCT	
	00000		
	01000010	PARTIAL PRODUCT	
STEP 5	10110	MULTIPLICAND	
	1	SHIFTED MULTIPLIER	
	01000010	SHIFTED PARTIAL PRODUCT	
	10110		
	110100010	PRODUCT	

Figure 20
MODIFIED BINARY MULTIPLICATION

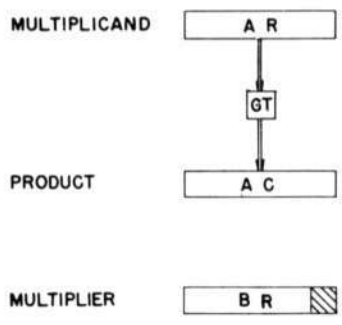


Figure 21
MULTIPLICATION I

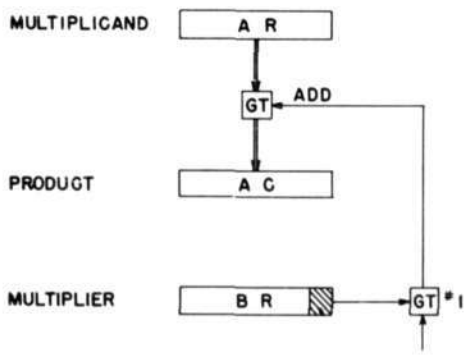


Figure 22
MULTIPLICATION II

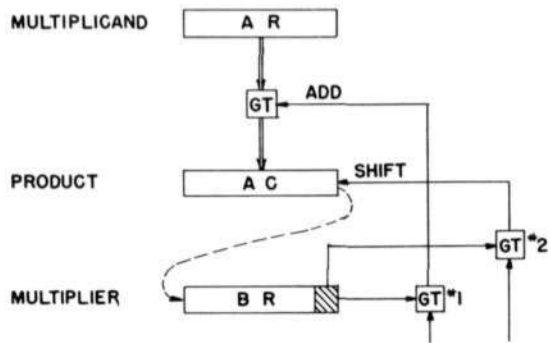


Figure 23
MULTIPLICATION III

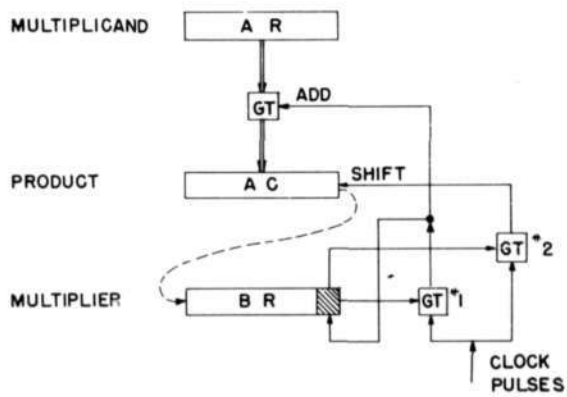


Figure 24
MULTIPLICATION IV

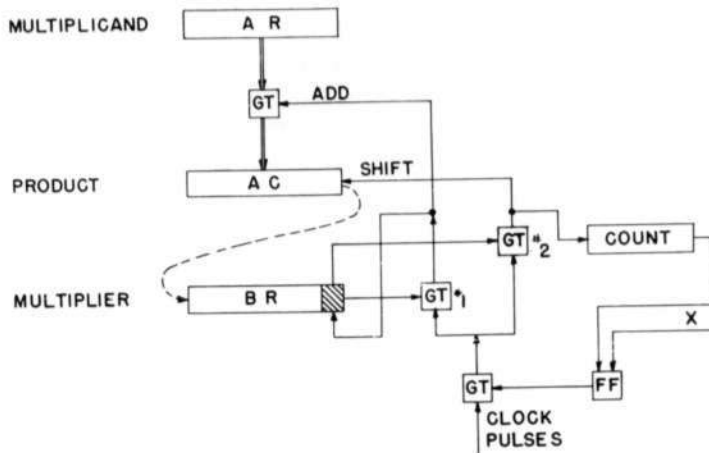


Figure 25
MULTIPLICATION V

DECIMAL	1734	6148
		5
	1735	1
	173	46148
		5
	173	9

BINARY	11010	1010
		1
	11011	
	1101	01010
		1
	1101	1

Figure 26
ROUNDING OFF

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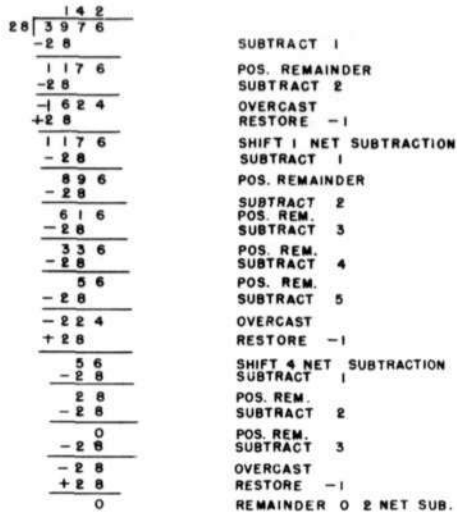


Figure 27
 DECIMAL DIVISION

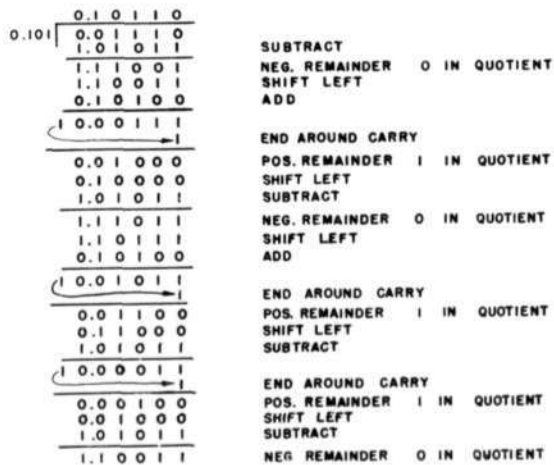


Figure 28
 BINARY DIVISION

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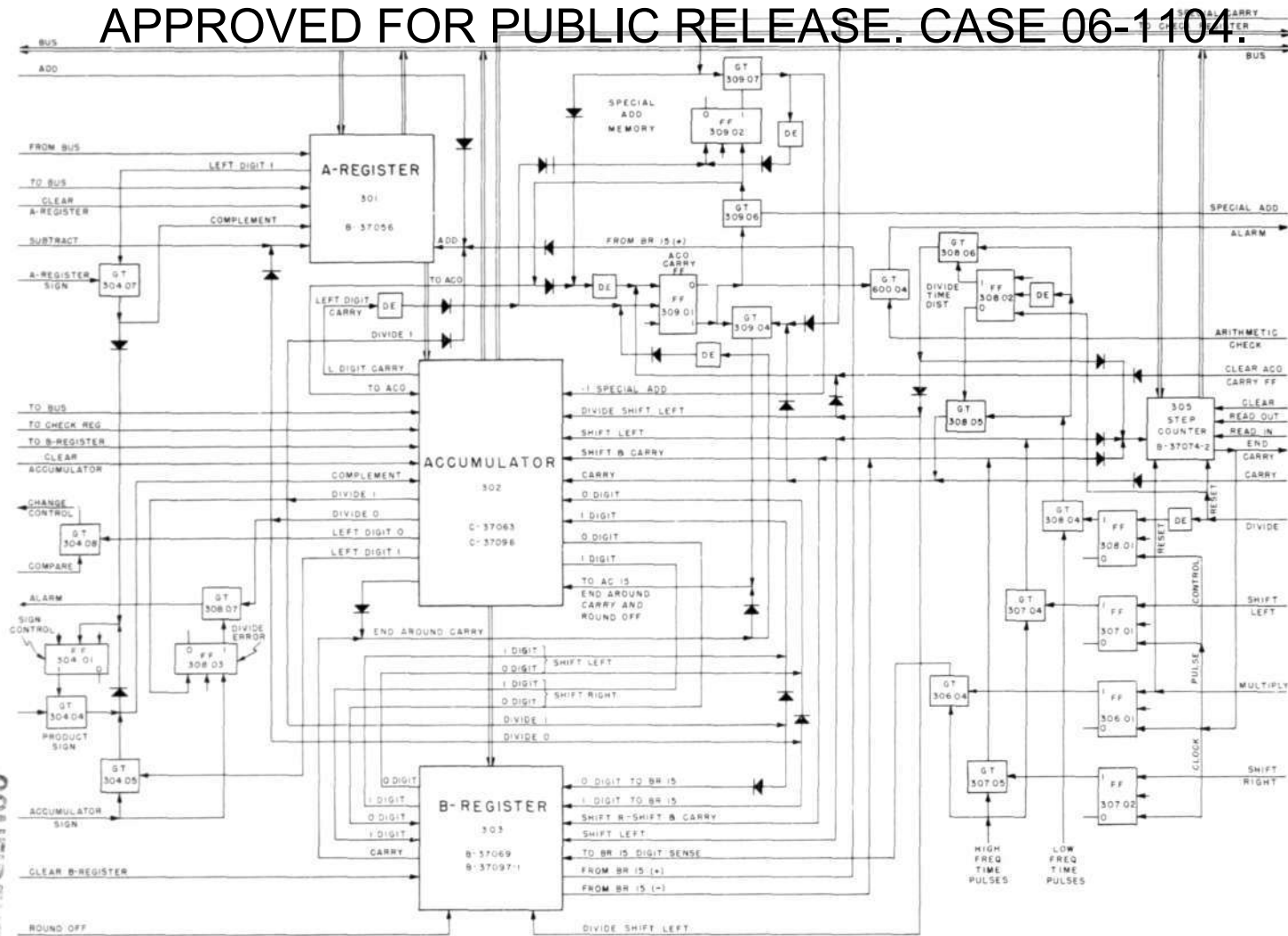


Figure 29
ARITHMETIC ELEMENT

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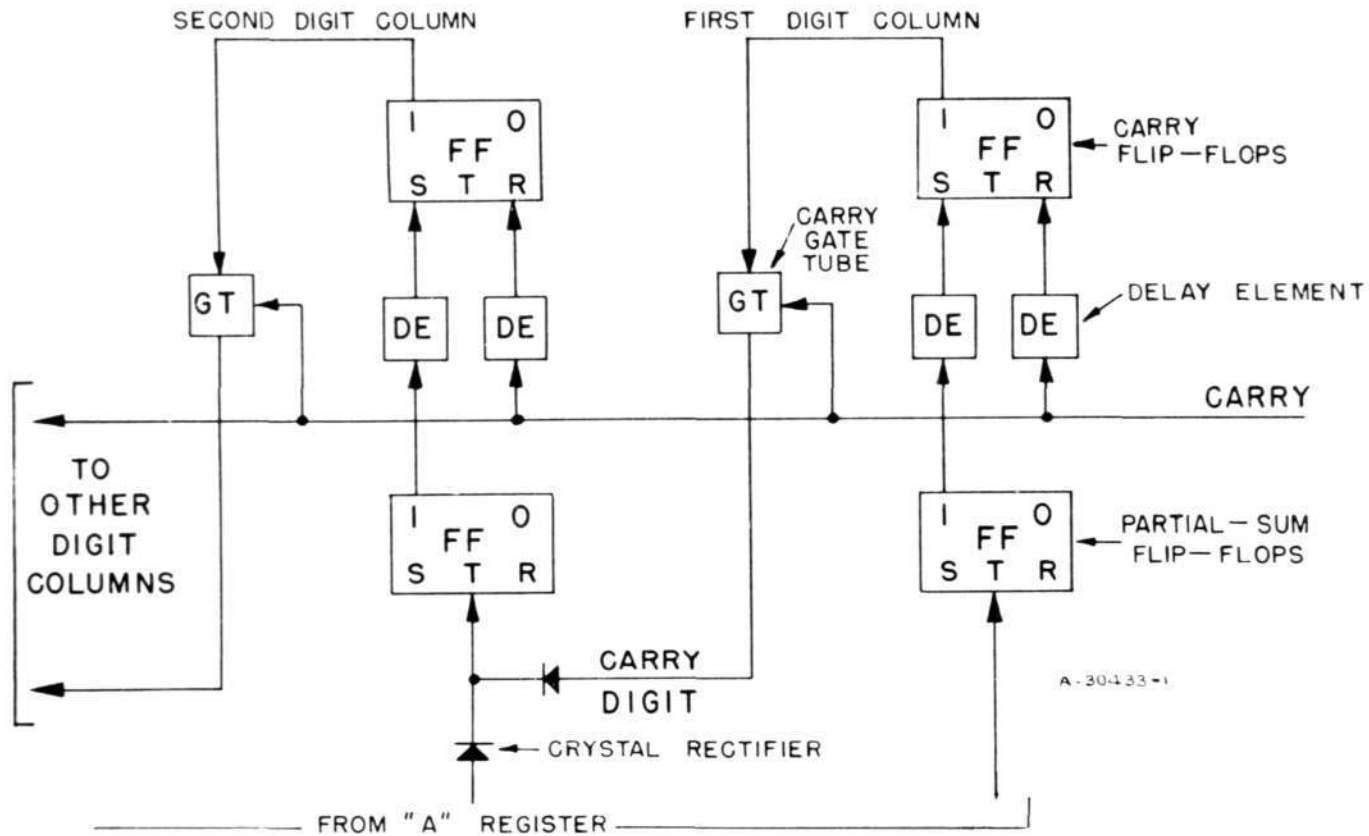


Figure 30
ACCUMULATOR

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

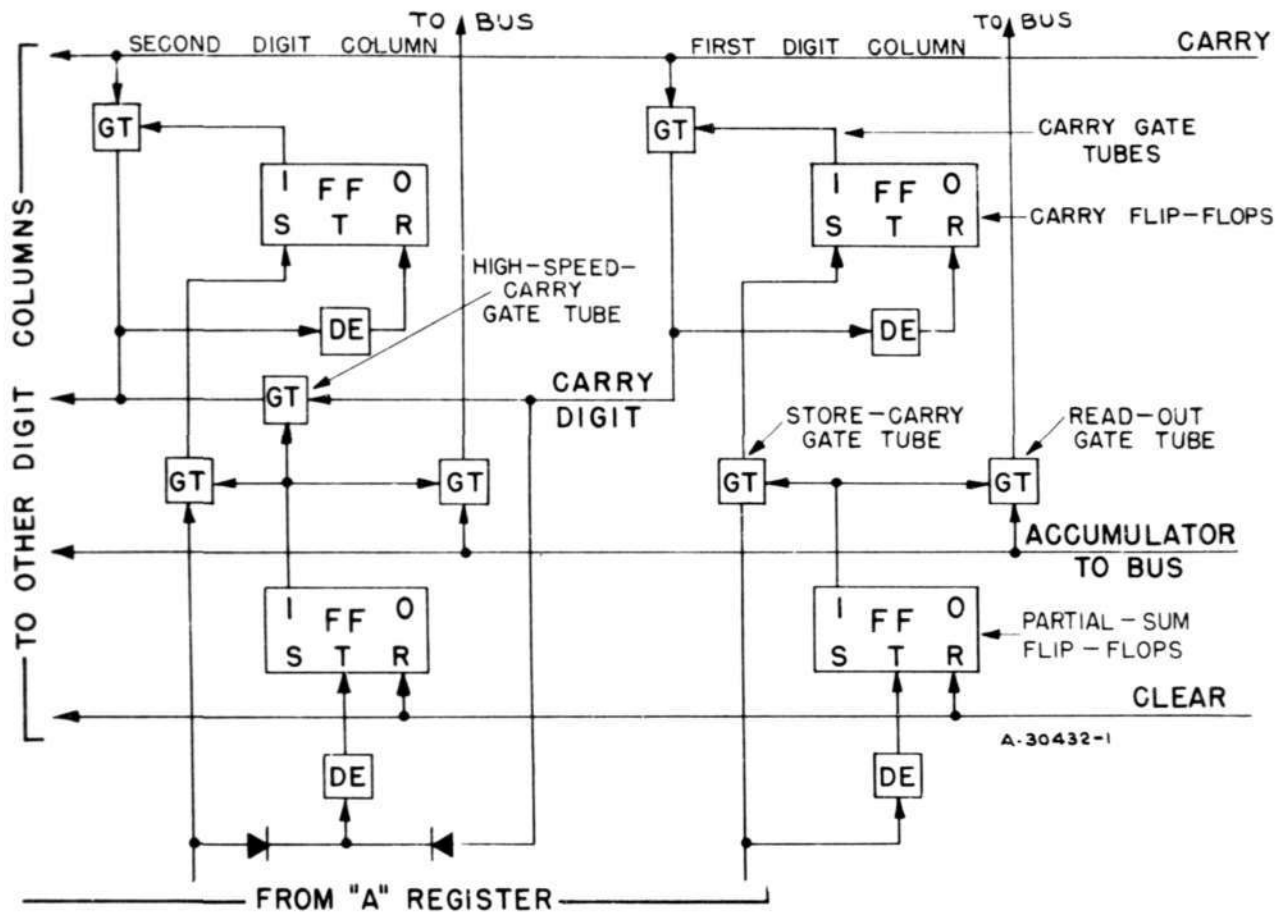


Figure 31
ACCUMULATOR

CONFIDENTIAL

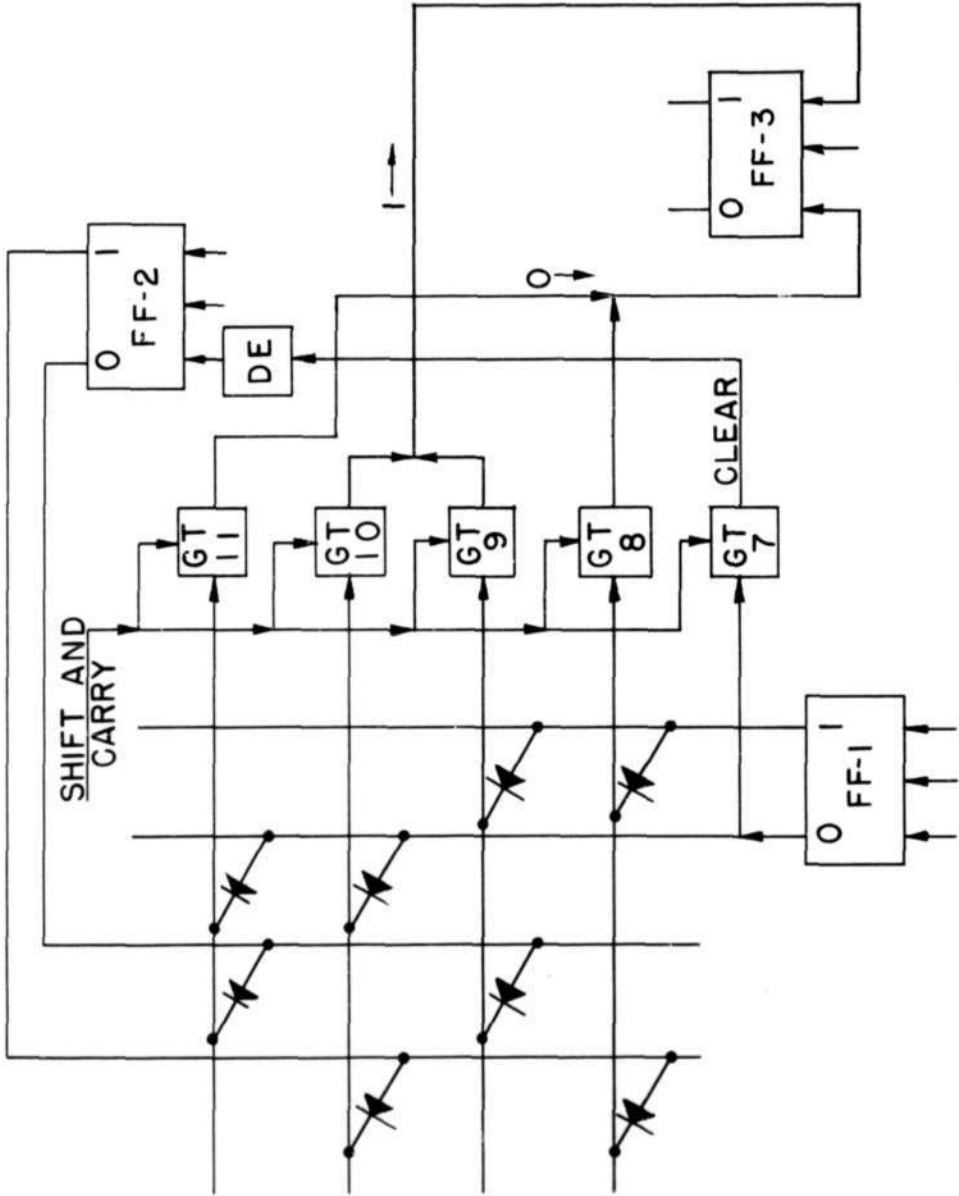


Figure 32
SHIFT AND CARRY

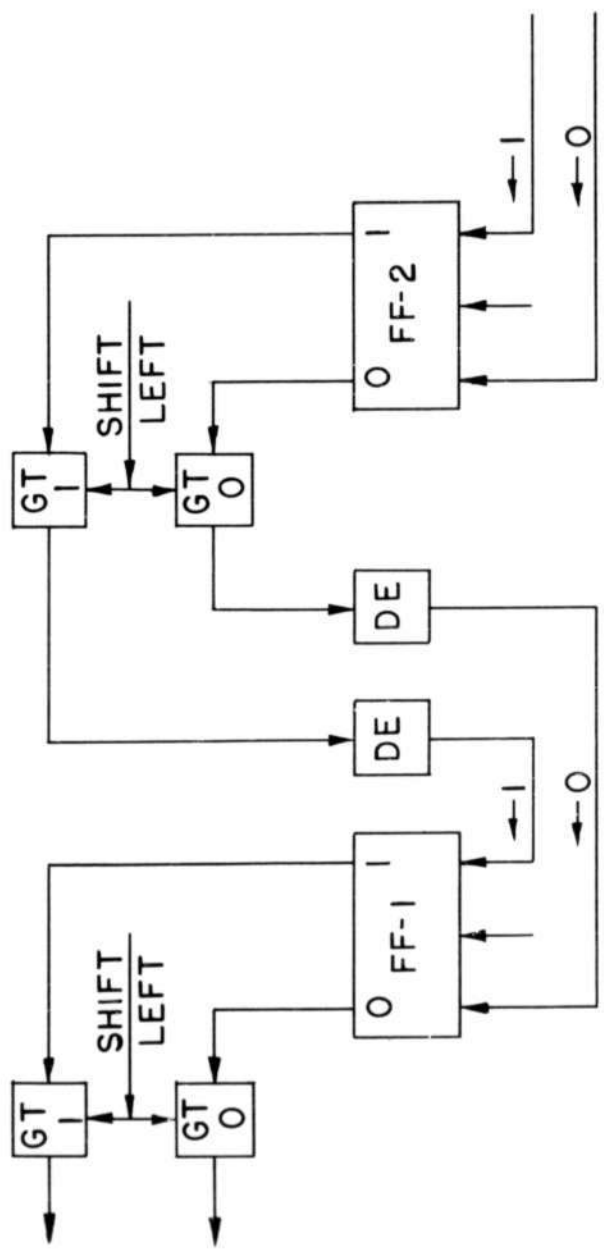


Figure 33
SHIFT LEFT

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APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

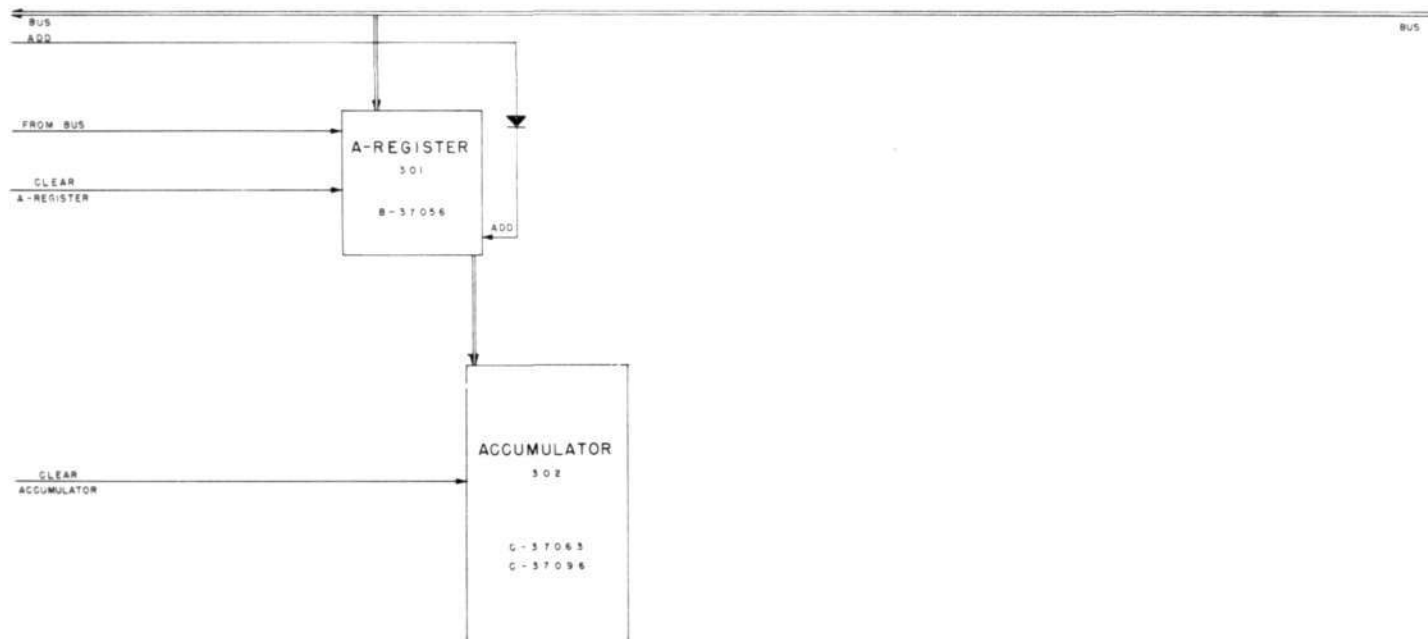


Figure 34
CLEAR AND ADD

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

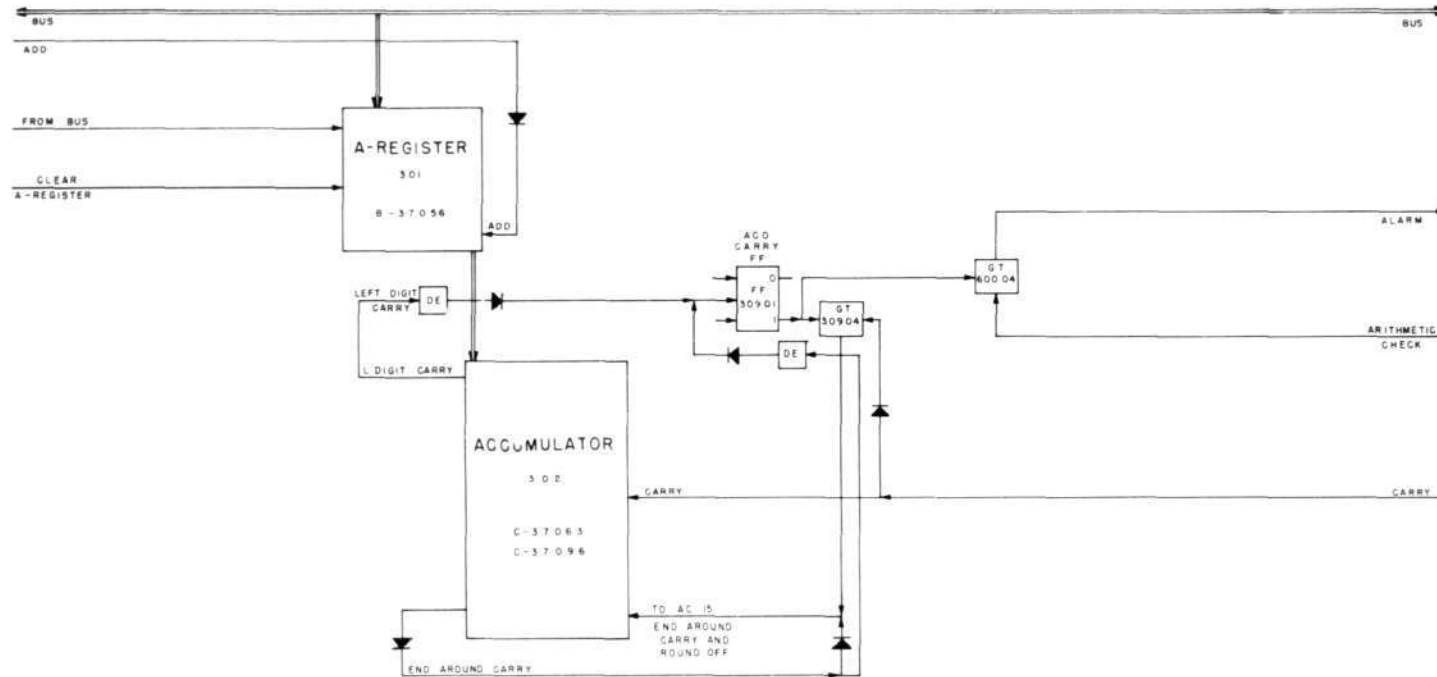


Figure 35
ADD

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

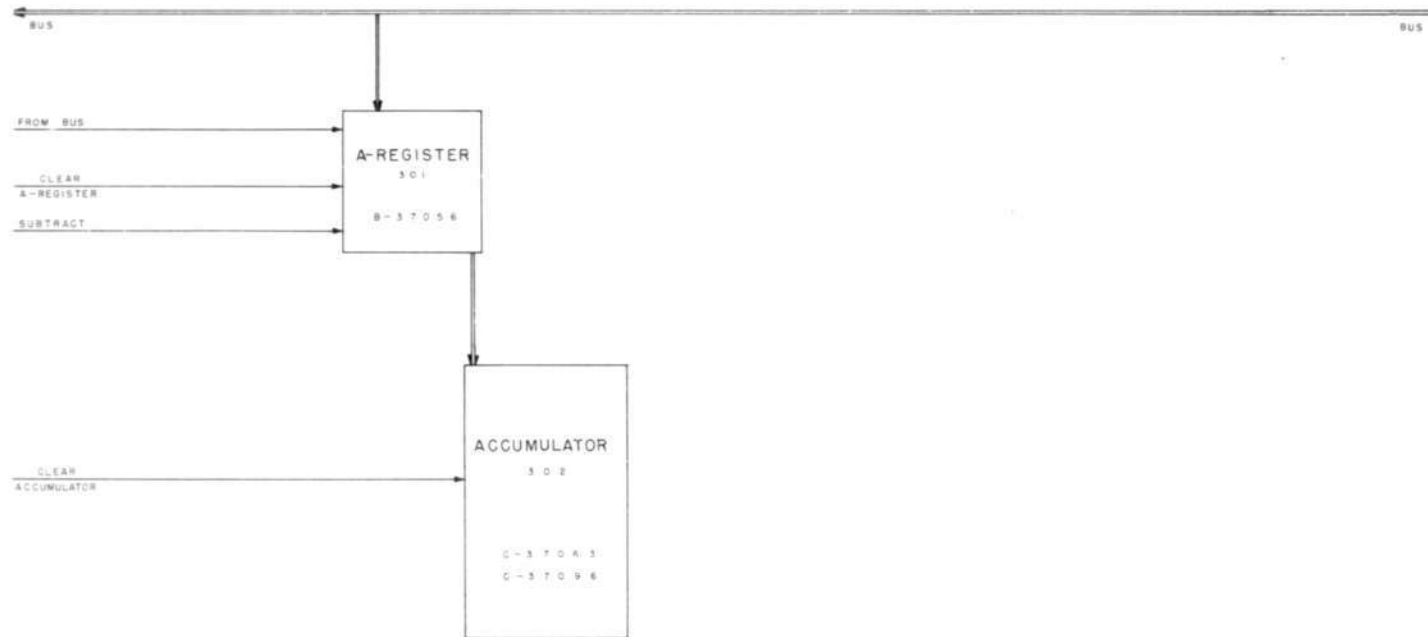


Figure 37
CLEAR AND SUBTRACT

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APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

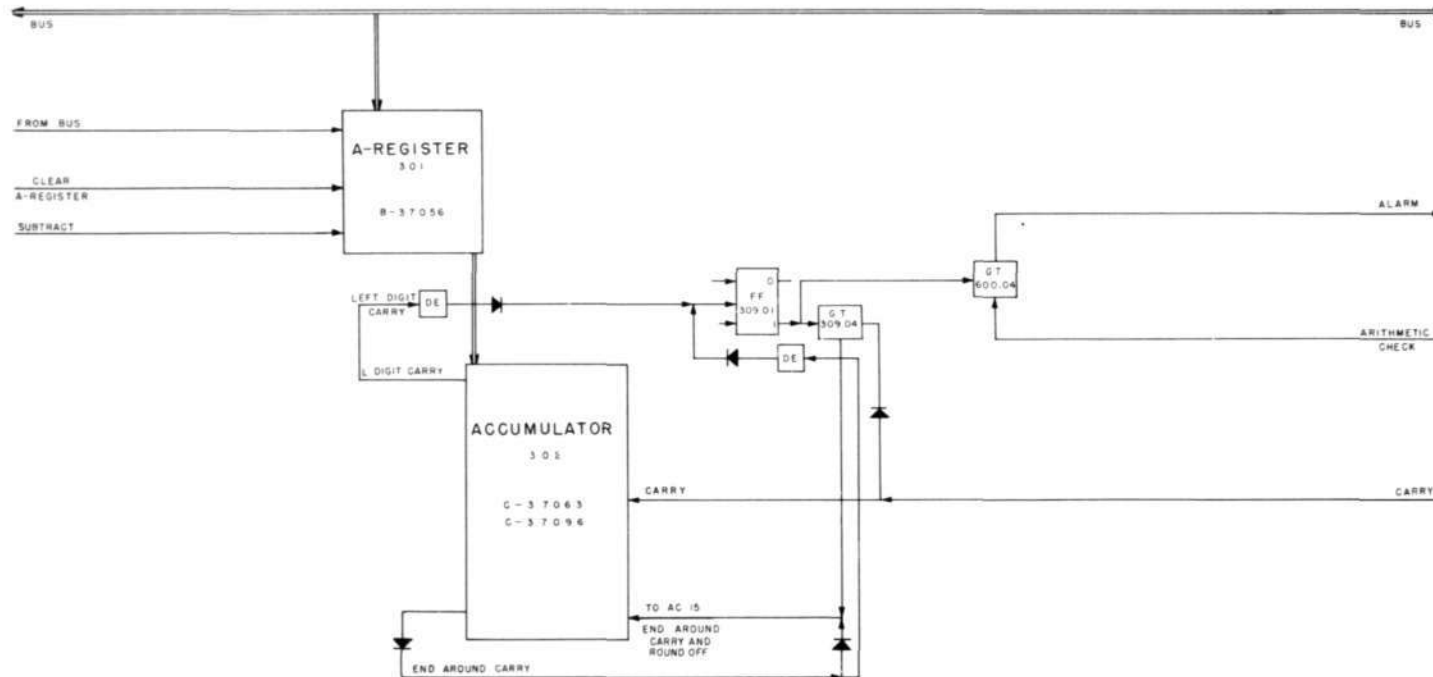


Figure 38
SUBTRACT

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

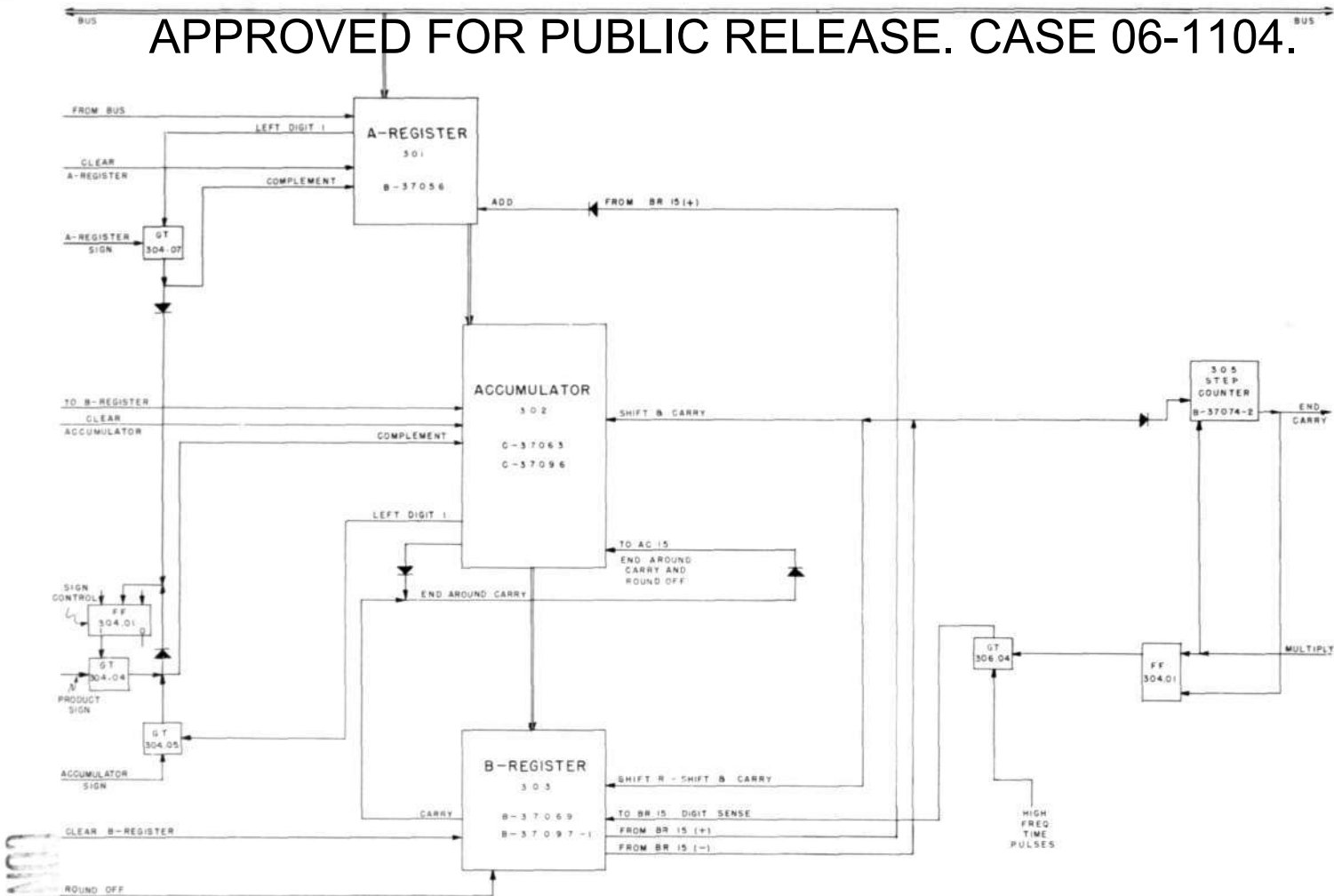


Figure 39

MULTIPLY AND RONDOFF

MULTIPLY AND HOLD FULL PRODUCT

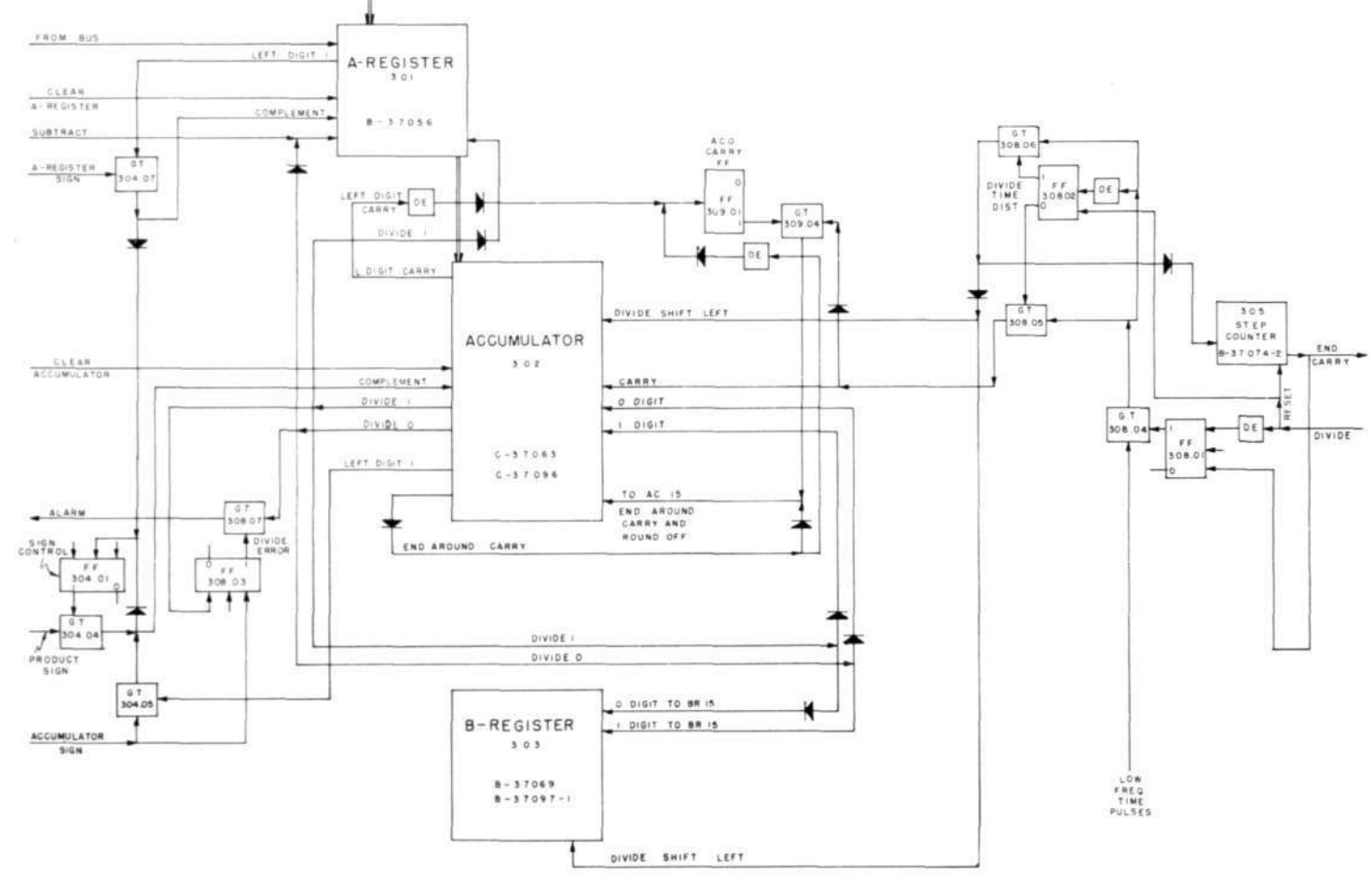


Figure 40
DIVIDE

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

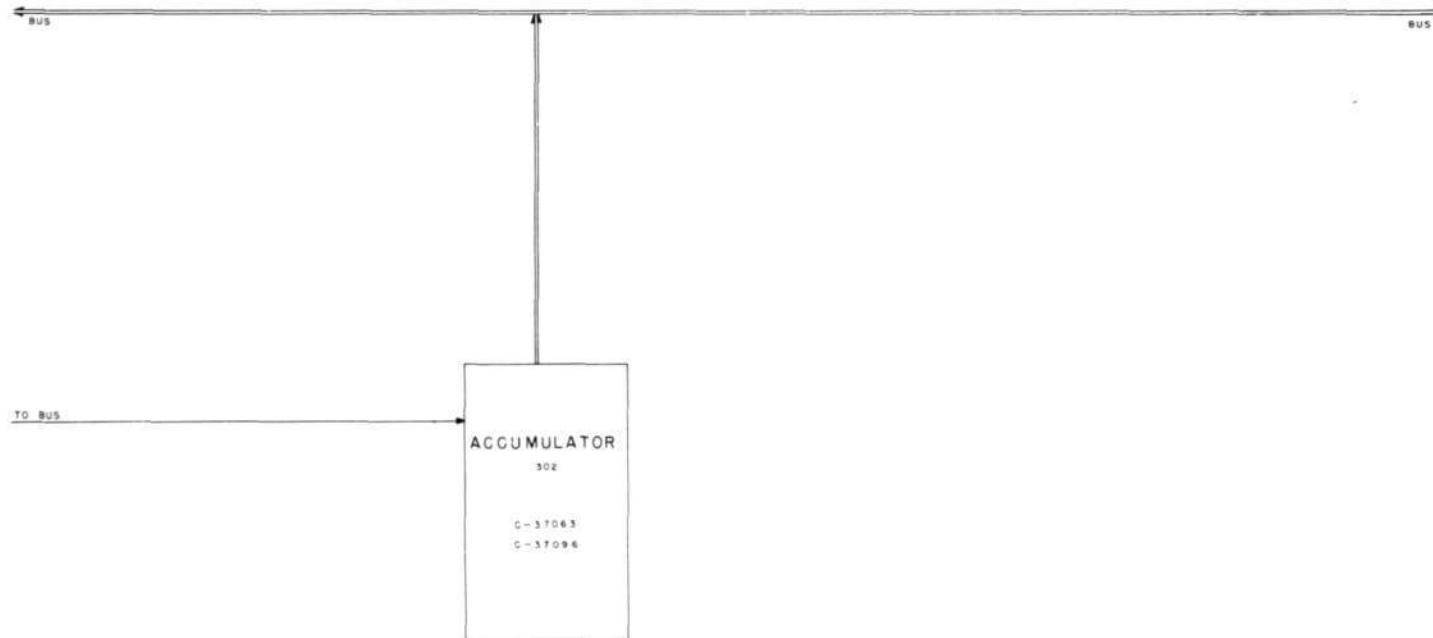


Figure 41
TRANSFER TO STORAGE
TRANSFER DIGITS
STORE AND DISPLAY

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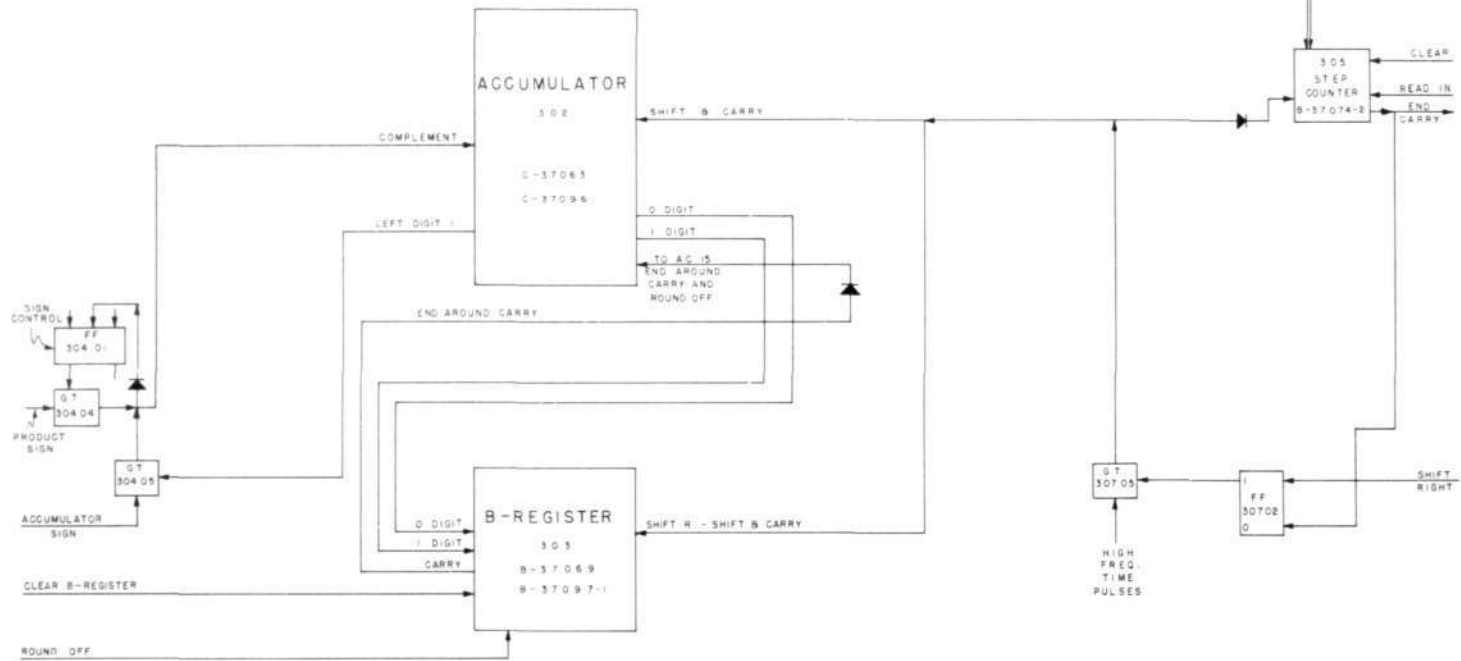


Figure 42
SHIFT RIGHT

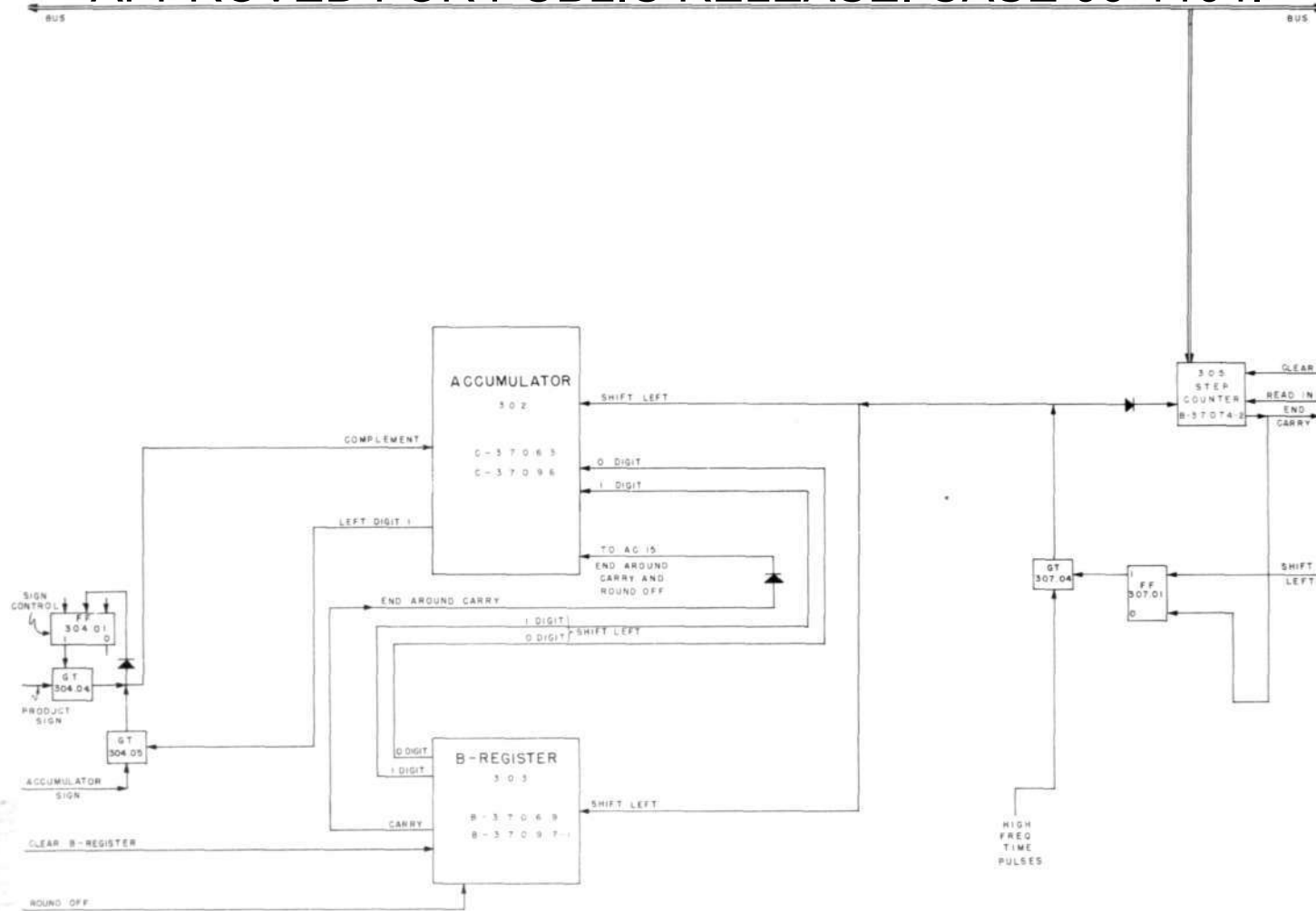


Figure 43
SHIFT LEFT

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APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

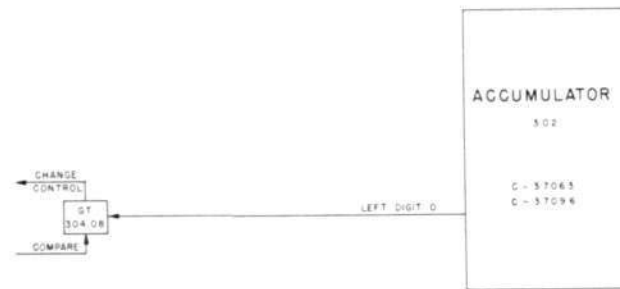


Figure 44
CONDITIONAL PROGRAM

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

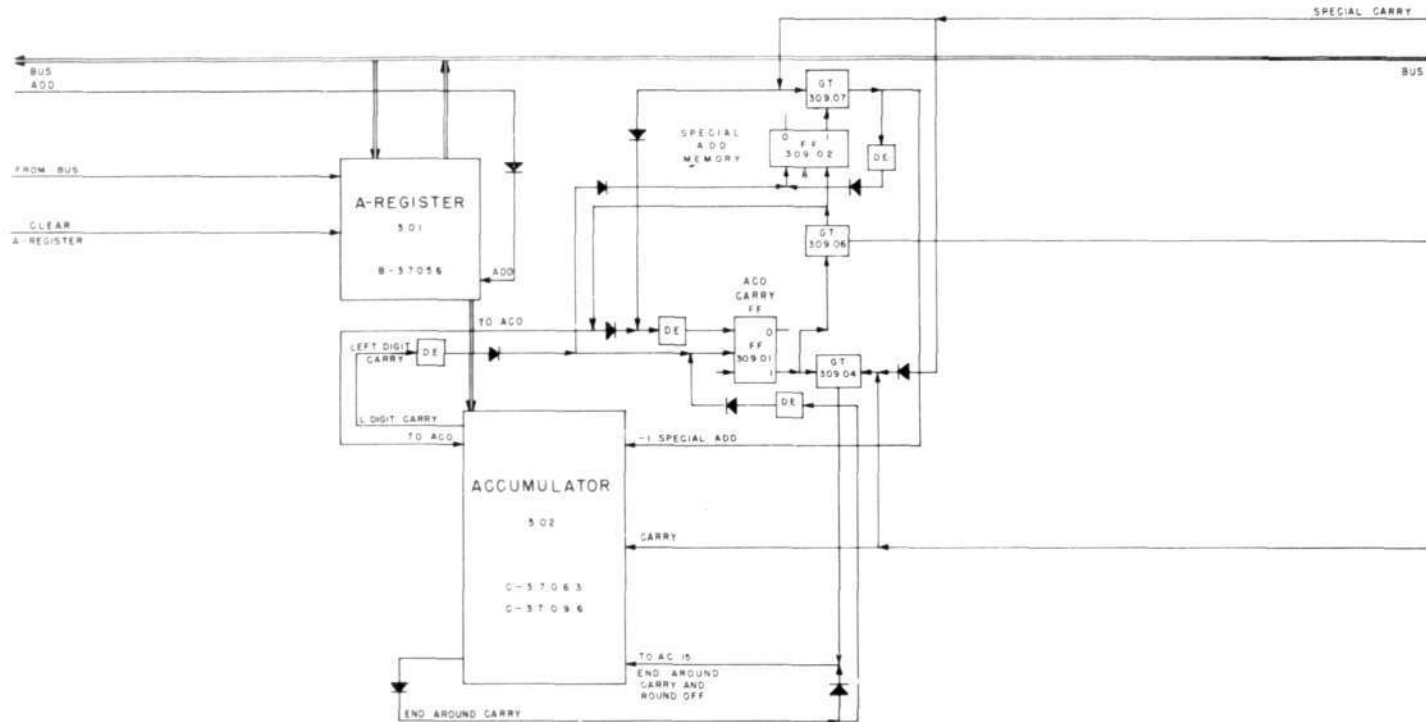


Figure 45
SPECIAL ADD

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

<u>ARITHMETIC ELEMENT CONTROL</u>		<u>PROGRAM COUNTER CONTROL</u>		<u>PROGRAM STORAGE CONTROL</u>	
1. Bus to A-Register	GT 301.01	1. In from Bus	GT 102.01	1. Bus to Storage Switch	GT 201.01
2. A-Register to Bus	GT 301.02	2. Out to Bus	GT 102.02	2. Storage Switch to Bus	GT 201.02
3. Subtract: A-Register to Accum.	GT 301.04	3. Out to Check Register	GT 102.03	3. Storage Readout	GT 203.02
4. Add: A-Register to Accumulator	GT 301.05	4. Add Pulse		4. Storage Switch Clear	
5. Accumulator to Bus	GT 302.02	5. Clear		5. Storage to Check Register	GT 203.03
6. Accumulator to Check Register	GT 302.03				
7. Accumulator to B-Register	GT 302.04				
8. Carry	GT 302.20				
9. Roundoff	GT 303.08				
10. Product Sign	GT 304.04				
11. Accumulator Sign	GT 304.05				
12. A-Register Sign	GT 304.07				
13. Compare	GT 304.08				
14. Multiply	FF 306.01				
15. Shift Left	FF 307.01				
16. Shift Right	FF 307.02				
17. Divide	FF 308.01				
18. Special Add	GT 309.06				
19. Arithmetic Check	GT 600.04				
20. Clear Accumulator					
21. Clear B-Register					
22. Special Carry					

<u>PROGRAM REGISTER CONTROL</u>		<u>OPERATION STORAGE CONTROL</u>	
1. In from Bus	GT 103.01	1. In from Bus	GT 203.01
2. Out to Bus	GT 103.02	2. Storage Readout	GT 203.02
3. Clear		3. Out to Check Register	GT 203.03
		4. Storage Clear	

<u>CONTROL SWITCH CONTROL</u>		<u>STEP COUNTER CONTROL</u>	
1. In from Bus	GT 104.01	1. In from Bus	GT 305.01
2. Out to Bus	GT 104.02	2. Out to Bus	GT 305.02
3. Clear		3. Clear	

NOTE: See Figure 46

Figure 47
CONTROL FUNCTIONS

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

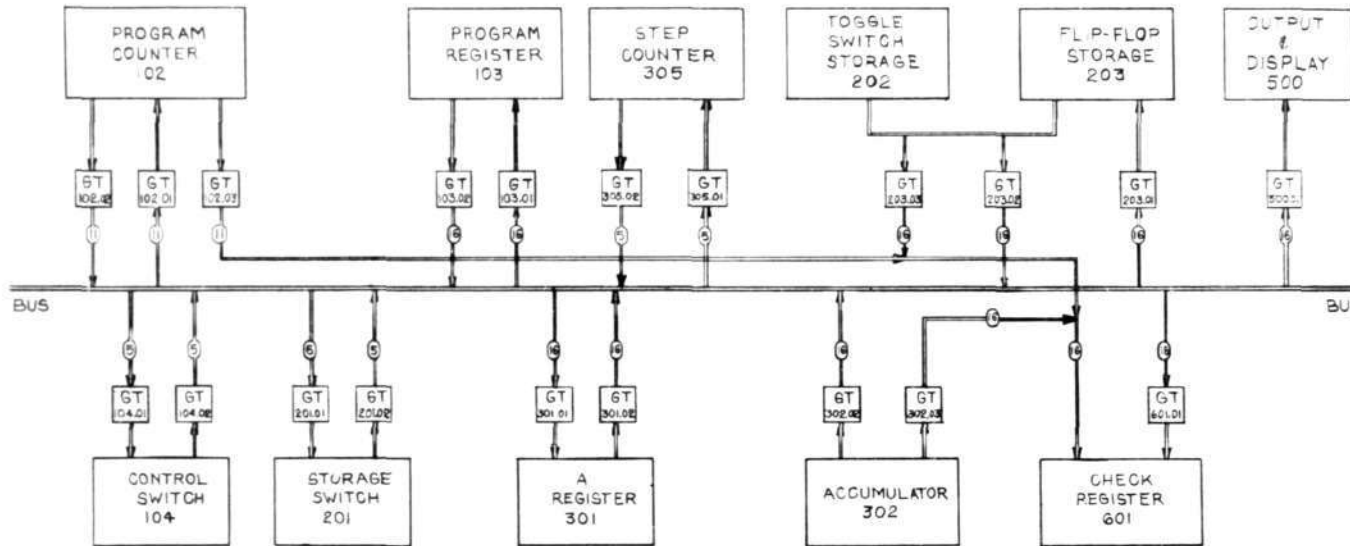


Figure 48
BUS CONNECTIONS

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

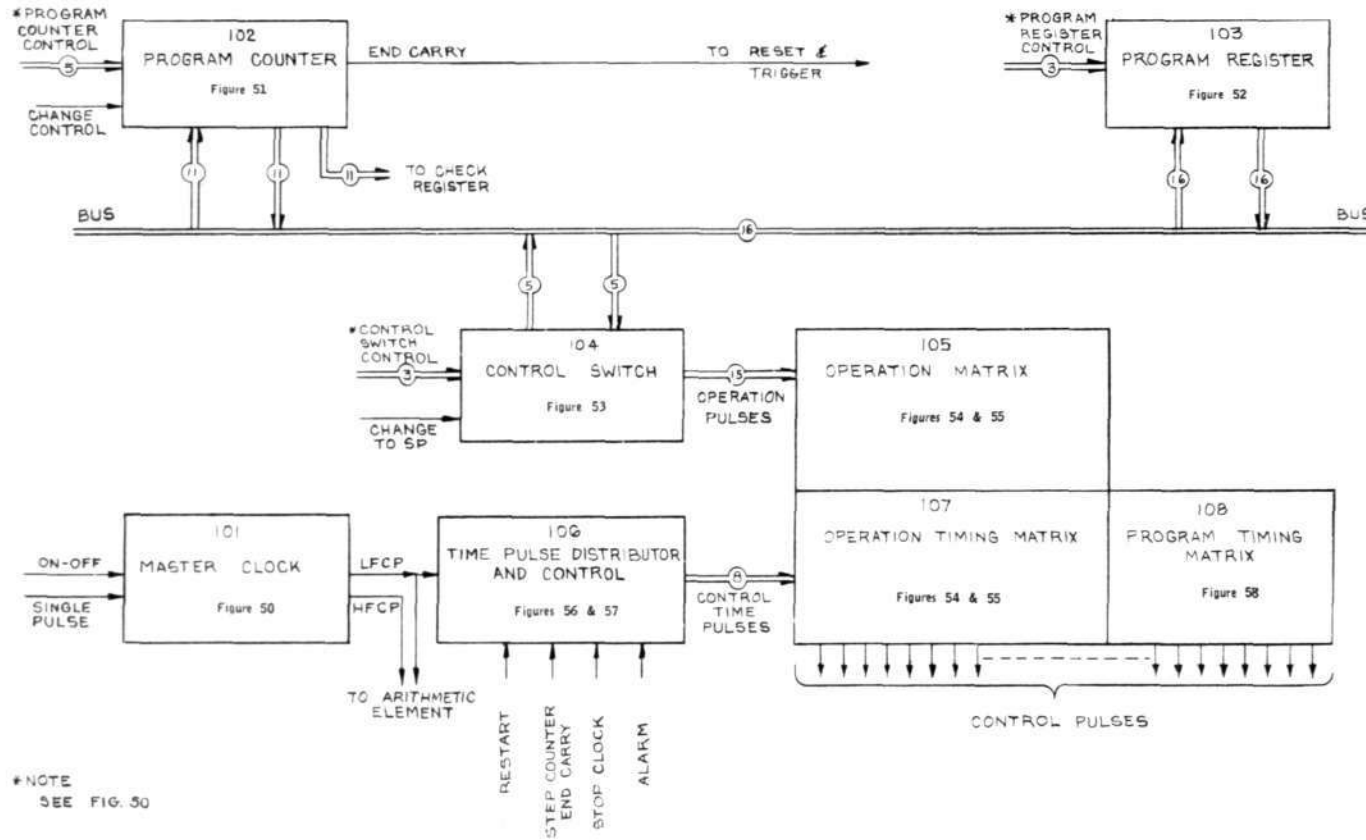


Figure 49
CONTROL

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APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

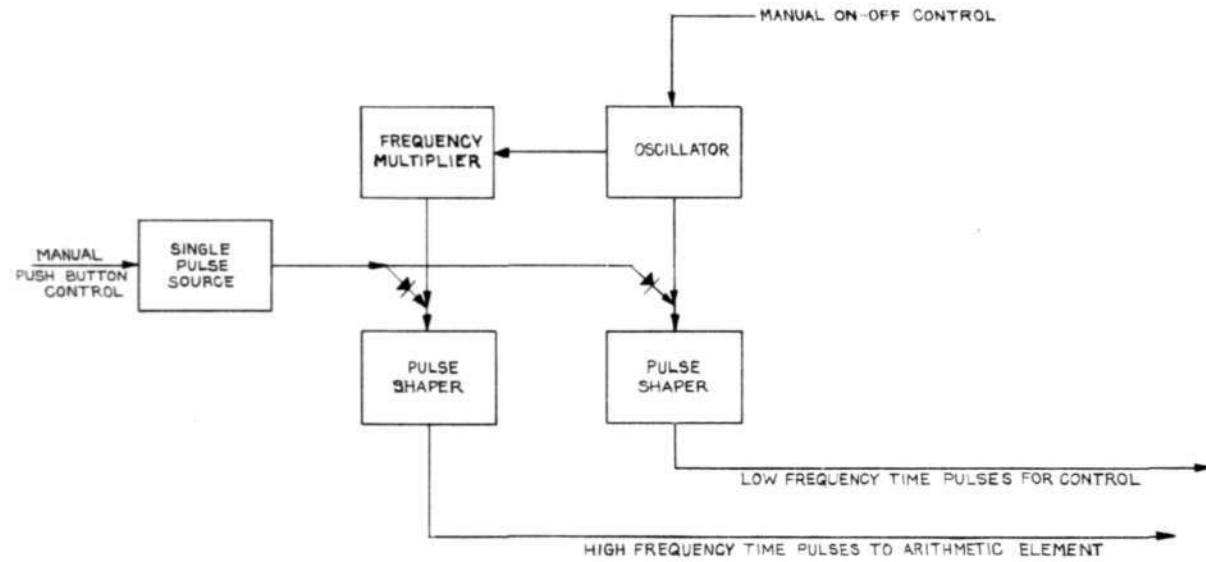


Figure 50
MASTER CLOCK

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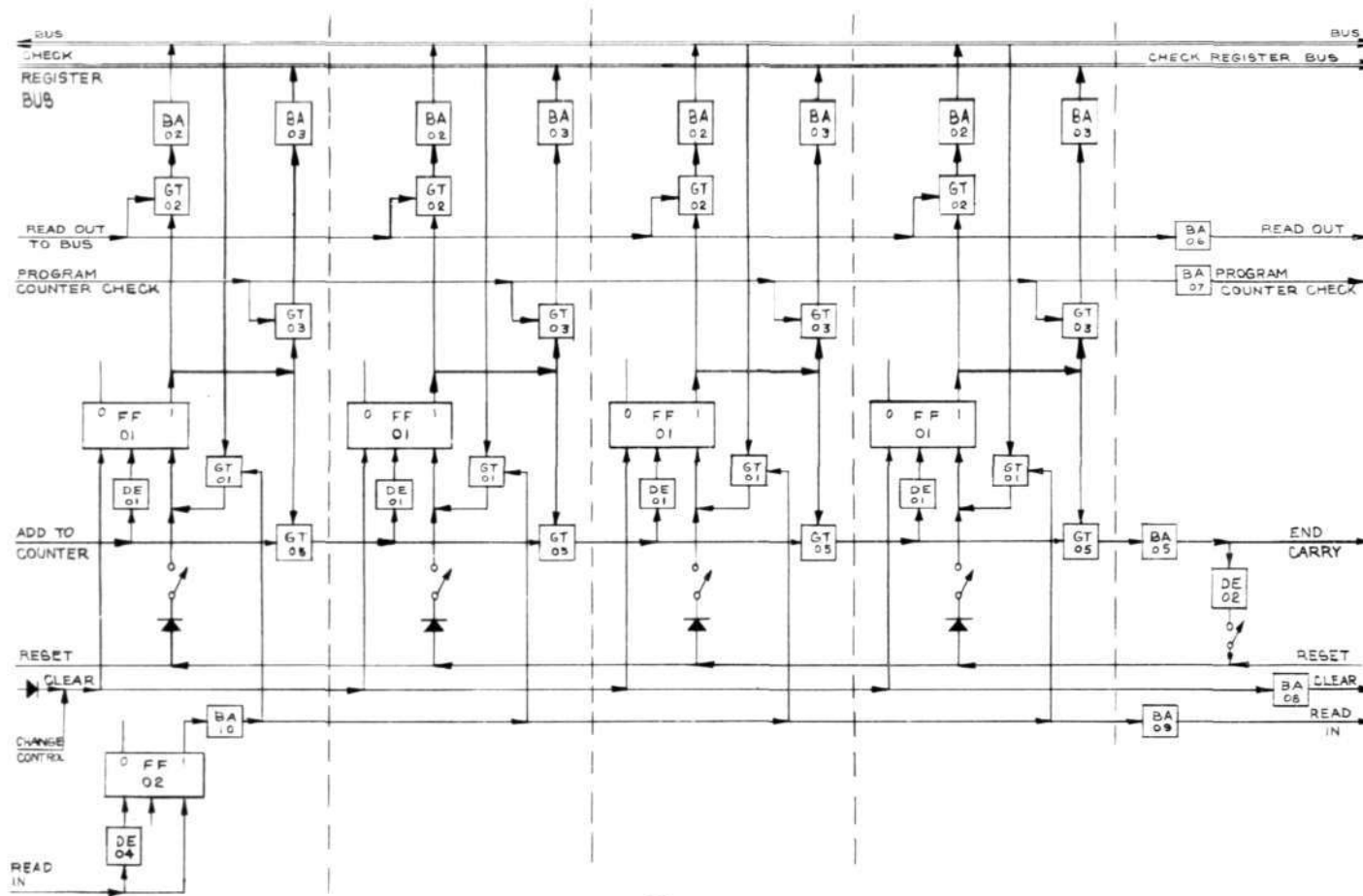


Figure 51
PROGRAM COUNTER

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APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

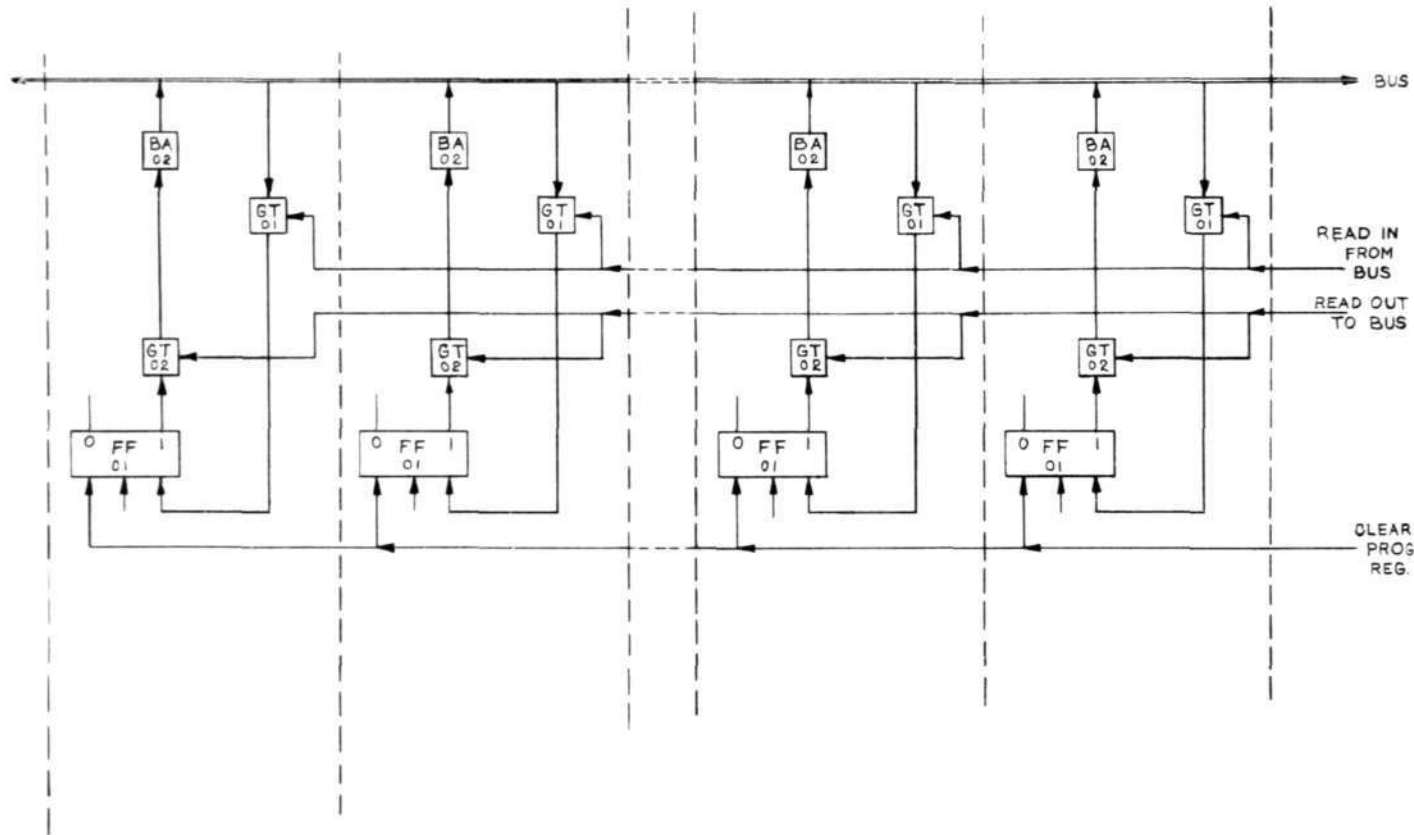


Figure 52
PROGRAM REGISTER

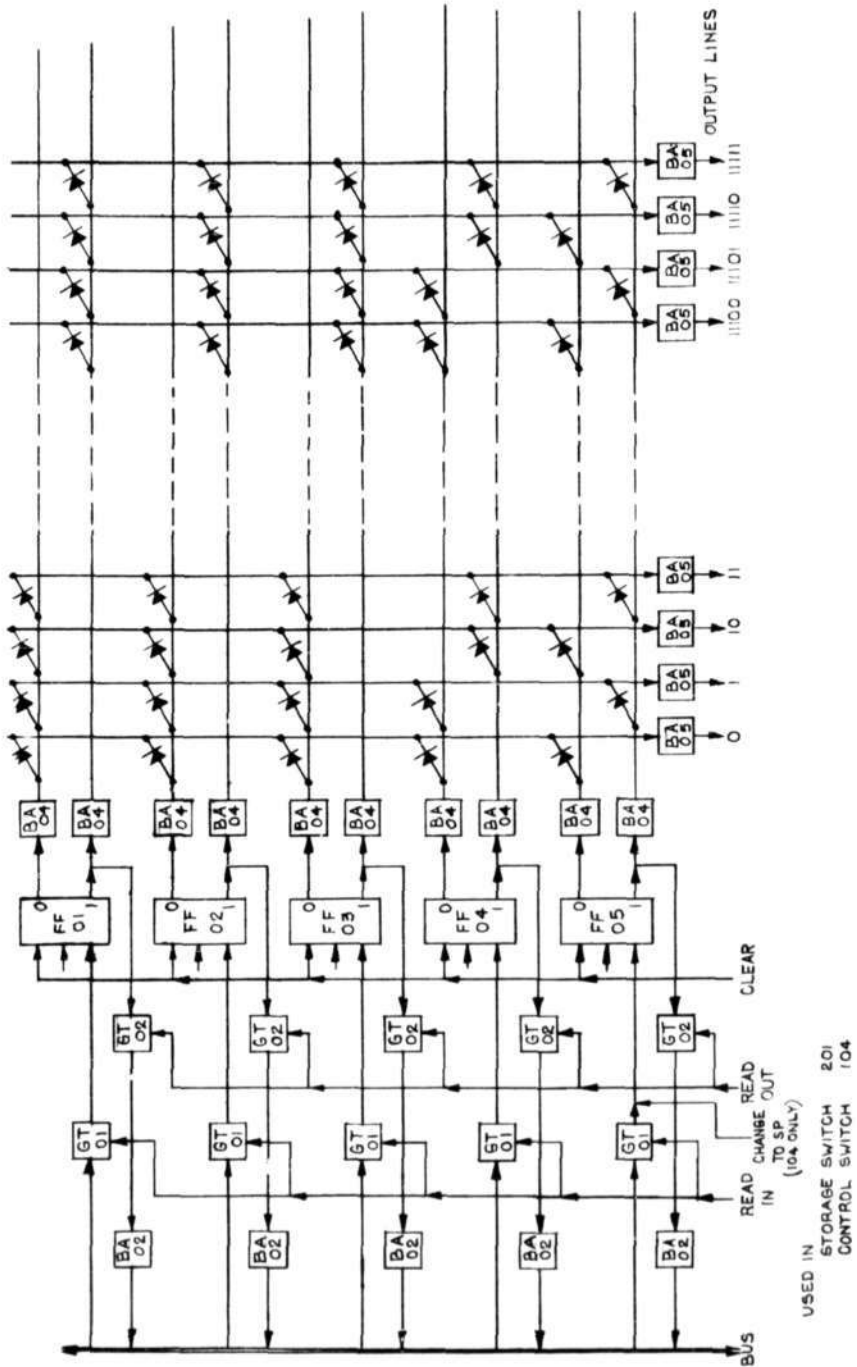


Figure 53
CONTROL SWITCH

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FROM PART I
Doc. 637577

OT 301.01
OT 301.02
OT 301.04
OT 301.05
OT 302.02
OT 302.03
OT 302.04
OT 302.20
OT 303.08
OT 304.04
OT 304.05
OT 304.07
OT 304.08
FF 306.01
FF 307.01
FF 307.02
FF 308.01
OT 309.06
OT 309.06
OT 309.06
OT 309.06

- Bus to A-Register
- A-Register to Bus
- Subtract: A-Register to Accumulator
- Add: A-Register to Accumulator
- Accumulator to Bus
- Accumulator to Check Register
- Accumulator to B-Register
- Carry
- Roundoff
- Product Sign
- Accumulator Sign
- A-Register Sign
- Compare
- Multiply
- Shift Left
- Shift Right
- Divide
- Special Add
- Arithmetic Check
- Clear Accumulator
- Clear B-Register

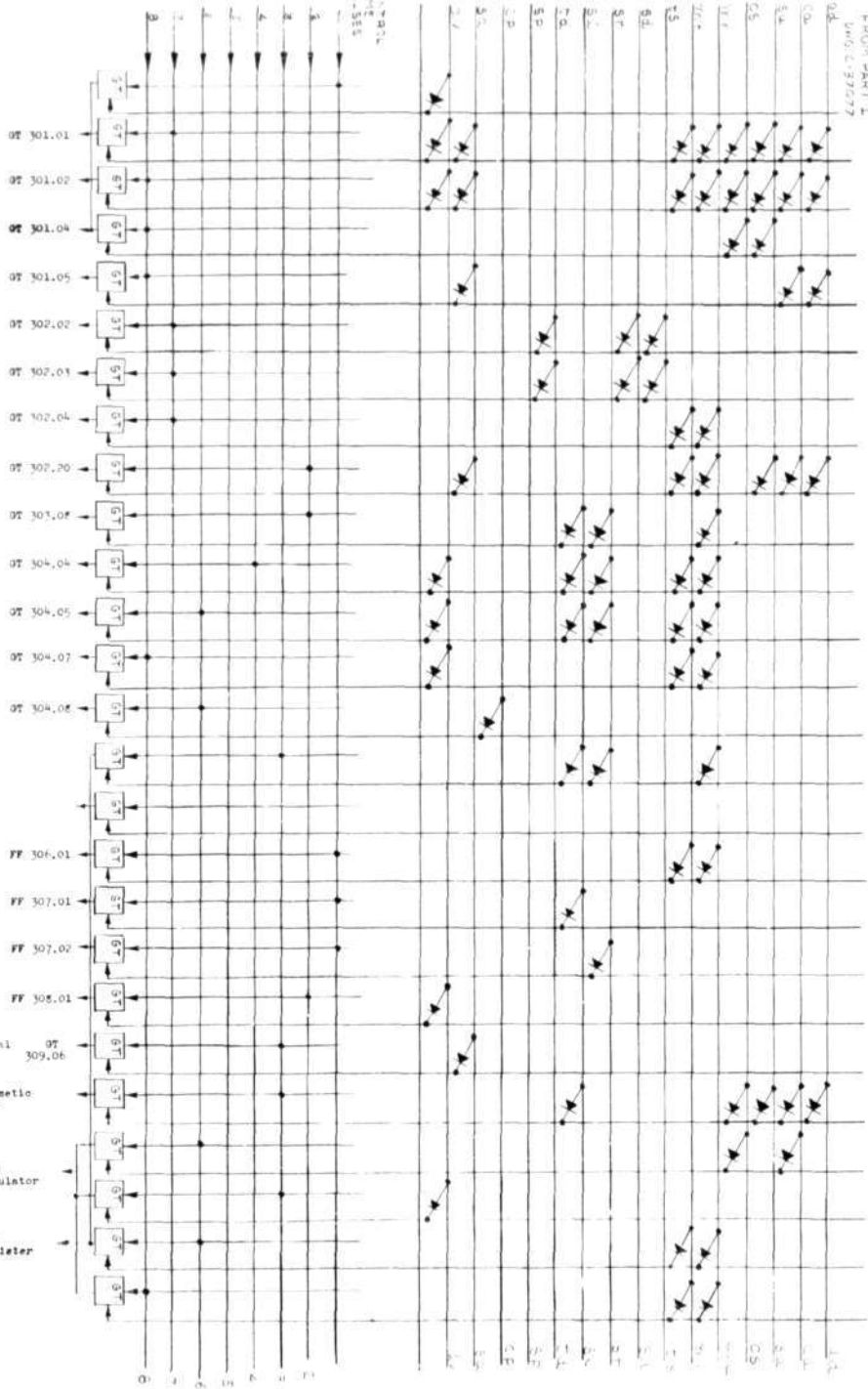


Figure 55
OPERATION MATRIX II

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

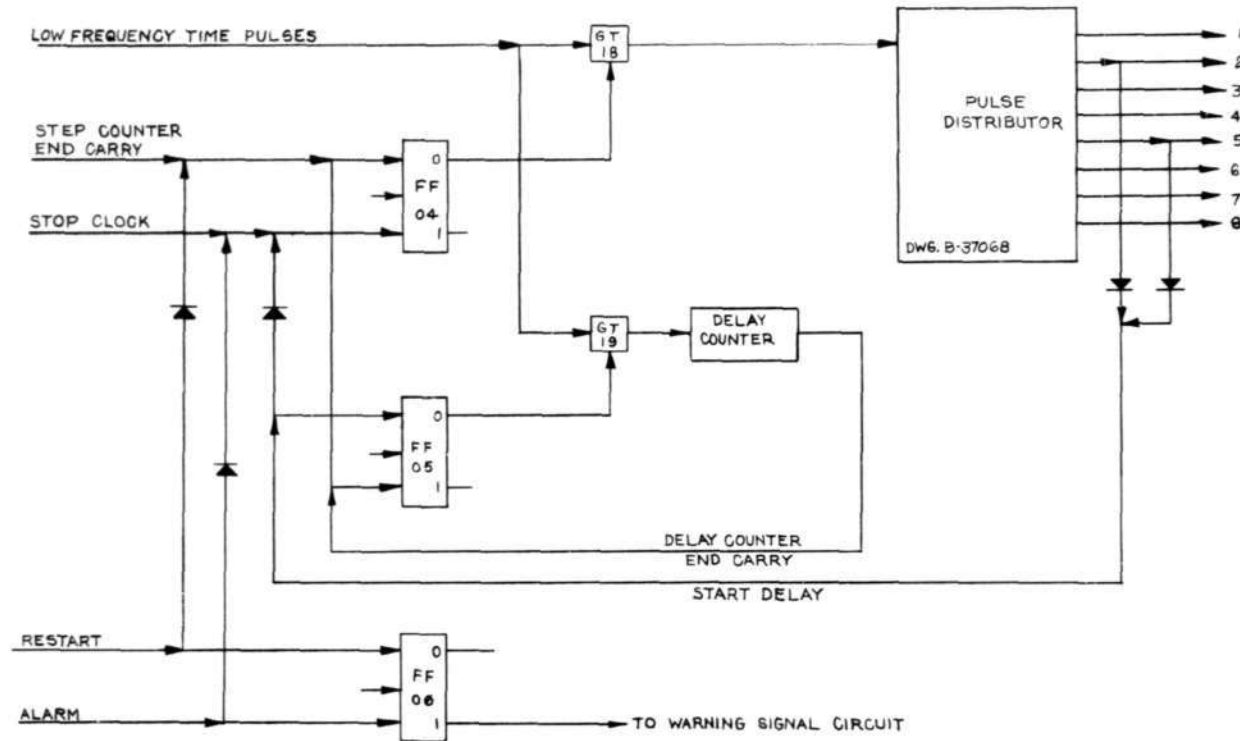


Figure 56
TIME PULSE DISTRIBUTOR CONTROL

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

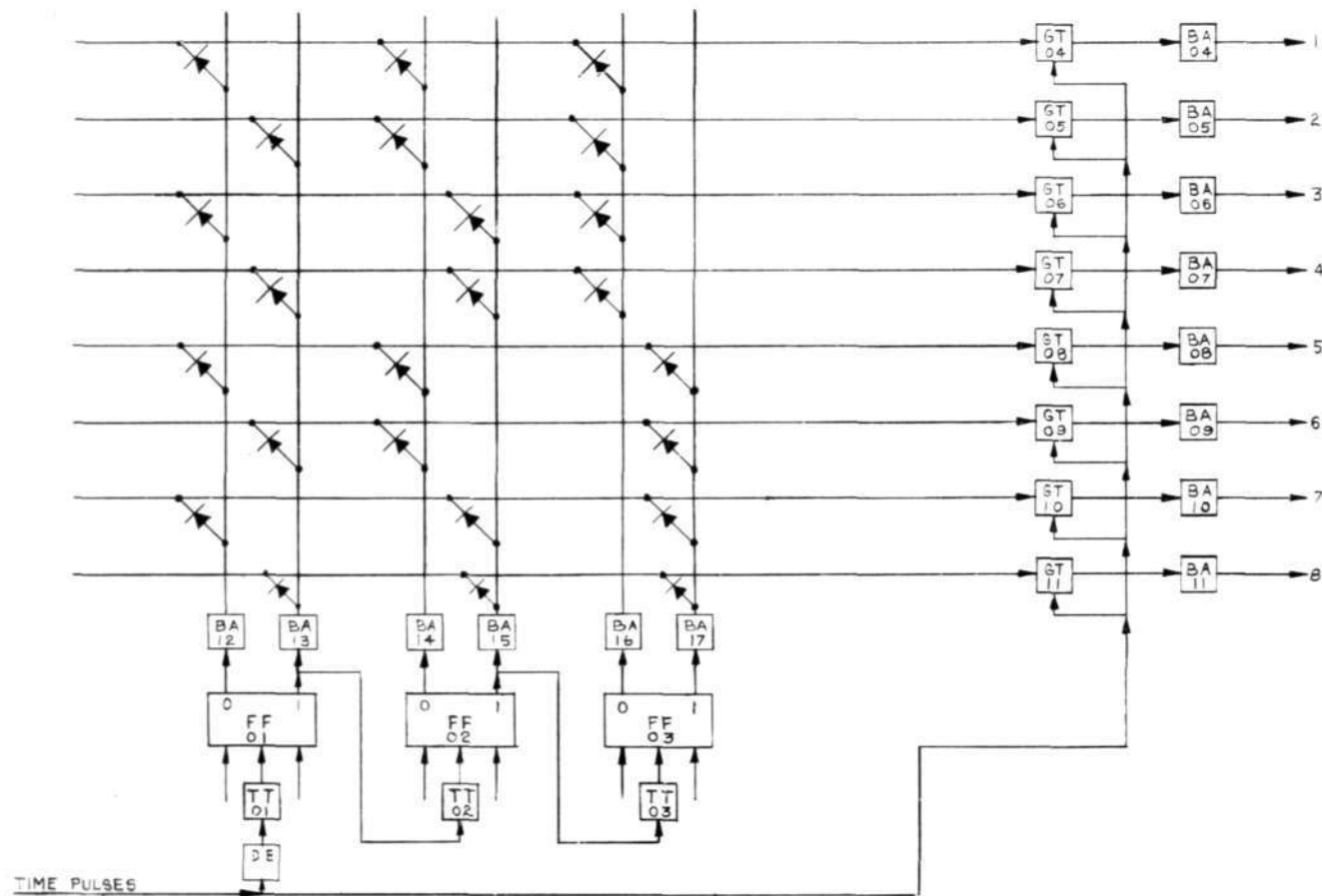
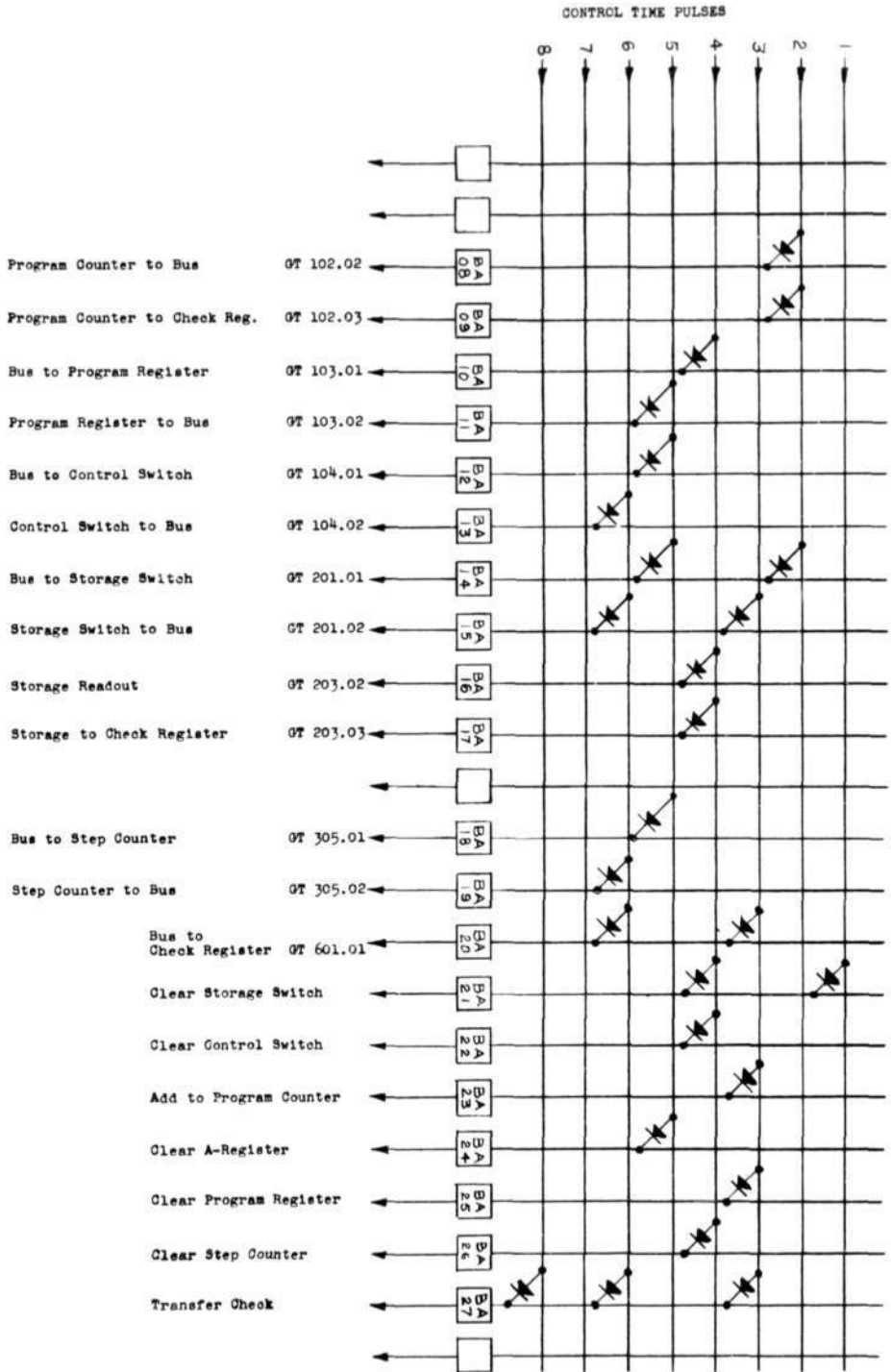


Figure 57
PULSE DISTRIBUTOR

CONFIDENTIAL

PROGRAM TIMING MATRIX
Figure 58



APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

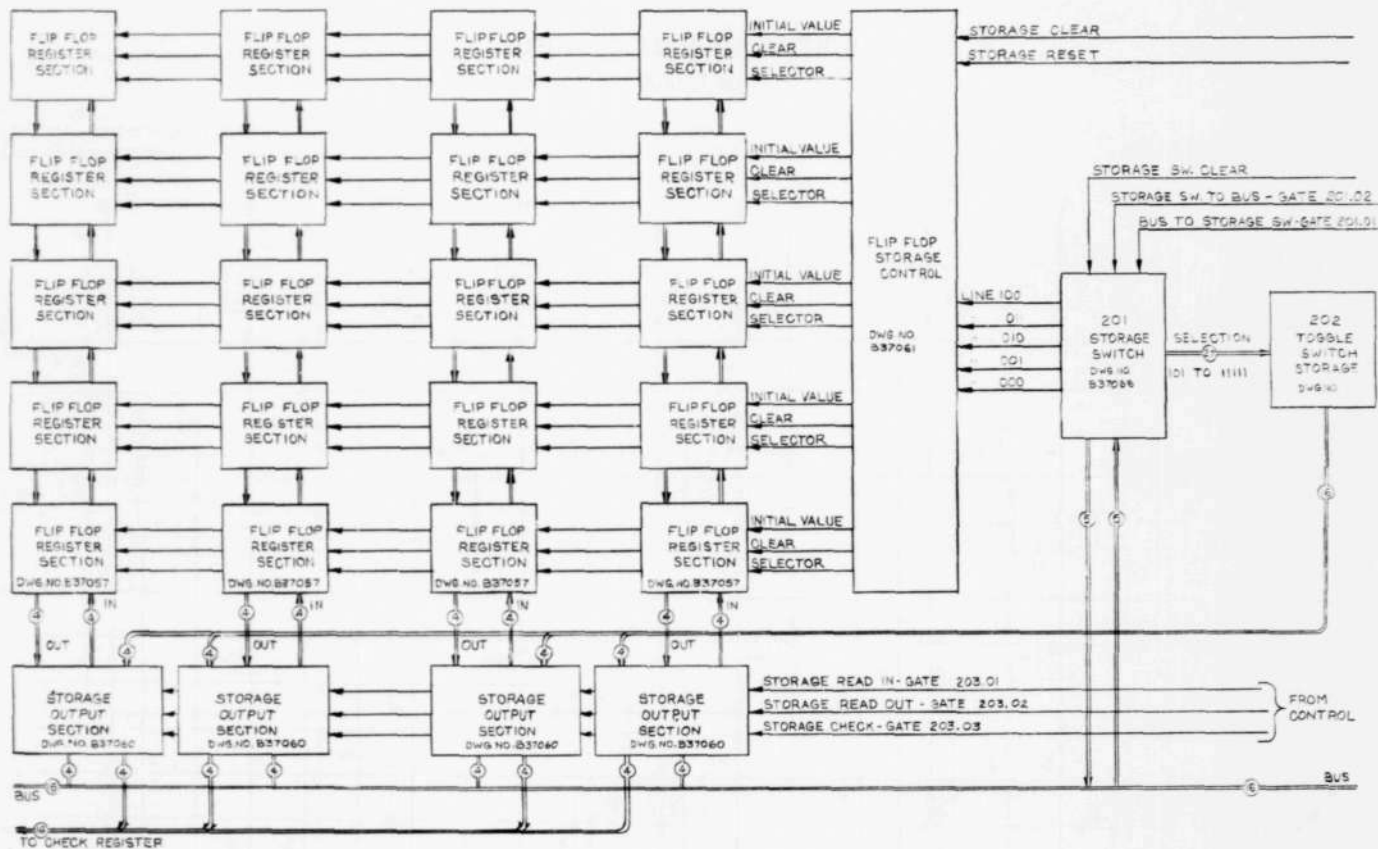


Figure 59

STORAGE CHASSIS ARRANGEMENT

CONFIDENTIAL

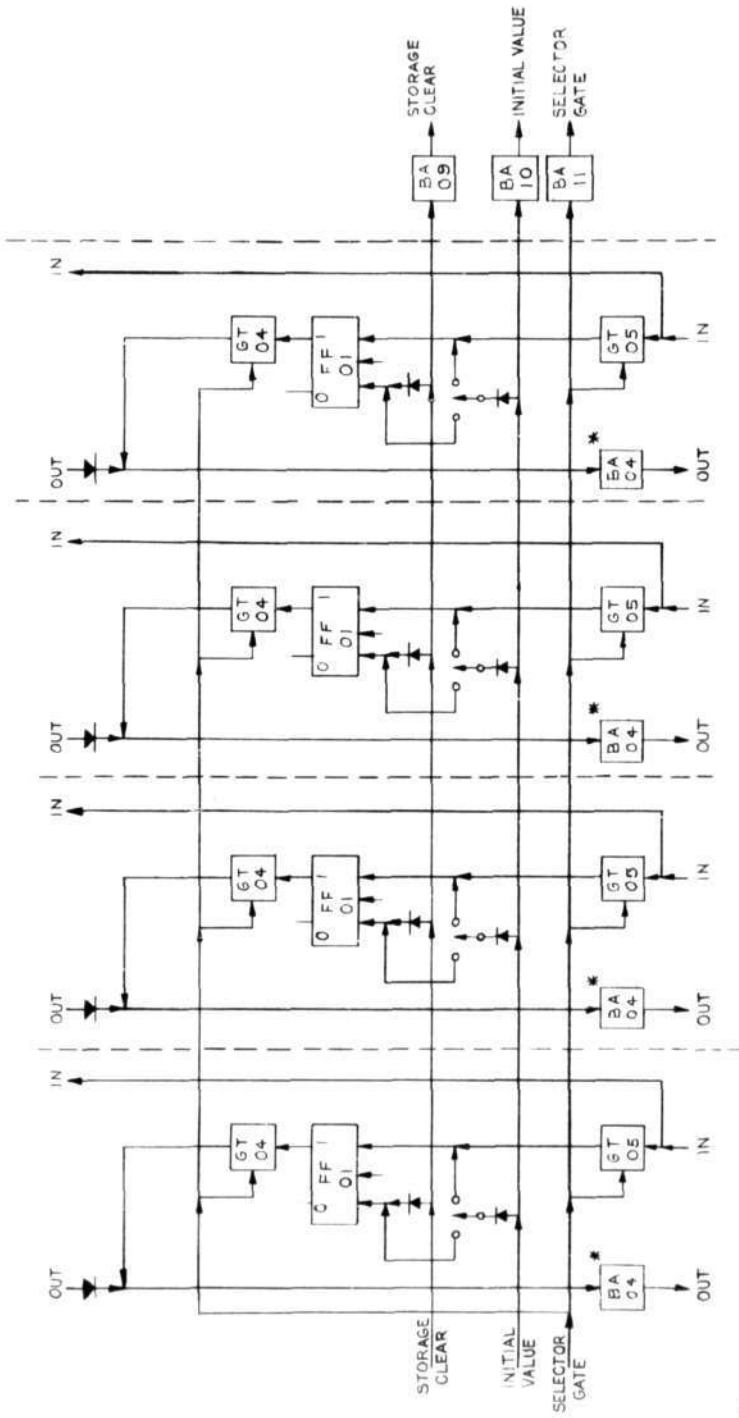


Figure 60
FLIP-FLOP STORAGE SECTION

* THESE AMPLIFIERS IN
BOTTOM SECTION ONLY

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

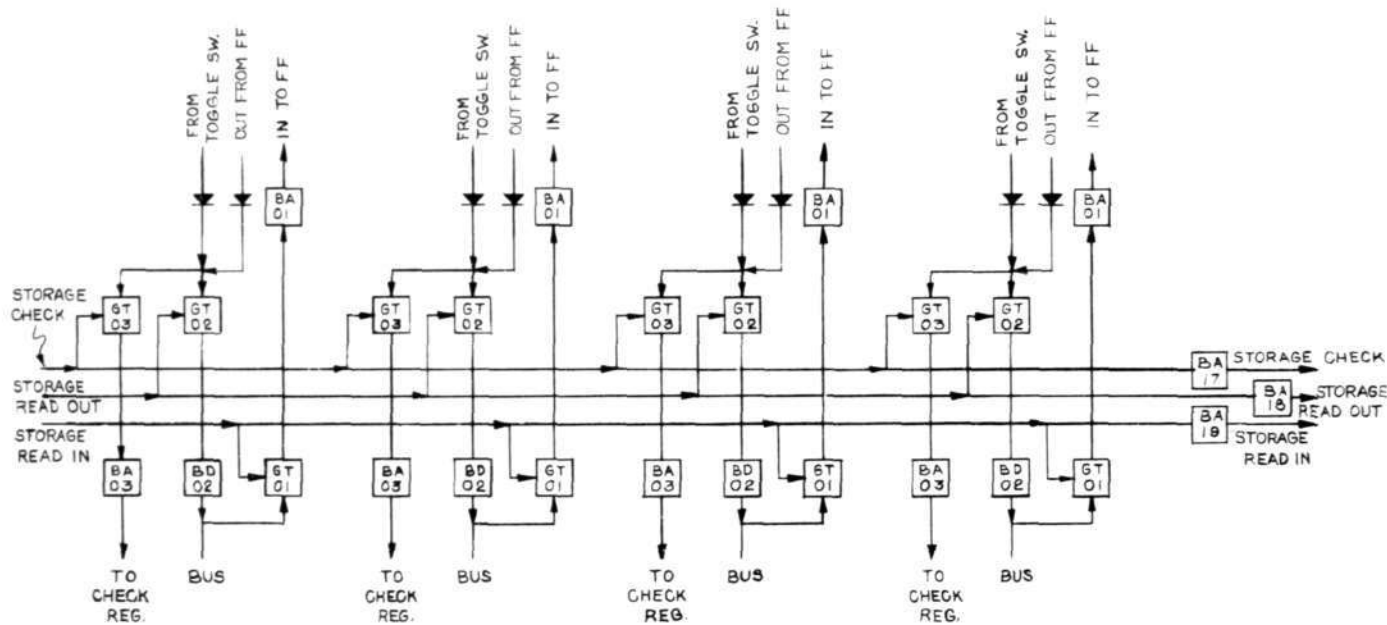


Figure 61
STORAGE OUTPUT SECTION

CONFIDENTIAL

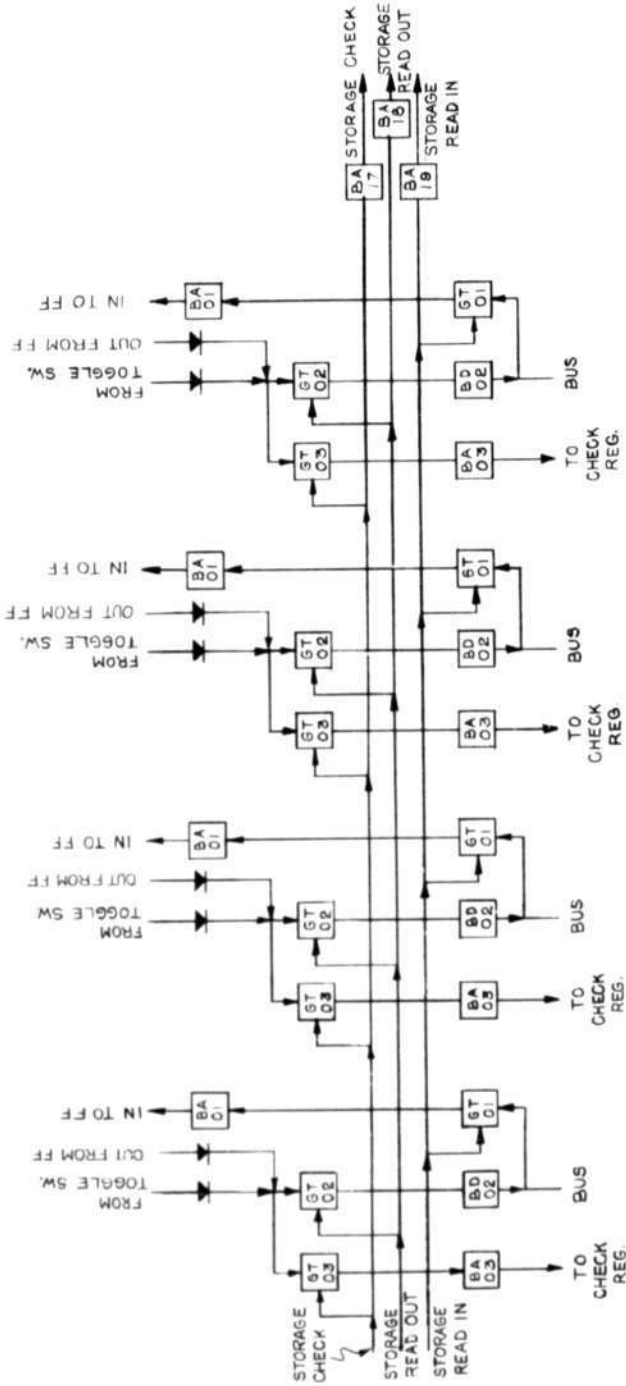


Figure 61
STORAGE OUTPUT SECTION

CONFIDENTIAL

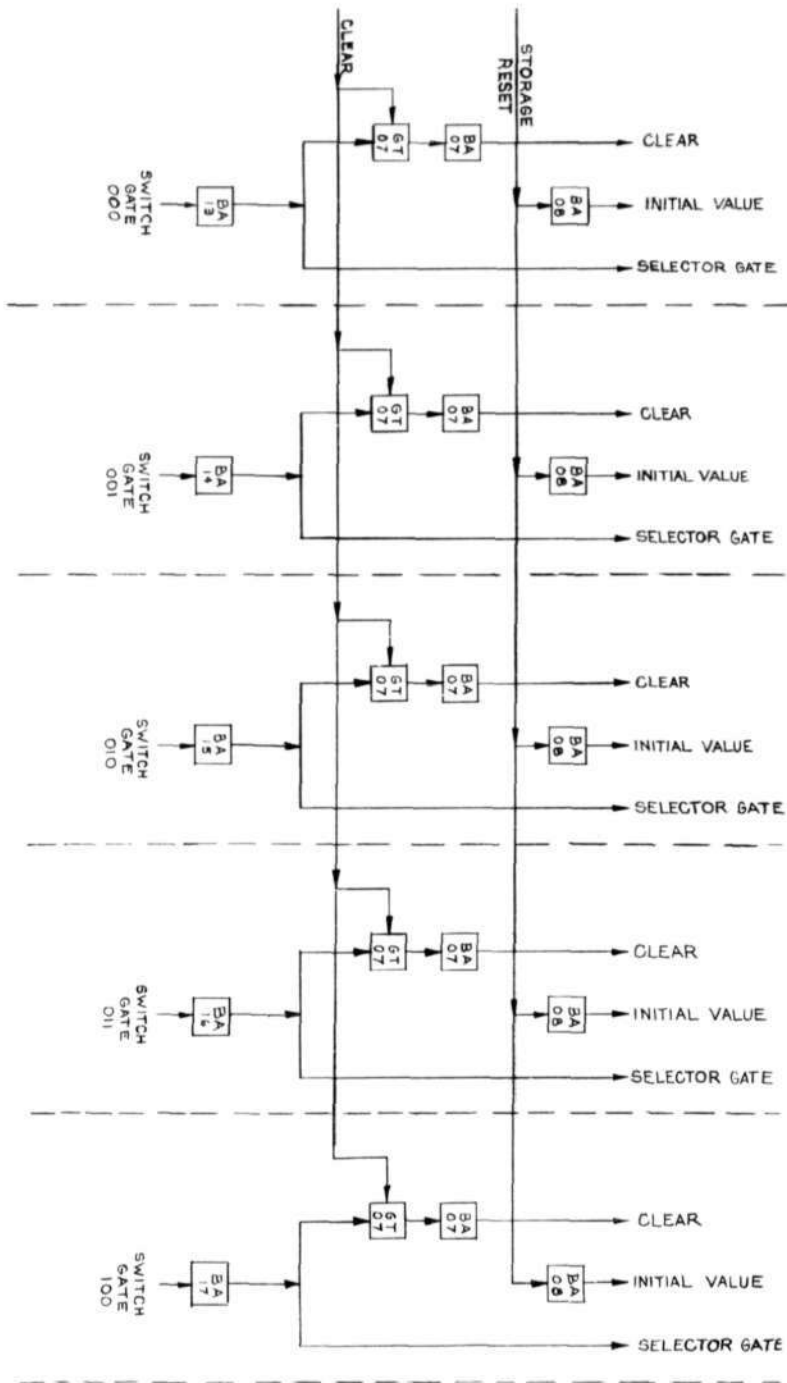


Figure 62
FLIP-FLOP STORAGE CONTROL

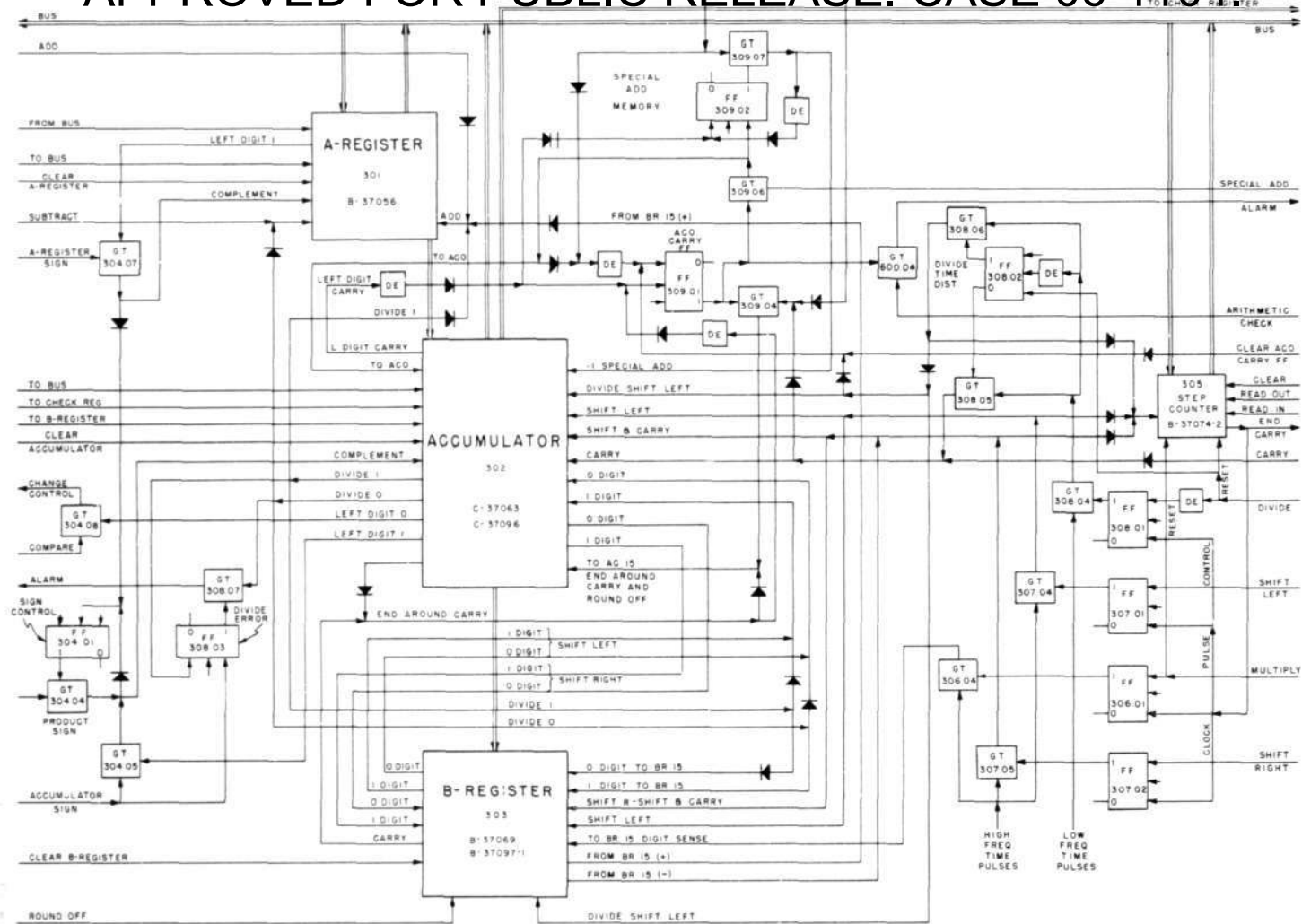


Figure 63
ARITHMETIC ELEMENT

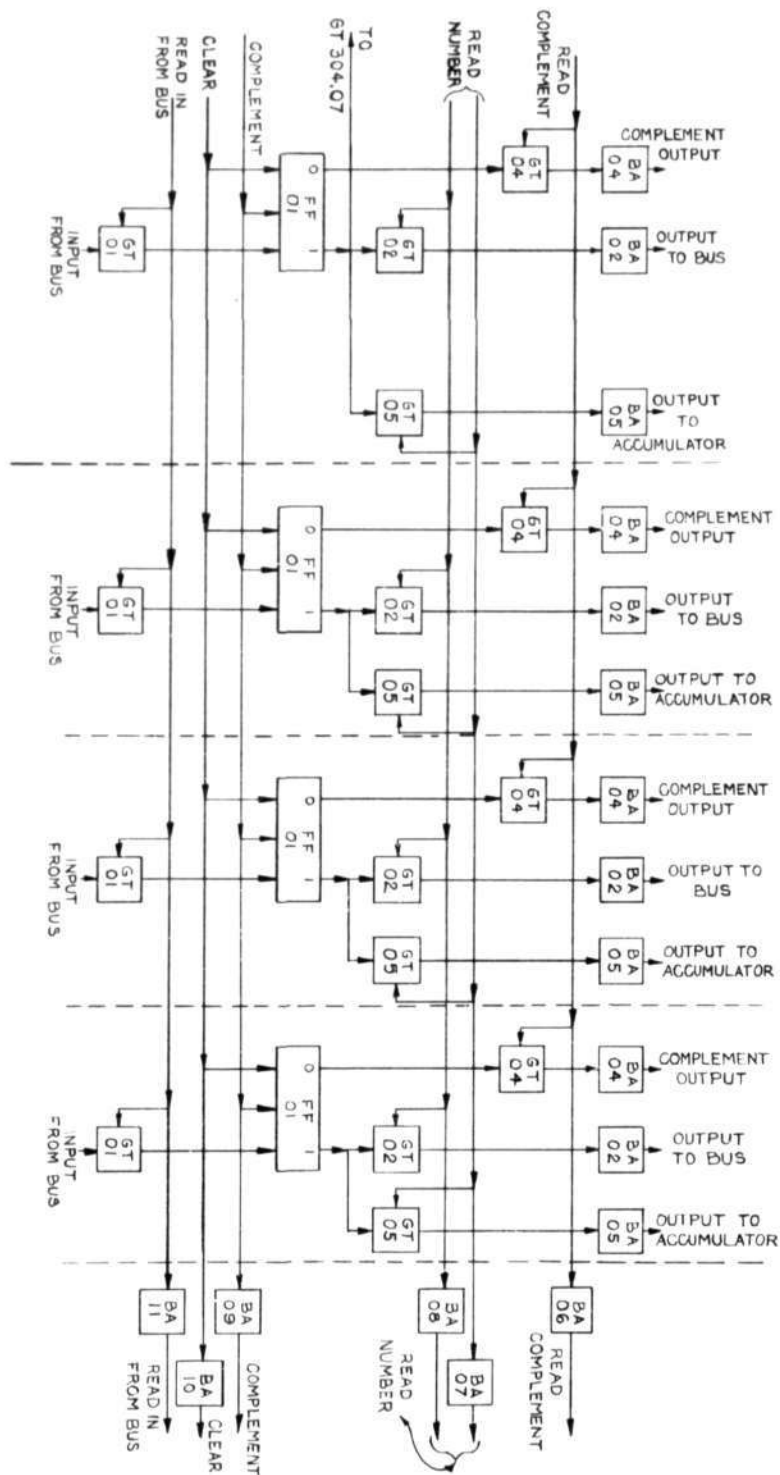


Figure 64
SECTION OF A-REGISTER

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

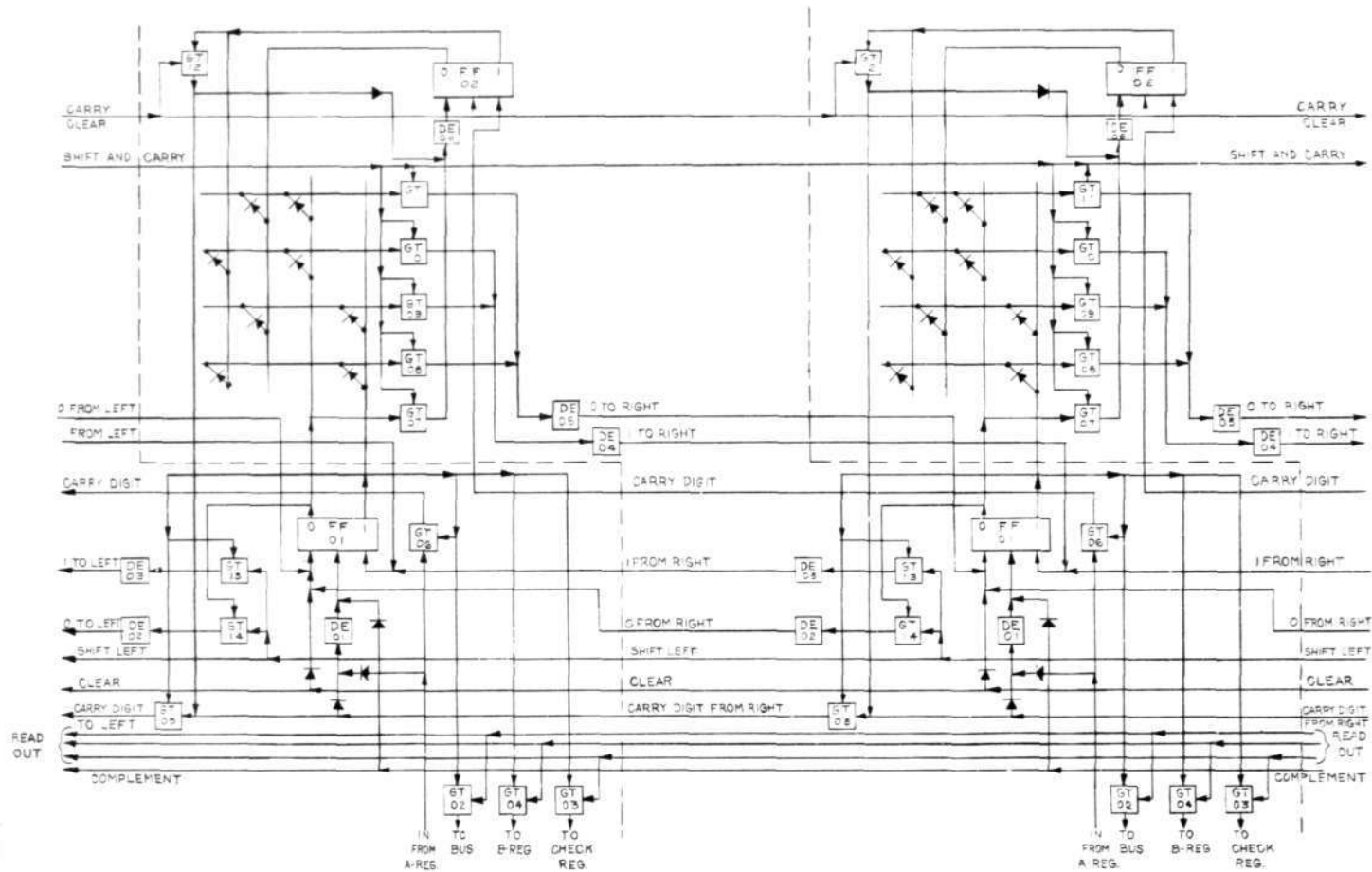


Figure 65
ACCUMULATOR SECTIONS

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

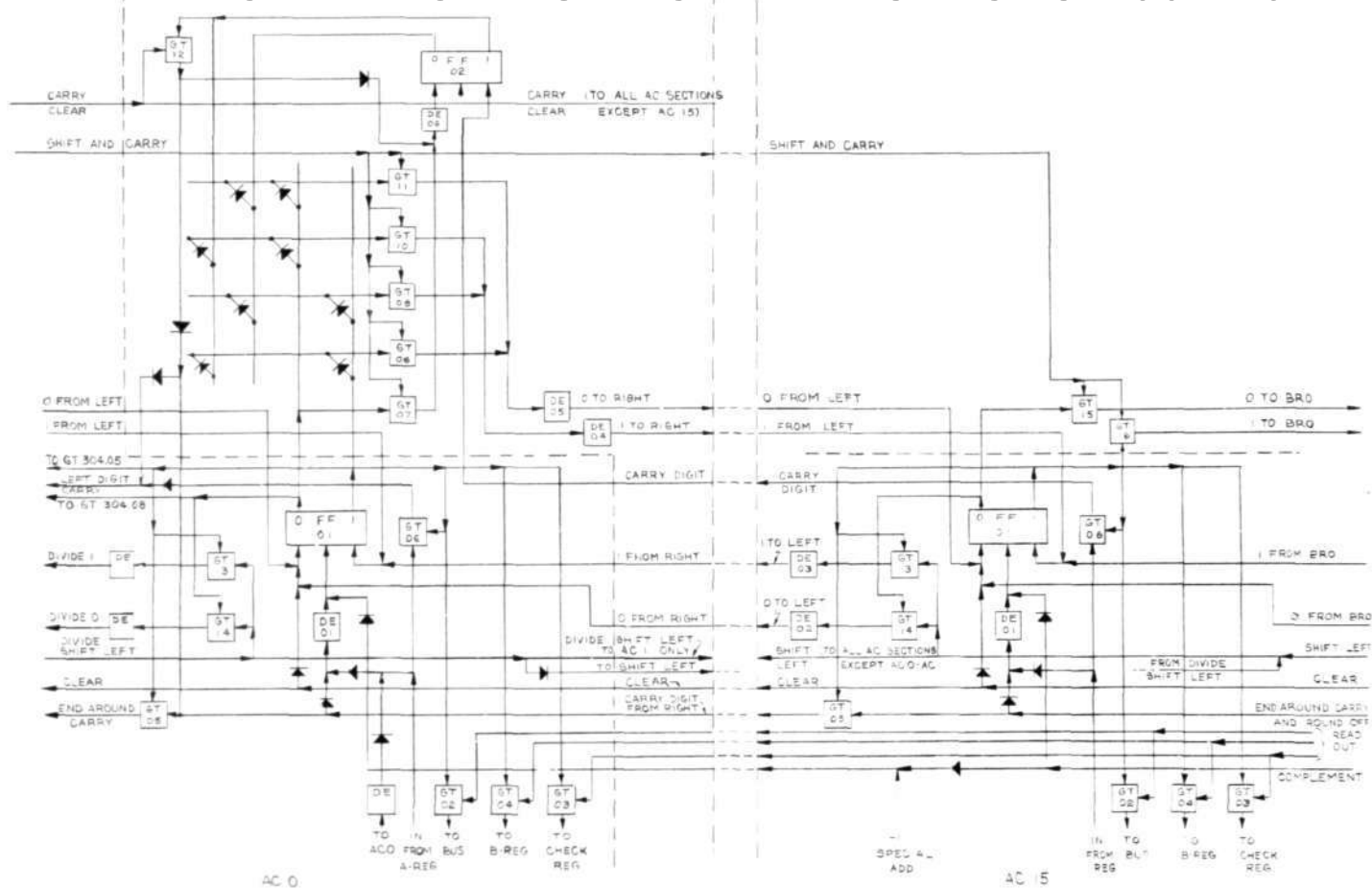


Figure 66
ACCUMULATOR SECTIONS AC0-AC15

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

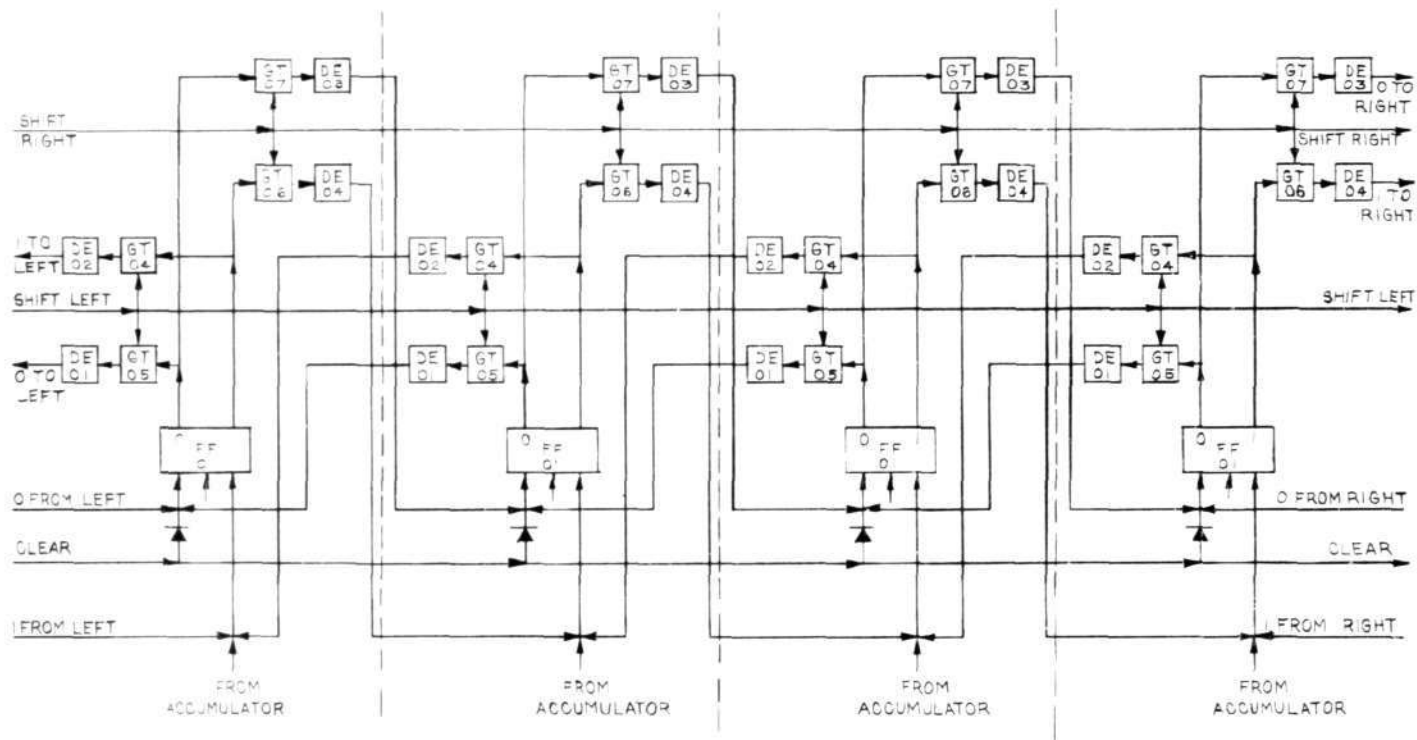


Figure 67
B-REGISTER SECTIONS

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

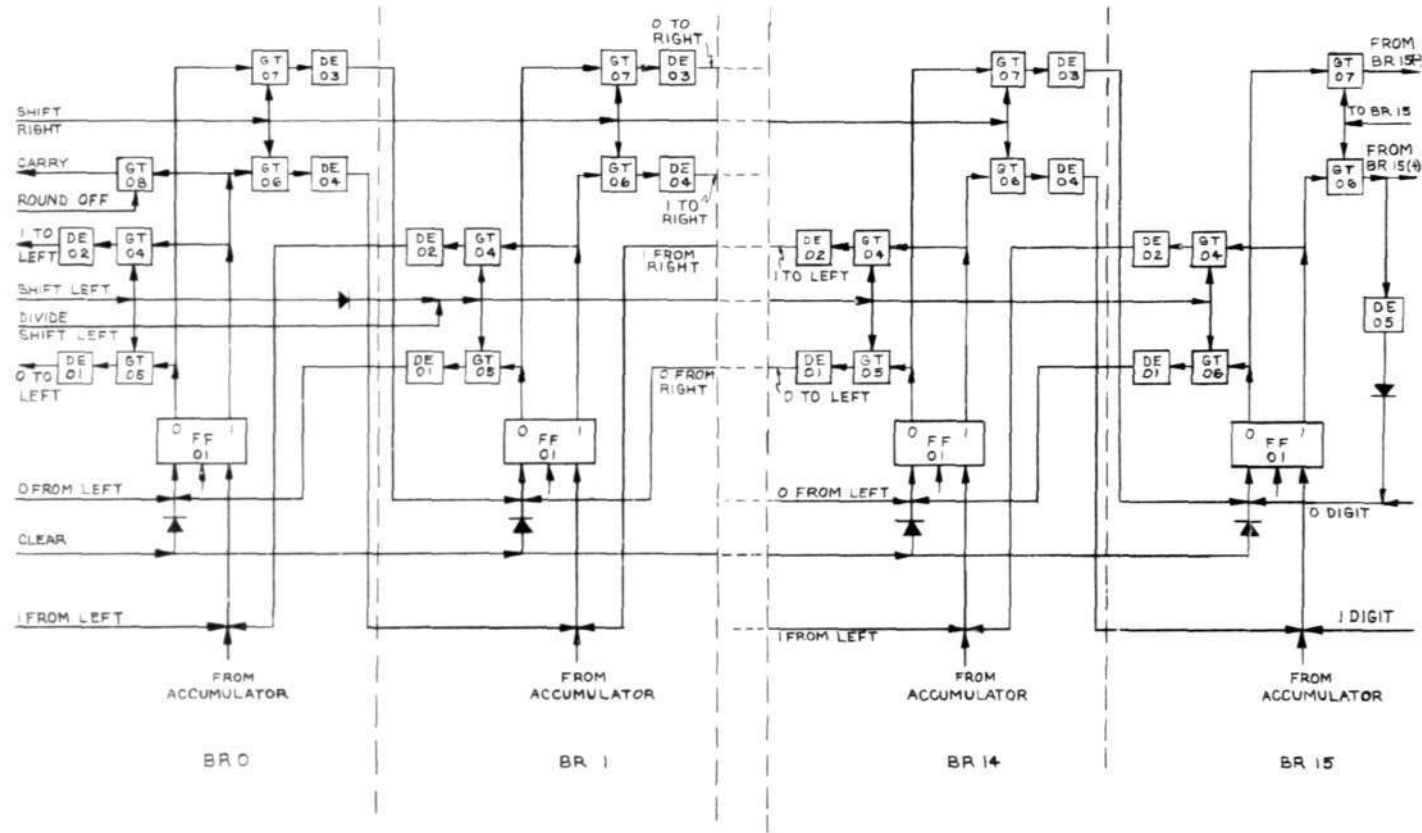


Figure 68
B-REGISTER SECTIONS BR 0, 1, 14, 15

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

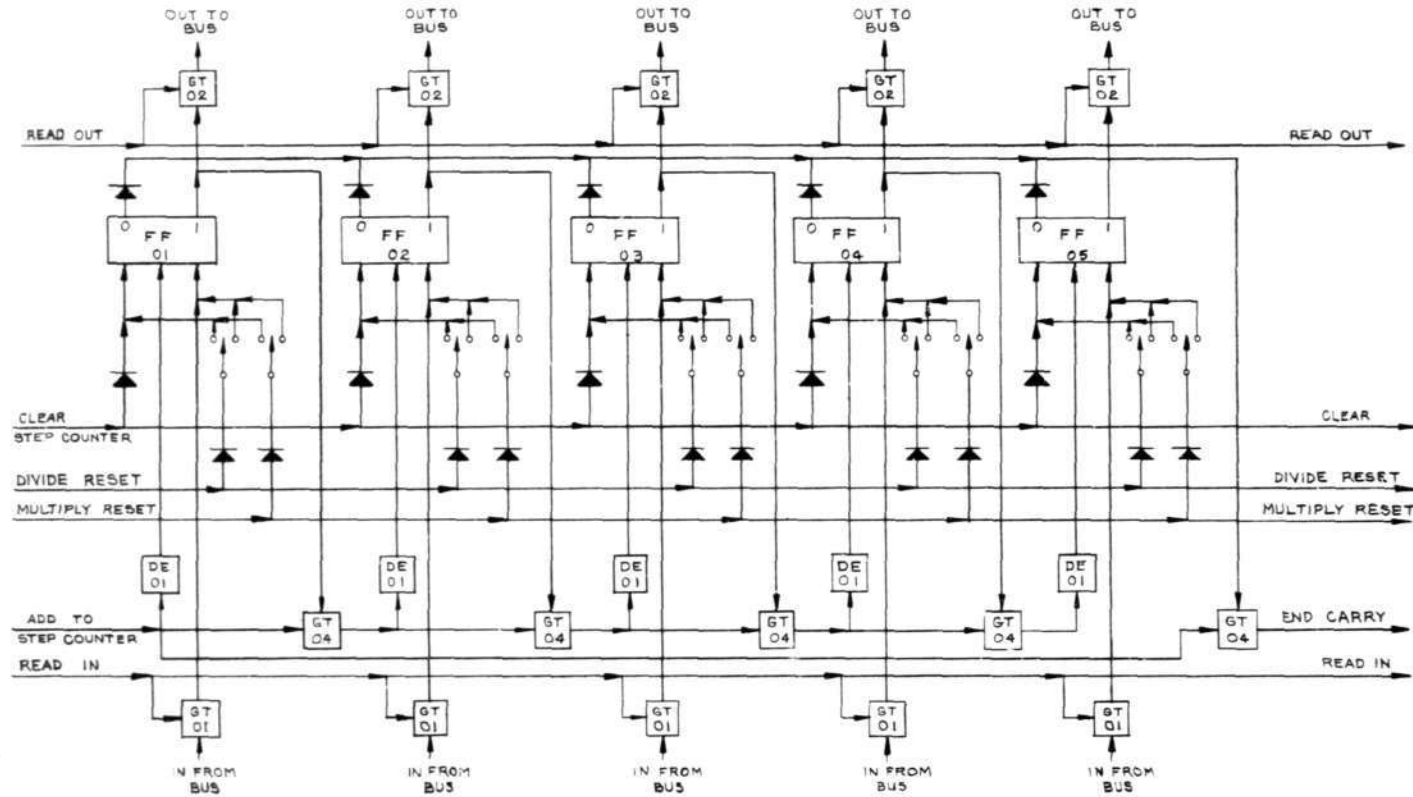


Figure 69
STEP COUNTER

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APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

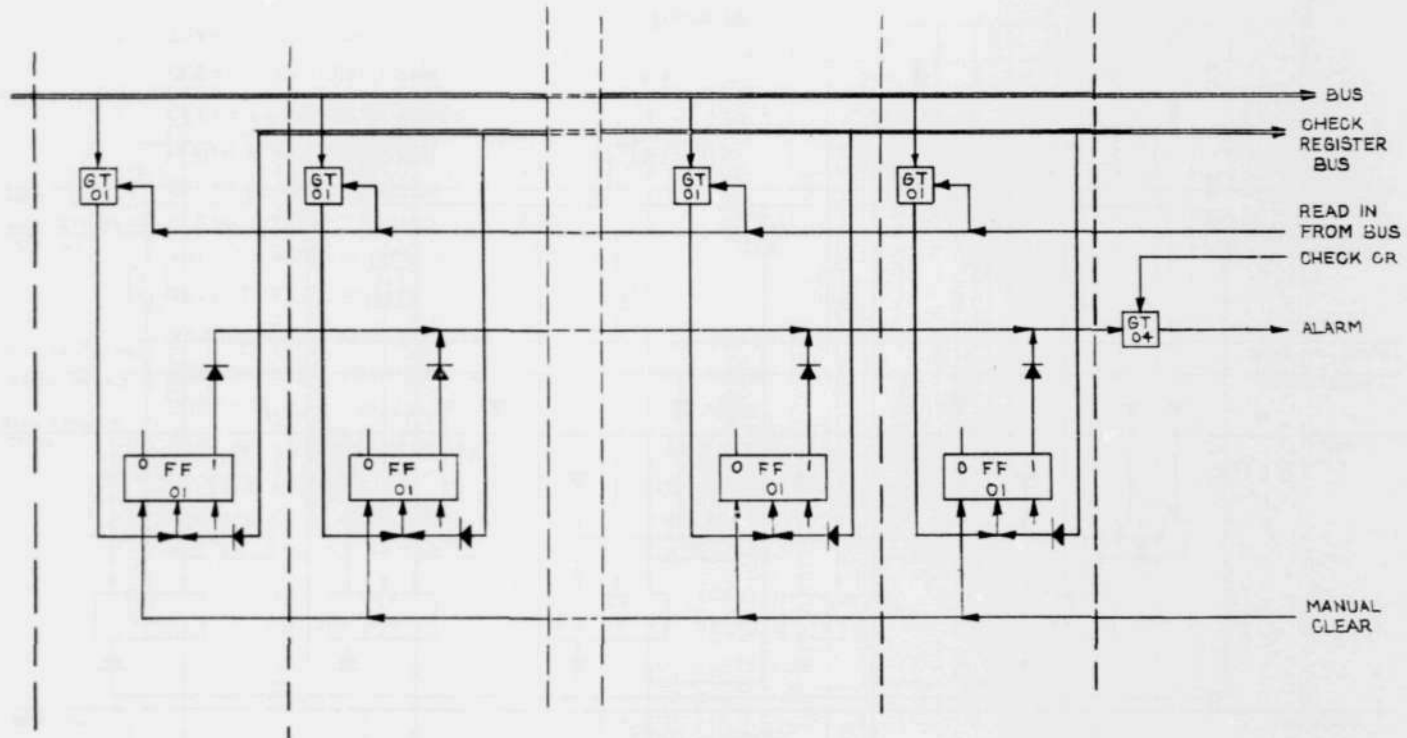


Figure 70
CHECK REGISTER

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

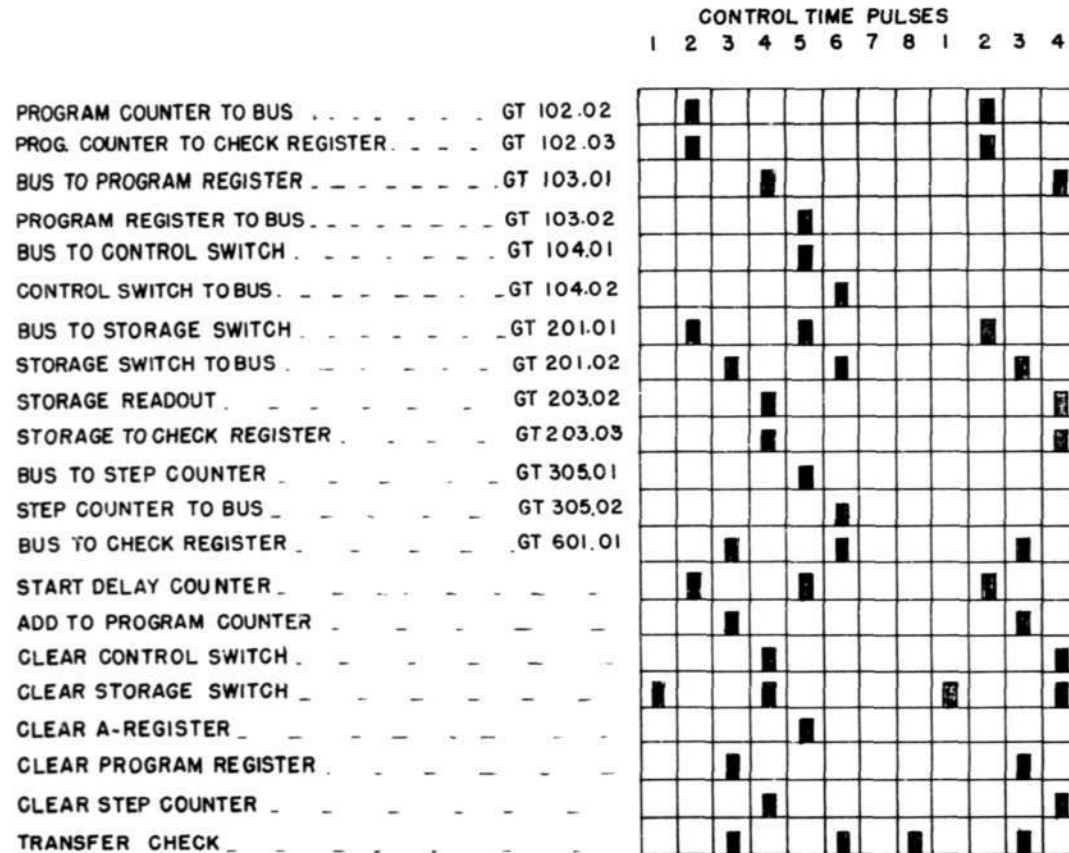


Figure 71
PROGRAM TIMING

CONFIDENTIAL

OPERATION: ADD ad

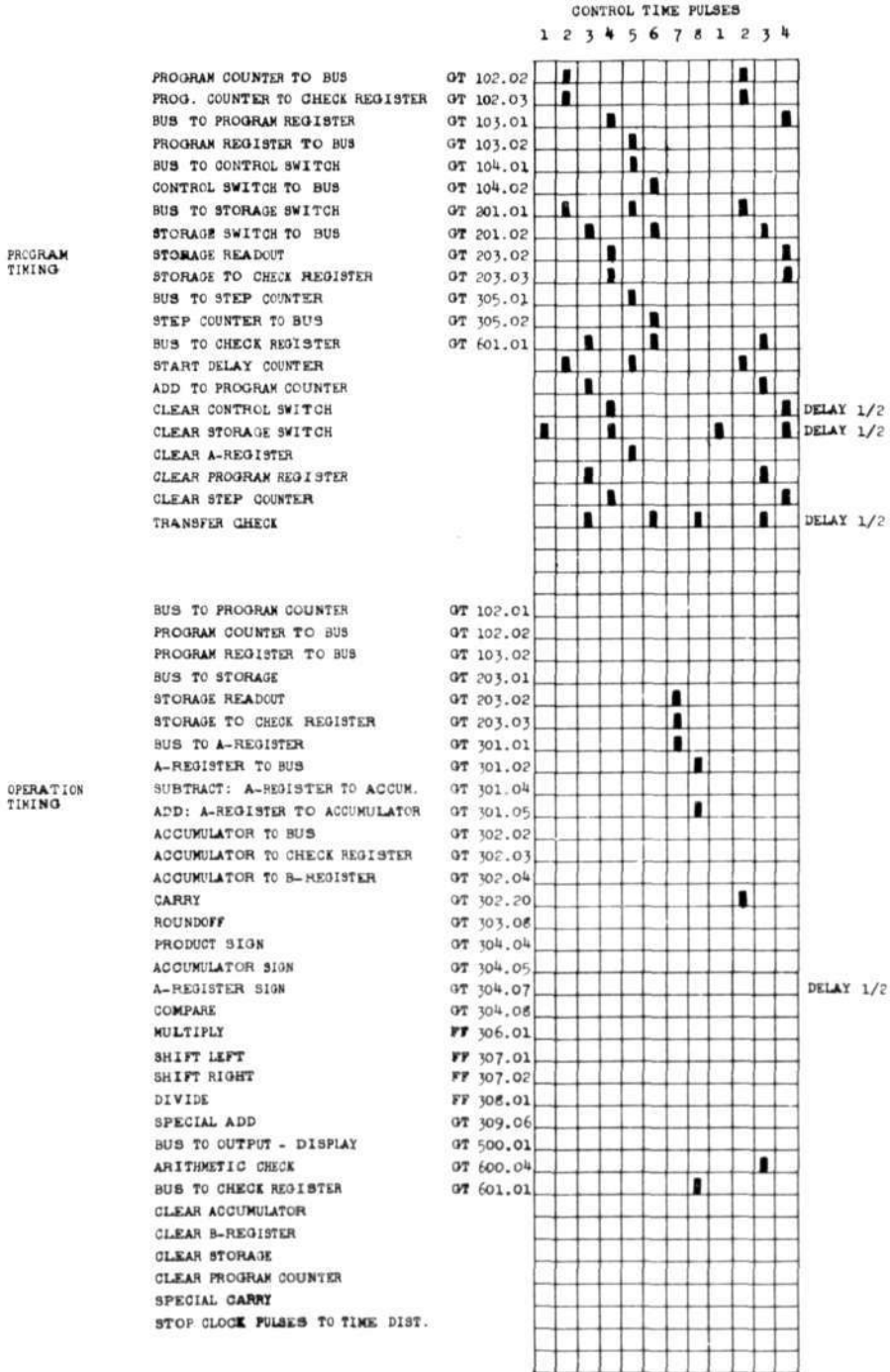


Figure 72
TIMING FOR ADD

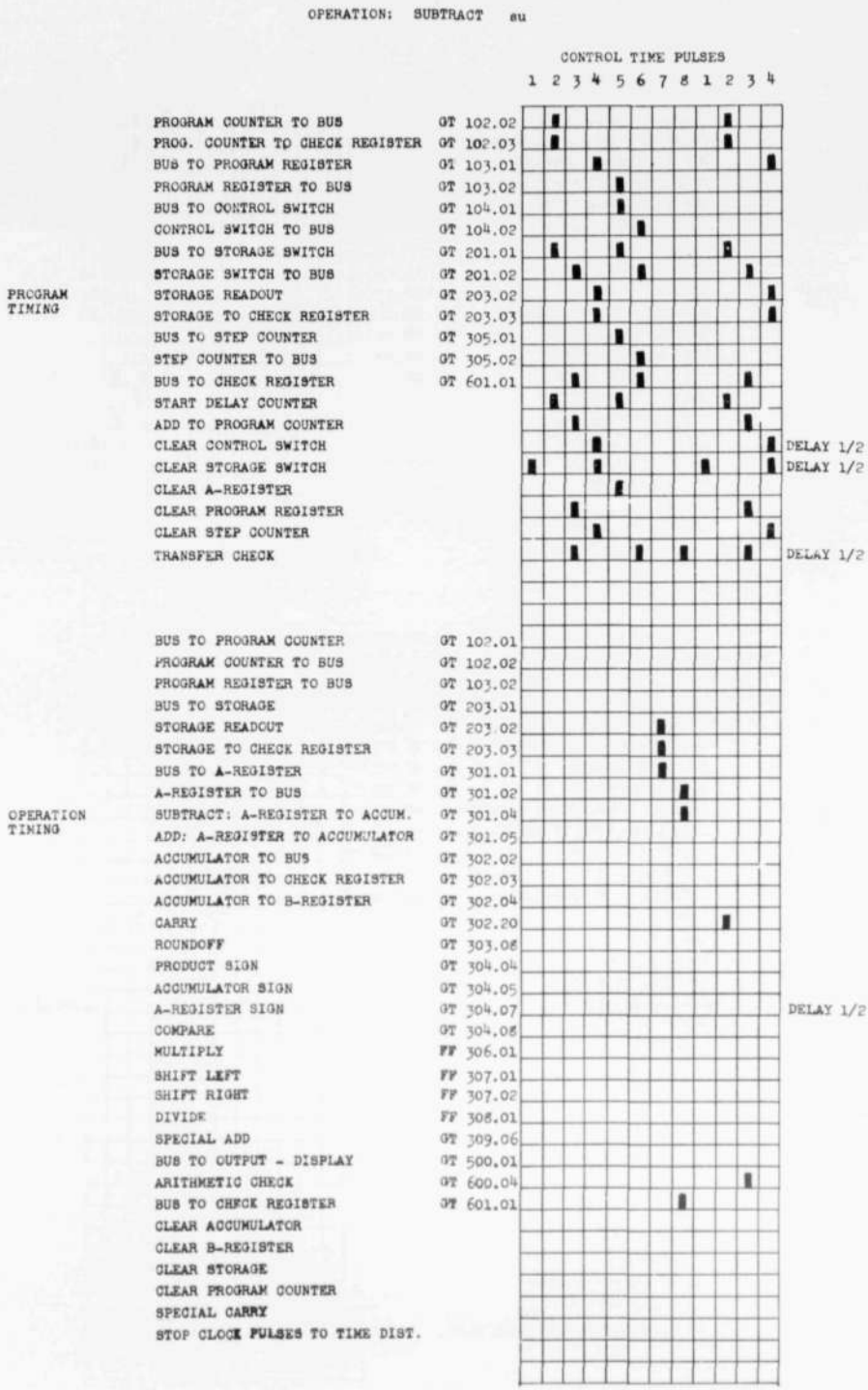


Figure 74
TIMING FOR SUBTRACT

OPERATION: MULTIPLY AND HOLD FULL PRODUCT msh

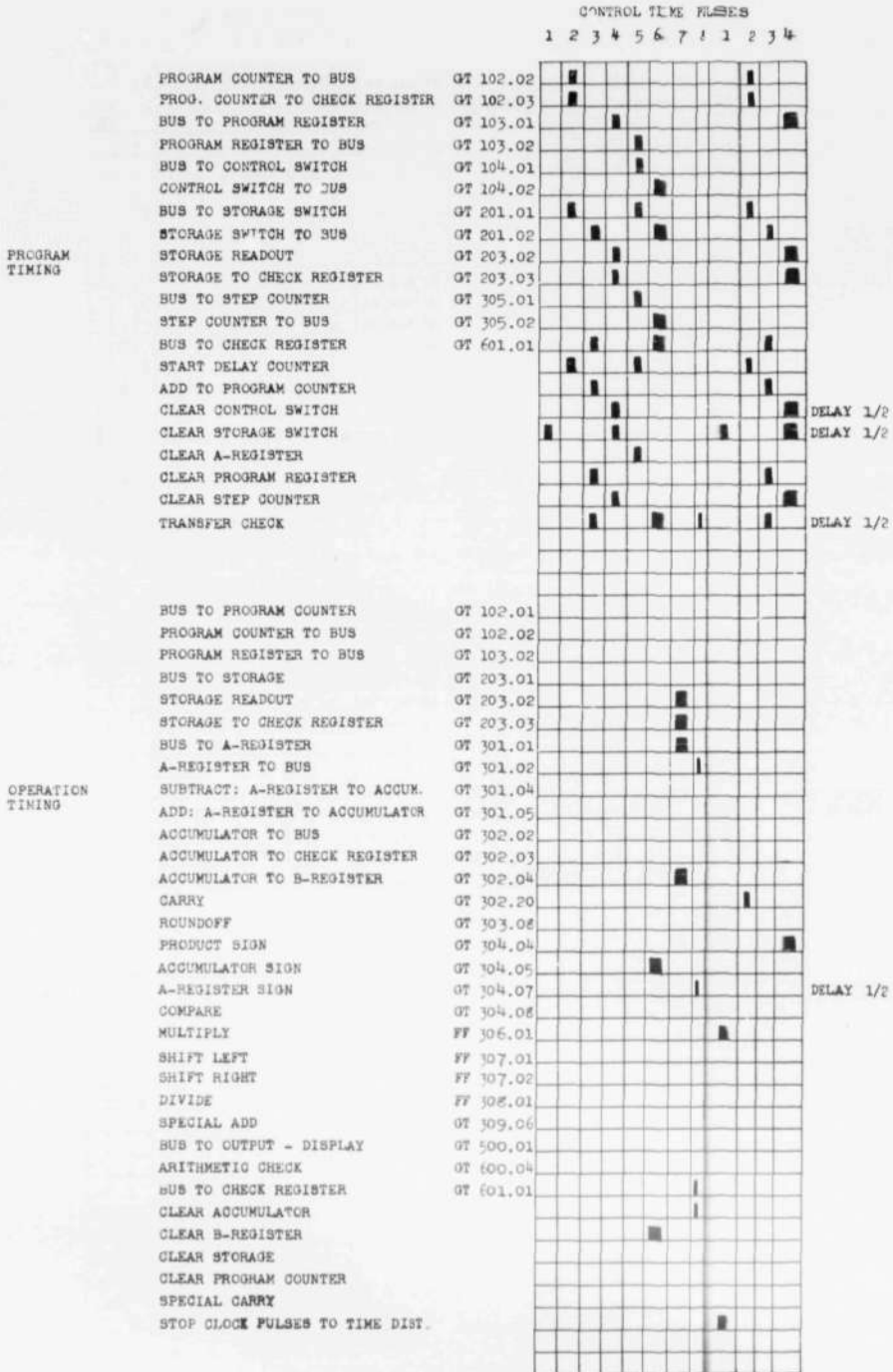


Figure 77
TIMING FOR MULTIPLY AND HOLD FULL
PRODUCT

CONFIDENTIAL

OPERATION: DIVIDE dv

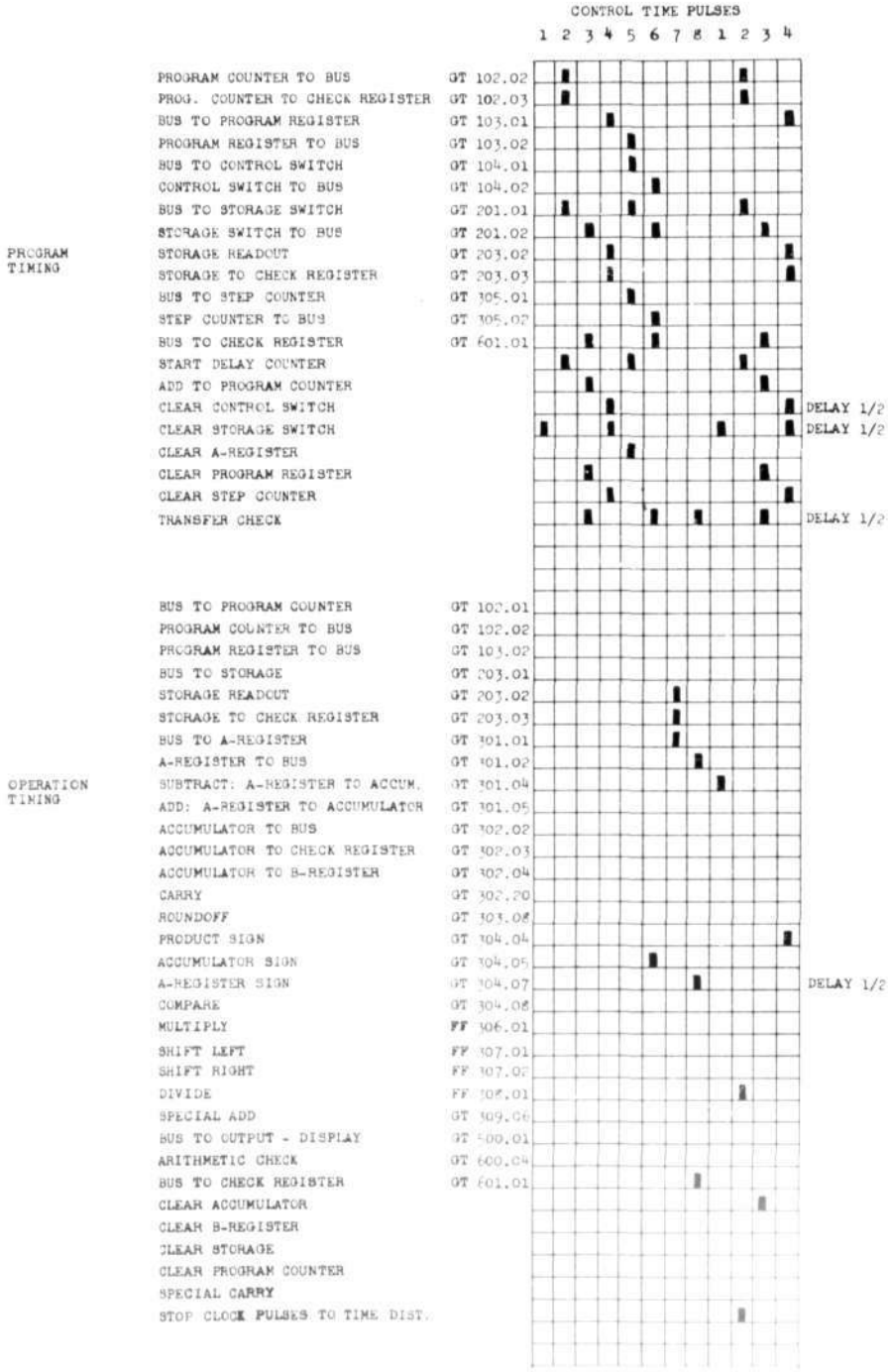


Figure 78
TIMING FOR DIVIDE

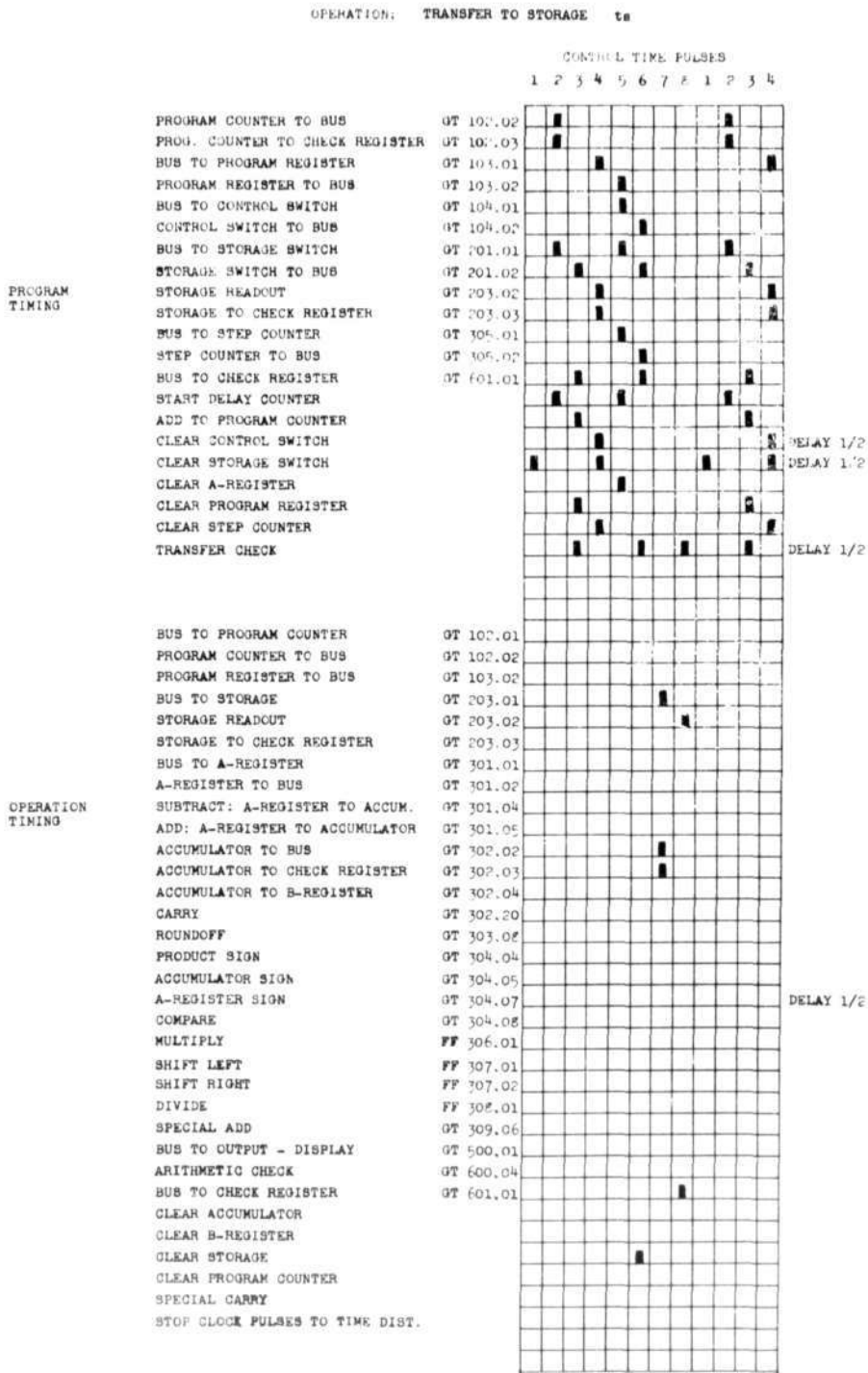


Figure 79
TIMING FOR TRANSFER TO STORAGE

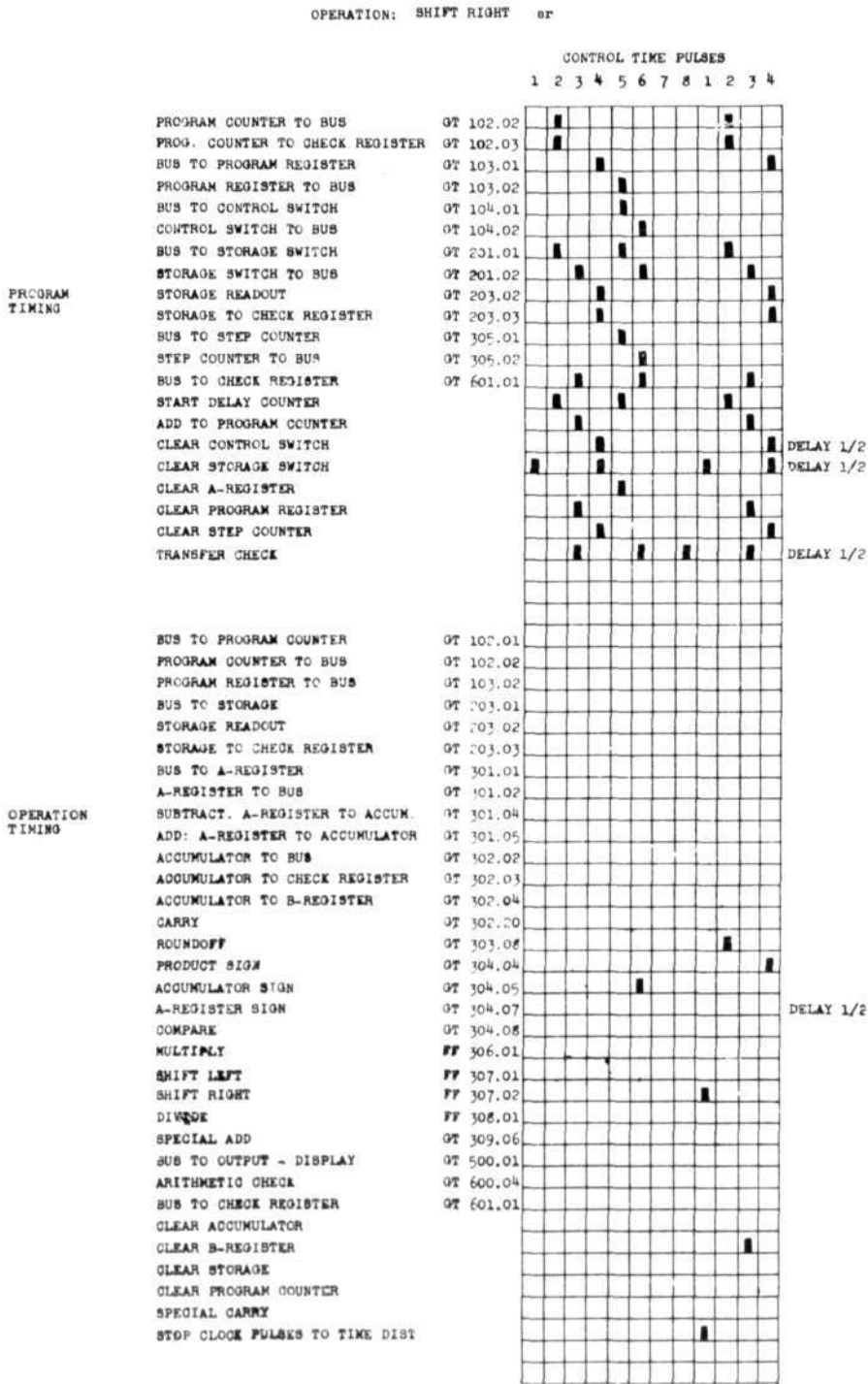


Figure 80
TIMING FOR SHIFT RIGHT

OPERATION: SHIFT LEFT 81

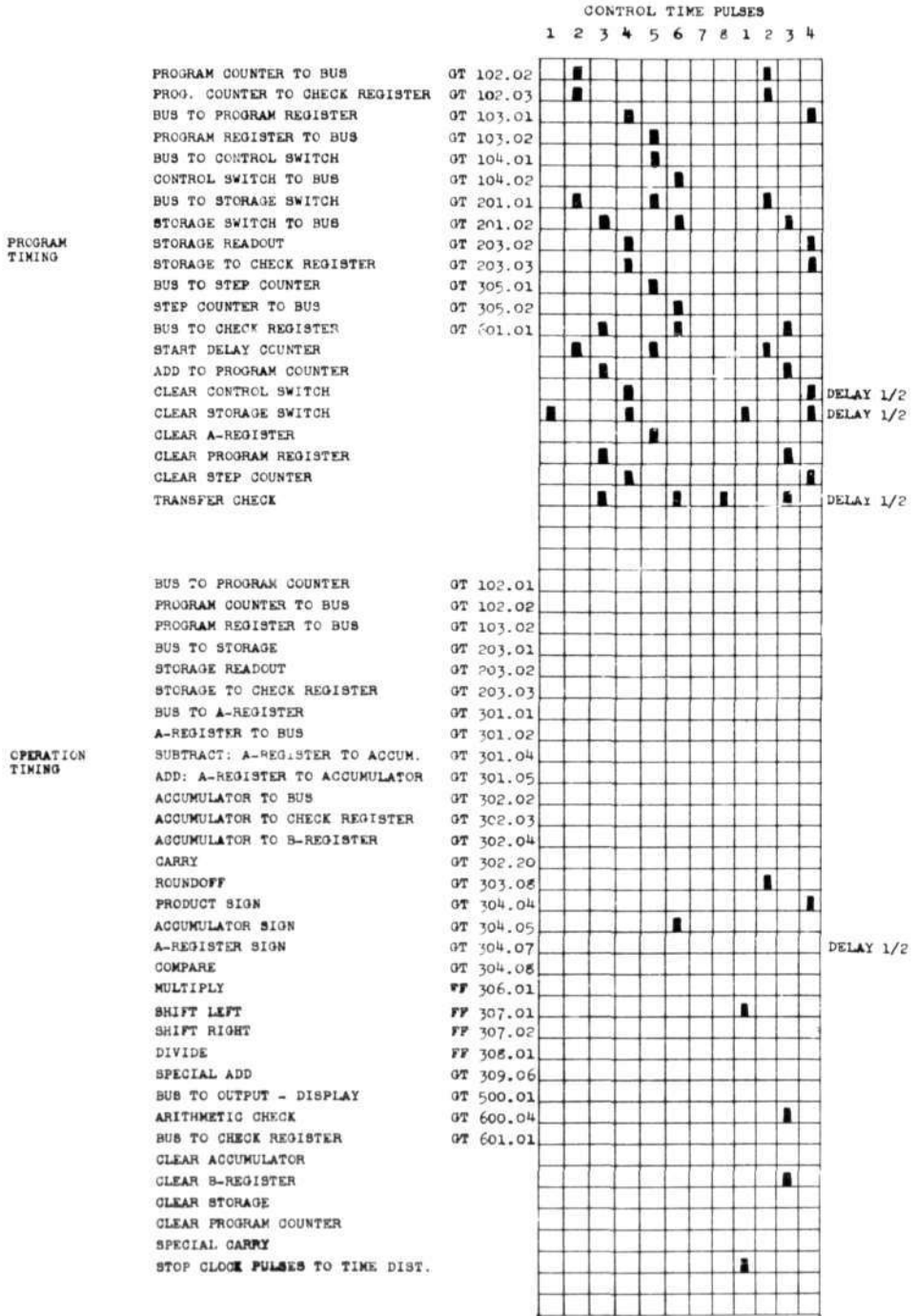


Figure 81
TIMING FOR SHIFT LEFT

OPERATION: COMPARE op

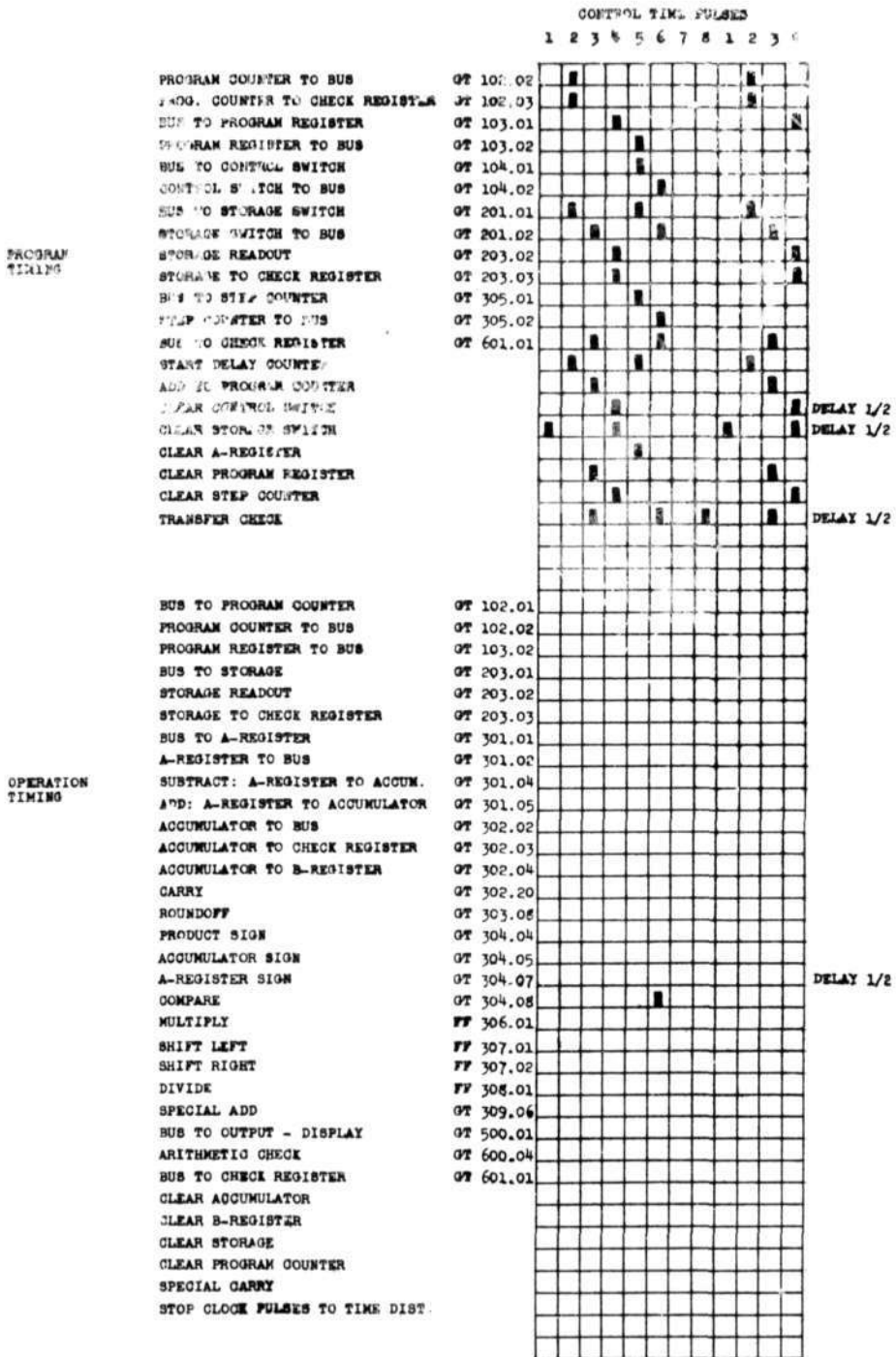


Figure 83

TIMING FOR CONDITIONAL PROGRAM

Handwritten signature or initials

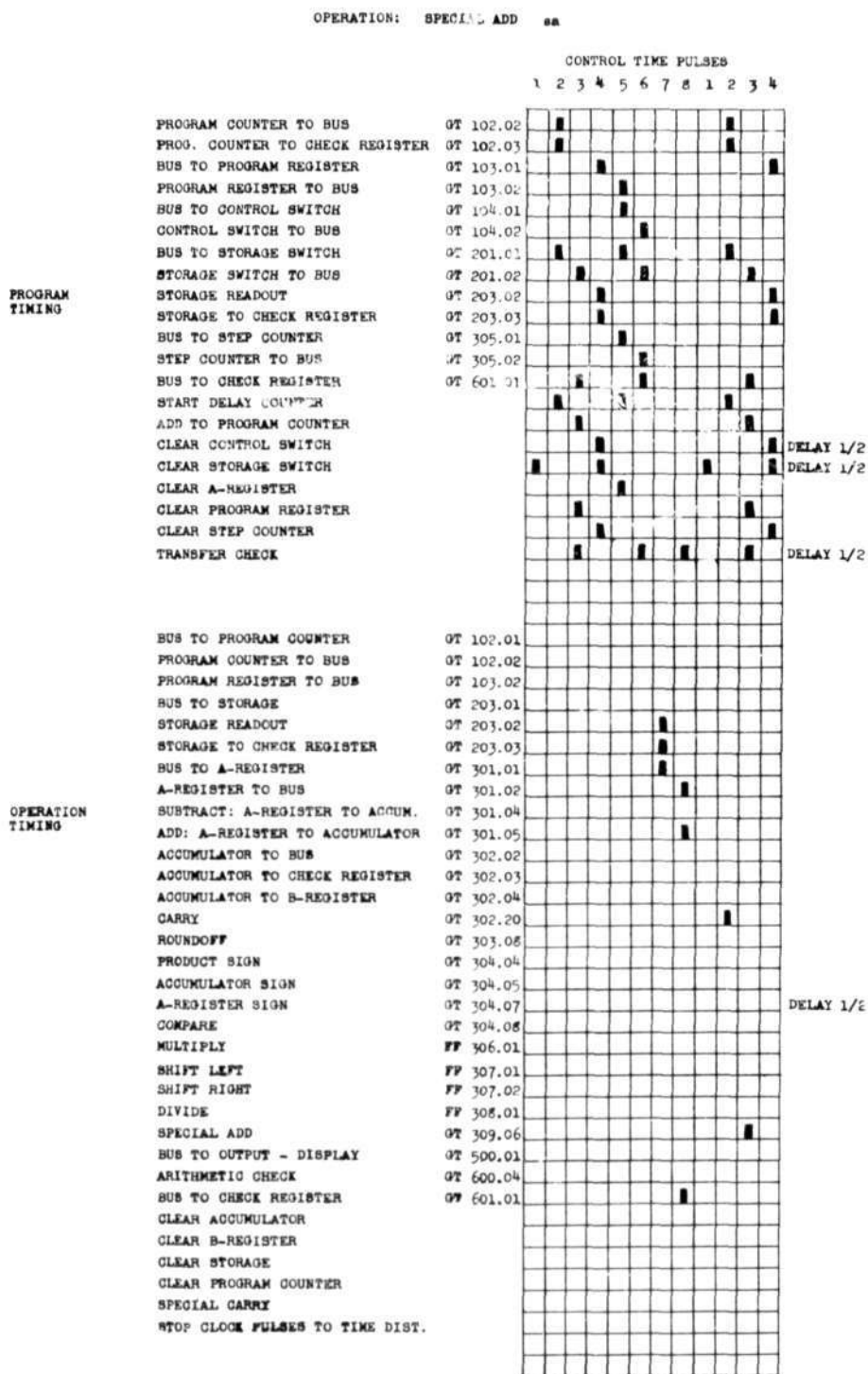


Figure 85
TIMING FOR SPECIAL ADD

OPERATION: STORE AND DISPLAY ad

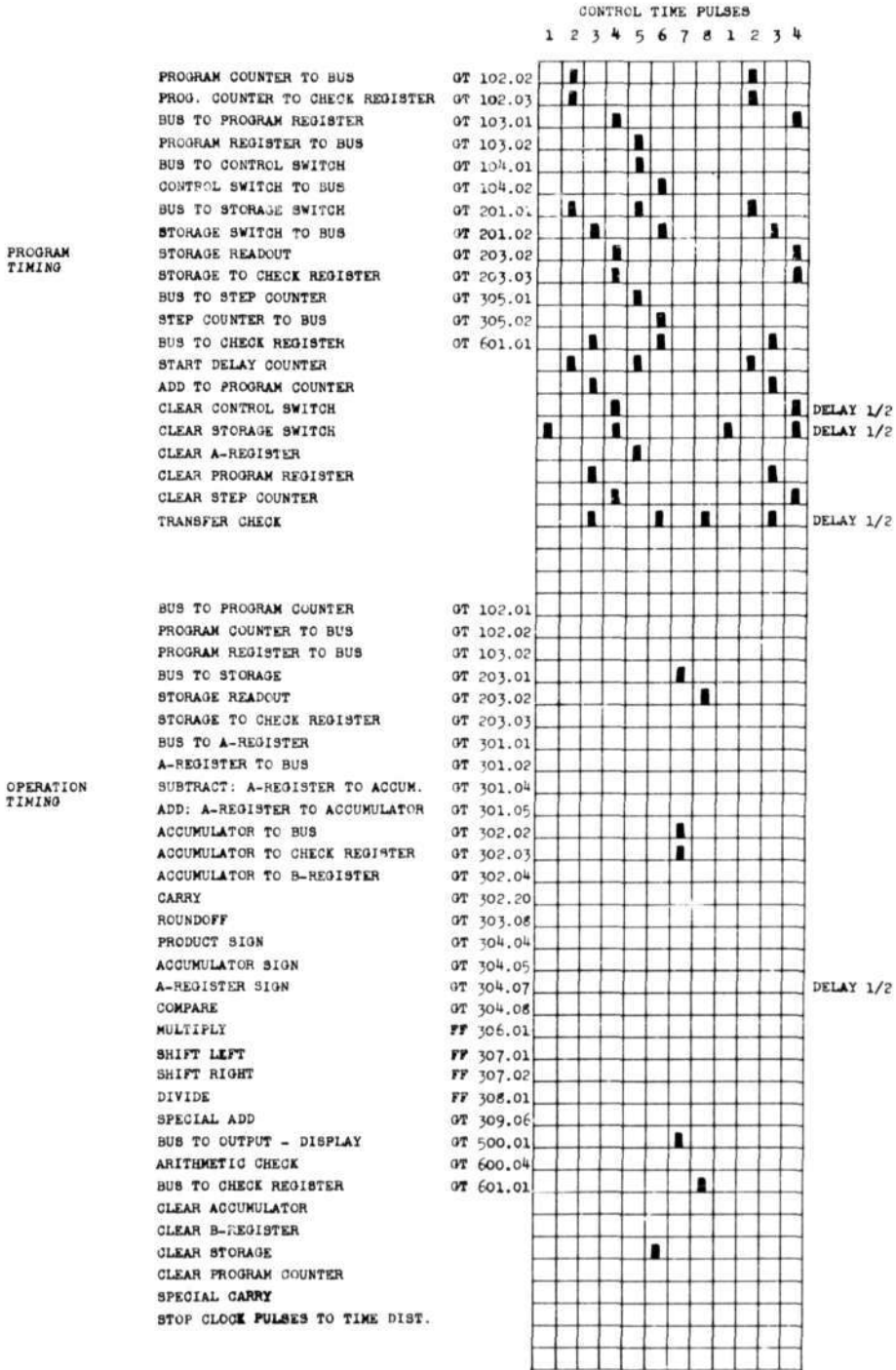


Figure 86

TIMING FOR STORE AND DISPLAY

APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

UNIT CODE NUMBERS

100 Control

101 Master Clock
102 Program Counter
103 Program Register
104 Control Switch
105 Operation Matrix
106 Time Pulse Distributor
107 Operation Timing Matrix
108 Program Timing Matrix
109 Repeat Switch - (Removed from System)

200 Storage

201 Switch
202 Toggle Switch Storage
203 Flip Flop Storage

300 Arithmetic Element

301 A-Register
302 Accumulator
303 B-Register
304 Sign Control
305 Step Counter
306 Multiply
307 Shift
308 Divide

400 Input

500 Output

600 Checking

601 Check Register

LETTER SYMBOLS

AC Accumulator
BA Buffer Amplifier
BC Binary Coder
BD Bus Driver
DE Delay Element
ES Electronic Switch
FD Frequency Divider
FF Flip Flop
GT Gate Tube Circuit
IC Intensity Control Circuit
PF Pulse Forming Circuit
ST Storage Tube
TG Trigger Pulse Generator
TP Timing Pulse Generator
TT Trigger Tube

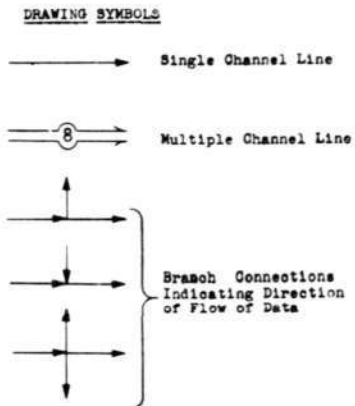


Figure 87
PARALLEL DIGIT COMPUTER CODES