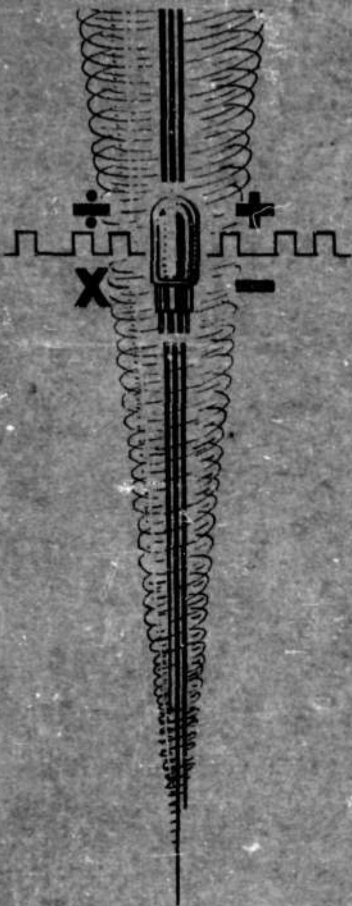

PROJECT
WHIRLWIND
Contract N5ori60

SUMMARY REPORT NO. 2

VOLUME 7

BLOCK DIAGRAMS
(PART III)

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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DEPARTMENT OF THE NAVY
OFFICE OF NAVAL RESEARCH

SPECIAL DEVICES CENTER

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PROJECT WHIRLWIND
Summary Report No. [illegible]
November, 194[illegible]

BLOCK DIAGRAMS, PART III

Volume V of 22 Volumes

Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

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INTRODUCTION

Work was begun on block diagrams for a digital computer in February, 1946. At that time the project was considering the use of a high-speed erasable storage using serially-read electrostatic storage tubes plus some photo-electric card readers for storing and reading orders and constants and tables of functions. Studies were therefore made of a serial-type computer. Since high operating speeds were required for the solution of the airplane problem, a three-address code was proposed, allowing setting up storage elements in parallel and a full high-speed whiffletree-type multiplier was proposed with non-cyclic operation resulting in a multiplication time of about 100 microseconds. Since this speed was still not great enough for complete solution of the airplane problem, it was proposed to build two computers; one of which would be used solely for interpolation, while the other would be used for the numerical calculations. A study was made of this system by Everett, Rider, and Tilton. One of the proposals is discussed in E-24 by Peter D. Tilton.

In the fall of 1946 it was decided that an electrostatic storage tube could be developed which could be used in a parallel-digit transmission system. It was further decided that if such a system was used it would be possible to solve the entire airplane problem with a single computer and yet to have greater flexibility and simplicity than the serial computer considered before. Detailed block diagrams were made for this system and are described in Vols. 5 and 6 of this report. Omitted from Vols. 5 and 6 is any discussion of the electrostatic storage control, the input and output to the computer, a large part of the checking, the control desk, and certain of the additional orders. The input and output devices are described in the reports of Vols. 11 and 12. A proposed set of block diagrams for using these devices is presented in M-158 in this Volume. A tentative proposal is also given for electrostatic storage control in M-135. The computer equipment required for the additional orders is discussed in Memoranda M-111 and M-123. Some of the checking problems are also considered in M-127 and M-161, while some comments on the control desk by Jay W. Forrester are given in M-117.

As an indication of the flexibility of the system, M-136 describes how a modification could be made to allow automatic accumulation of products in the Whirlwind Computer. This modification could be made even after the computer is built and running. Some comments are made in M-134 on how alphabetical in information could be handled in the Whirlwind Computer.

M-137 discusses the code proposed for Whirlwind I in somewhat more detail than is given in Vol. 5. A comparison is also made in this Memorandum between the code proposed for Whirlwind I and the code proposed by the Institute for Advanced Study for their digital computer.

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Memorandum M - 137

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: COMPUTER CODES FOR WHIRLWIND I

To: Jay W. Forrester

From: Robert R. Everett

Date: November 4, 1947

1. INTRODUCTION

The first fifteen orders for the code proposed for Whirlwind I are described in detail in the Block Diagram Report, R-127. The basic reasons for choosing this type of code are not discussed in any great detail in this Report. It is the purpose of this memorandum to consider the basic problems of code selection and compare the code chosen for Whirlwind I with those codes chosen by other computer groups, particularly that chosen by the Institute for Advanced Study.

By computer codes is meant the group of orders or elementary operations built into the machine and available to the operator for instructing the machine in the solution of a problem.

2. SELECTION OF A CODE

First I would like to quote a paragraph used in the Institute for Advanced Study Report entitled, "Preliminary Discussion for the Logical Design of an Electronic Computing Instrument", paragraph 3.1, page 4:

"It is easy to see by formal logical methods, that there exist codes that are in abstracto adequate to control and cause the execution of any sequence of operations which are individually available in the machine and which are, in their entirety, conceivable by the problem planner. The really decisive considerations from the present point of view, in selecting a code, are more of a practical nature: simplicity of the equipment demanded by the code, and the clarity of its application to actually important problems together with the speed of its handling of those problems."

It is possible to perform any of the arithmetic operations using only very simple orders, such as: the ability to examine a single digit to determine if it is a 0 or a 1, and the ability to create or destroy digits.

With these operations only we can add or subtract, and using the additions and subtractions we can multiply, divide, and carry out all the other operations desired for a machine of this type. The problem then is not one of discovering whether or not we can devise a code adequate for our purposes, but rather how good a code we can devise in view of our own particular problems. The basic conflict then is between cost and the ease and rapidity with which the machine can be used. By cost, I mean not only monetary cost but the limitations of space and weight, the complexity of the equipment with resulting trouble shooting and maintenance difficulties, and possible set-up complexity requiring highly trained operators. This conflict between cost and performance is inevitable in any kind of design work. The resulting design must be an engineering compromise.

It is first necessary to discover what would be desired as a code and then to compare it with what is readily available. In particular, the operations which would facilitate the solution of the kinds of problems in which we are most interested, must be discovered. There is no such thing as a completly general-purpose machine. The computing machines have not reached the stage of speed and flexibility where they can be said to handle satisfactorily all types of problems. Instead, the computers are intended for specific classes of problems. These classes are very large, to be sure, compared with what has been possible in the past and the computers are able also to handle with less efficiency problems outside their specific design classes but the fact remains that the computer must be designed with certain specific requirements in mind. These requirements are dictated by the kinds of problems to be encountered.

Going beyond then the simple logical operations mentioned above, we can state that almost all classes of problems require large numbers of the arithmetic operations of addition, subtraction and multiplication. For this reason, it is desirable to build in these operations even though the amount of the equipment required may be considerable. We also basically require the ability to examine a digit of a word in the computer and to order the further operation of the computer according to the condition of this digit.

Beyond these simple operations is a second category which would be desirable in almost any case and which will be built in if the amount of equipment required is not excessive. Among these operations are; transferring data from one part of the computer to another without arithmetic operations, absolute as well as conditional transferance of control, the shifting of information within the computer without requiring multiplication and transferring parts of a word without requiring a lengthy shifting operation. These operations are sufficiently valuable and used sufficiently often to warrant their inclusion although they can be fairly readily made up of the simpler operations. In fact, the very readiness with which they can be made up indicates the simplicity of the additional equipment needed for their automatic accomplishment.

Then there is a third category containing operations of a more special nature whose general value is not so immediately apparent. Once again it is possible to make up these operations from the simpler ones; the question is shall they be made automatic. Among these operations are others such as addition and subtraction using the absolute values of numbers, division, and square root which would be included only if they were either very easy to add or if the problems under particular consideration require them in such quantities as to make economic their inclusion. Among these operations are still others which would not be included at all unless the particular problems required them.

It so happens then that the first two categories involved are decided without regard to the mathematical problems involved; the first category, arithmetic operations, because it would be included anyway, and the second category, convenient operations, because of its general value and the ease with which it can be added to the computer. It also happens that the third category, special operations, tends to be decided according to the cost in machine complexity unless the need for them in special problems is immediately apparent.

3. BASIC CODES.

Orders in general consist of an instructional operation code plus the positions or addresses of one or more of the words in the storage. Orders are called single or multiple address orders depending on whether there are one or more references to storage for each operation.

The choice of the number of addresses to be used in the order is once again largely dependent on the physical nature of the machine. Since most arithmetic operations require three numbers, two of which are combined in some fashion to form the third, a three address code might at first be thought best, since two of the addresses could be for the two original numbers and the third address for the disposal of the result. However, many times only one or two of the addresses are required resulting in considerable waste of order storage. The address position of a single address code is almost always used thus making it somewhat more efficient, particularly as it is not necessary to store the results of operations if they are to be used again immediately. Four address codes are also useful. The fourth address can be used to select the next order to be performed; thus it is no longer necessary to store the orders in approximate linear sequence in the machine and considerable numbers of transfers using the sub-program operations are avoided. However, all these considerations are secondary.

In the first place the single address code requires the simplest kind of equipment since only one elementary operation is being carried on at a time. The effective use of a triple address code requires considerable duplication of control equipment. In the case of a parallel type machine such as Whirlwind the increase in control equipment would be considerable and the saving in time small. In the case of serial type machines where the time required to extract information from storage is long, the use of a multiple address code allows these extractions to be carried out in parallel with a considerable saving in time. For this reason a multiple address code was selected for the early serial computer investigation of Project Whirlwind and has also been selected for some of the EDVAC type machines.

There is another important consideration, however, and that is word length. The length of an address is fixed by the memory capacity of the machine and is of the order of ten to fifteen binary digits. A triple address code is thus of the order of 50 binary digits in length. Thirty to forty binary digits are usually considered adequate for most types of computing. If the word length is made 50 or more digits long just to accomodate the length of an order, there is a considerable wastage both of memory capacity and quipment. If, however, the order is cut in two parts or stored in two words, each part need only be about 25 digits which is now too short for most computing purposes. Therefore, when multiple address codes are considered the four address code exhibits the advantage of nicely filling two word lengths of an ordinary computer. Although the triple address code was used in the coding investigations carried out in the serial computer study of the Whirlwind Program a four address code or a modification of it was proposed for the actual machine. At the moment there seems to be no advantage in using a two address code or in using more than four addresses. Both the Whirlwind and Institute for Advance Study machines use a single address code as is best suited to their basic system which is to perform operations in series while handling digit columns in parallel. Two complete single address orders fit easily through a single word length of a machine such as Whirlwind II or the Institute for Advance Study Machine while a single address order was used to determine the word length for Whirlwind I.

There are other possible modifications such as an early EDVAC code which filled a full word length with a single address order and included space for such information as the number of transfers to be performed. The Naval Ordnance Laboratory machines proposed providing space for "stop orders" which were indices carried along with orders to facilitate keeping track of inductive processes.

The selection of a fixed or floating point system has considerable effect upon the code to be used. In order to facilitate certain operations it is desirable to have a fixed point system available. If a floating point system is desired for ease of setup then usually both fixed and floating point systems must be provided. It has been decided that the Whirlwind machine and most of the other proposed machines use a fixed point system only because it has not been felt that any simplicity gained by the floating point in setup is warranted by the extra complication and loss of speed of the computer.

The procedure for handling signs also has an effect upon the code. The particular convention used has no effect when elementary arithmetic operations are considered but has considerable effect when multiple length number operations are carried out or when the digital character of the numbers are considered as in comparisons in conversions of one base system to another. A 9's complement system was chosen for the Whirlwind I Computer because of the simplicity obtained thereby in the arithmetic element although the tens complements system is used by the Institute for Advanced Study appears to result in occasional coding simplicity.

The rounding procedure used also has a considerable effect upon the code selected. In general during ordinary arithmetic computation, it is desirable to round off numbers as carefully as possible. When the digital characters of the numbers is considered it is desirable not to round off the numbers. There are 3 possibilities. The first is to round off whenever desirable from the point of view of arithmetic and to accept the resulting complications of the coding when other types of problems are considered. The second is not to round off at all, either accepting the resulting error or rounding off when desired by application of the elementary operations. The third possibility is to duplicate orders for rounding off or not rounding off accepting the cost in machine complication for ease in coding. The Whirlwind machine uses a combination of the first and third method. Since the problems for which it is intended, in particular simulator and other physical problems, are arithmetic in nature, rounding off is performed whenever desirable. In some instances special orders are provided to avoid rounding off, in particular to facilitate operations with multiple length numbers. These points will be made clear in the paragraph below.

4. THE INSTITUTE FOR ADVANCE STUDY AND WHIRLWIND CODES

The IAS and WW machines are physically very similar as dictated by the similarity of their storage devices. Their differences lie in the extra complication of the Whirlwind machine added to obtain the very high computing speed required for the problems considered for Whirlwind. Since their physical natures are very similar and their physical natures have a very great effect upon the codes as shown above, the codes proposed for the IAS and WW machines are also very similar. These codes are given below and compared and discussed in detail. I shall first give a short summary of the major differences between these two codes.

SUMMARY OF THE DIFFERENCES BETWEEN THE IAS AND WW CODES.

1. There is no appreciable difference between the orders required for addition and subtraction.

2. In multiplication the Whirlwind machine multiplies the number selected by the order by the contents of the accumulator in the arithmetic element and leaves the product in this accumulator. It is thus possible to perform repeated multiplications without restoring the products at each step. The IAS machine multiplies the number selected by the order by the number which is in the shifting register of the arithmetic element and leaves the product in the accumulator. The only path between the accumulator and the shifting register is via the storage thus requiring a transfer omitted in the Whirlwind machine if repeated multiplications are to be carried out.

3. The Whirlwind code provides two orders for multiplication one of which includes rounding off and one of which does not. The IAS code has but one order which always rounds off the product but leaves an indication so that the rounding can be cleared later if desired.

4. In division the remainder is cleared from the accumulator in the Whirlwind code and is left in the accumulator in the IAS code.

5. Since there is but one order per word in the Whirlwind machine as compared to two orders per word in the IAS machine only half as many control modification orders are required.

6. The shift orders in the IAS code cause the accumulator in the arithmetic element to be stepped but one space to the right or left for each shift order. In the Whirlwind code shifts up to the full length of the accumulator can be ordered by a single order.

7. There are also some special orders provided in the Whirlwind code for facilitating operations with multiple length numbers. This facility is desirable in Whirlwind I because of its short register lengths.

8. Since data is not available no comparison is given between the input and output orders proposed for the two machines.

The detailed comparison of the codes now follows:

Order Number	Code	Symbol	Description
1	IAS		Clear accumulator and add number located at position x in the selectrons into it.
	WWI	ca	Clear and add. Clear AC and add the contents of register x into it.

These two orders are identical as far as the operator is concerned.

Order Number	Code	Symbol	Description
2	IAS	-	Clear accumulator and substract number located at position x in the selectron into it.
	WWI	cs	Clear and substract. Clear AC and substract the contents of register x into it.

These two orders are identical as far as the operator is concerned.

Order Number	Code	Symbol	Description
3	IAS	M	Clear accumulator and add absolute value of number located at position x in the selectron into it.
	WWI	cm	Clear and add magnitude. Clear AC and add the absolute magnitude of the number in register x into it.

These two orders are identical as far as the operator is concerned. The absolute value operations are not described in R-127.

Order Number	Code	Symbol	Description
4	IAS	M	Clear accumulator and substract the number located in position x into it.
	WWI	nm	Negative Magnitude clear AC and substract the absolute magnitude of the number in register x into it.

These two orders are identical as far as the operator is concerned.

Order Number	Code	Symbol	Description
5	IAS	h	Add number located at position x in the selectron into the accumulator.
	WWI	ad	Add. Add the contents of register x to whatever is in AC.

These two orders are identical as far as the operator is concerned.

Order Number	Code	Symbol	Description
6	IAS	h-	Substract number located at position x in the selectron into the accumulator.
	WWI	su	Substract. Substract the contents of register x from whatever is already in AC.

These two orders are also identical as far as the operator is concerned.

Order Number	Code	Symbol	Description
7	IAS	HM	Add absolute value of number located at position x in the selectron into the accumulator.
	WWI	am	Add magnitude. Add the absolute value of the number in register x to whatever is already in AC.

These two orders are also identical as far as the operator is concerned.

Order Number	Code	Symbol	Description
8	IAS	h-M	Substract absolute value of number located in position x in the selectron into the accumulator.
	WWI	sm	Substract magnitude. Substract the absolute value of the number in register x from whatever is already in AC.

These two orders are also identical as far as the operator is concerned.

9	IAS	R	Clear register and add number located at position x in the selectron into it.

There is no counterpart to this order in the Whirlwind code. The register mentioned is equivalent to Whirlwind B- Register. In the IAS Code this order is necessary prior to a multiplication.

10	IAS	A	Clear accumulator and shift number held in register into it.

There is no counterpart to this order in the Whirlwind Code. Whenever it is desired to shift the number in the B-Register into the accumulator the regular shift left operation is used.

11	IAS	X	Clear accumulator and multiply the number located at position x in the selectrons by the number in the register, placing the left hand 39 digits of the answer in the accumulator and the right hand 39 digits of the answer in the register. The sign digit of the register is to be made equal to the extreme left (non-sign) digit. If the latter is 1, then 2-39 is to be added into the accumulator.
	WWI	mr	Multiply and round off. Multiply the contents of register x by whatever is in AC and round off the result to one register length.

This is the first important difference between the IAS and Whirlwind code. Since the multiplier is originally in the accumulator in the Whirlwind code, order 9 described above is not needed. Since the product also appears in the accumulator successive multiplications can be carried out without transferring the product into the memory at each step. In the Whirlwind operation the product is rounded off and the contents of the B register are cleared. If, then, it is desired to retain the less significant half of the product, a special order described below is needed. In the IAS order not only is the less significant half of the product retained, but an indication is left in the sign digit position in the register so that the rounding can be cleared if desired. The IAS order is perfectly complete as far as allowing double length multiplication operations, but is less convenient if many of them are to be performed as is the case in Whirlwind I.

11	WWI	mh	Multiply and hold full product. Multiply the contents of register x by whatever is an AC but do not round off.

This is the order mentioned in the paragraph above.

12	IAS	÷	Clear register and divide the number in the accumulator by the number located by position x of the selectron, leaving the remainder in the accumulator and placing the quotient in the register.
	WWI	dv	Divide. Divide the contents of AC by whatever is in the register x.

Although the two orders are superficially alike there are two differences. In the IAS code the quotient is rounded automatically, while in the Whirlwind code the rounding is not performed until the quotient is shifted into the accumulator. Secondly, the remainder is retained in the IAS code and is cleared from the accumulator in the Whirlwind code. This is as a shortcoming of the Whirlwind code and is due to the particular way in which the division is accomplished within the machine. I do not feel that the result is serious.

13	IAS	C	Shift the control to the left hand order of the order pair located at position x in the selectron.
	WWI	sp	Sub-program. Transfer the register number x to the program counter.

These orders are identical as far as the operator is concerned except that since there is only one order per word in the Whirlwind machine it is not necessary to designate which half of the word is to be used.

14	IAS	C	Shift the control to the right hand order of the order pair located at position x in the selectron. There is no counterpart to this order in the Whirlwind code. Since WWI has but one order to a word.

Order Number	Code	Symbol	Description
15	IAS	cc	If the number in the accumulator is ≷ 0 shift the control as in order 13.
	WWI	cp	Conditional program. Transfer the register number x to the program counter if the number in AC is greater than zero.

There are two differences between these orders, the first is the one mentioned above that since there is only one order per word in the Whirlwind machine it is not necessary to designate which half of the word is to be used. The second is that since the Whirlwind machine used 9's complements while the IAS machine used 10's complements, zero has a zero sign digit in the IAS machine while it has a 1 sign digit in the Whirlwind machine. Zero is thus allocated to the positive numbers in the IAS machine and the control is shifted for a zero number, while in the Whirlwind machine zero is allocated to the negative numbers and the control is not shifted.

16	IAS	Cc	If the number in the accumulator is ≷0 shift the control as in order 14.

There is no counterpart to this order in the Whirlwind machine since there is only one order per word.

17	IAS	S	Transfer the number in the accumulator to position x in the selectron.
	WWI	ts	Transfer to storage. Transfer the contents of AC to register x .

These two orders are identical as far as the operator is concerned.

18	IAS	Sp	Replace the left-hand 12 digits of the left-hand order located at position x by the 12 digits 9 to 20 from the left in the accumulator.
	WWI	td	Transfer digits. Transfer the left-hand 11 digits in AC to the register position section of the order in x.

The difference here lies, first, as usual, in the number of orders per word and also in the selection of which digits in AC are to be transferred to the storage stored order. At present the WWI code states that the left-hand 11 digits in AC are to be transferred. This digit selection is not entirely satisfactory since the first digit is also the sign digit which puts certain limitations on arithmetic operations performed on the numbers to be transferred. The digit selection will therefore be changed, but it is not yet known what the final choice will be. The decision is not needed in the design until the final cabling diagrams are made.

Order Number	Code	Symbol	Description
19	IAS	SP	Replace the left hand 12 digits of th right hand order located at position x by the 12 digits 29 to 40 from the left in the accumulator.

There is no counterpart to this order in the Whirlwind code because there is but one order per word.

Order Number	Code	Symbol	Description
20	IAS	R	Replace the contents $E_0\ E_1\ E_2 \ldots E_{38}\ E_{39}$ of the accumulator by $E_0\ E_0\ E_1 \ldots E_{37}\ E_{38}$.
	WWI	sr	Shift right. Shift the contents of AC and BR to the right the number of digits designated by the number in the register number section of the order.

There are two differences between these orders. First the Whirlwind order allows shifting by as many digits as desired as compared to the IAS order which allows shifting by only one digit at a time. Secondly, the contents of AC are rounded off in the Whirlwind I order and are not rounded in the IAS order. The sign handling methods are the same.

Order Number	Code	Symbol	Description
21	IAS	L	Replace the contents $E_0\ E_1\ E_2 \ldots E_{38}\ E_{39}$ and $N_0\ N_1\ N_2 \ldots N_{38}\ N_{39}$ of the accumulator in the register, by $E_0\ E_2\ E_3 \ldots E_{39}\ 0$ and $N_1\ N_2\ N_3 \ldots E_{39}\ E_1$.
	WWI	sl	Shift left. Shift the contents of AC and DR to the left the number of digits designated by the number of the register number section of the order.

There are again two differences between these orders. The Whirlwind order allows shifting by any desired number of digits while the IAS order allows shifting only by one digit at a time. Secondly, the digits of the register are shifted into the accumulator and the result rounded off in the Whirlwind order while there is no round off in the IAS order. The sign handling methods are the same. However, in the IAS order the digits shifted off the left hand end of the accumulator are saved in the B register, while they are completely discarded in the Whirlwind order.

These orders are the only ones available for the IAS code that have been reported to us to date. Below are described some further orders proposed for Whirlwind I.

Order Number	Code	Symbol	Description
	WWI	sa	Special add. Add as in ad but retain any overflow for use in double length number position.

This order allows a complete double length addition to be performed in 6 orders while more than this number of orders is required in the IAS code without modification.

This additional order seems to be warranted in the case of Whirlwind I, first because of its short register length, and second because the handling of double length numbers is more complicated in 9's complement than in 10's complement.

WWI	as	Automatic sub-program. Put the contents of AC in BR. Put the contents of register x in AC.

This order is the preliminary step to the automatic sub-program operations discussed in M-123.

WWI	ax, ay, az	These are the three automatic sub-programs to be alloted in Whirlwind I.
WWI	sd	Store and display. Transfer the contents of AC to register x and also to the output element.

This is a very simple output order to be provided in Whirlwind I for use in test storage only. The more complicated special output orders have not yet been described in detail.

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5. CODING CHANGES FOR WHIRLWIND I.

The control of Whirlwind I is so designed that changes in the code, such as changing round off procedures or retention of digits in shifts or multiplications can be readily made at any time even after the machine is operating. If it is discovered later on that certain of the minor differences between the Whirlwind I and IAS code occasioned by decisions made in the light of the arithmetic problems proposed for Whirlwind I should be adjusted, they can be changed readily without serious physical change in the computer itself.

It is also possible to use some of the spare order positions left in the control order to set up modified additional orders while retaining the original ones.

Robert R. Everett
Robert R. Everett

RRE:hcs

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6345
Memorandum M-134

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: ALPHABETICAL INFORMATION IN WHIRLWIND COMPUTERS

To: Jay. W. Forrester

From: R. R. Everett

Date: November 13, 1947

The following comments have been prepared hurriedly in response to a Bureau of Standards request for information. Improved methods of handling alphabetical information could be worked out if more time were available.

1. There is nothing that prevents the insertion of alphabetic data into a binary machine such as WHIRLWIND. The twenty-six characters of the alphabet plus the few extra which are needed for certain kinds of punctuation and markers can be written in a base thirty-two system which requires five binary digits. The information may be inserted in the computer in this binary coded base thirty-two system. Five binary digits are needed for each letter; thus, three letters could be stored in the sixteen digit word length of WHIRLWIND I with one digit left over for a marker. WHIRLWIND II could store about eight alphabetic characters per word. Since either three or eight characters is insufficient for most alphabetic data, particularly names, the actual alphabetic words would have to be broken up into several registers in the computer. There are several possibilities for handling this:

a. Assign for each alphabetic element a certain number of registers large enough to contain the largest possible case. This system is probably too inefficient to be very useful.

b. Transmit, probably first, a register telling how many words are required to contain the following alphabetic information. The computer can use this information as an induction index to keep track of the alphabetic processes.

c. Use the digit left over in WHIRLWIND I or an equivalent digit in other computers as a marker. The first word, by word I mean computer word, in the alphabetic sequence could have a zero sign digit or marker. From then on, all words coming along with sign digits equal to one would be understood to be part of that alphabetic information. The next time that a zero sign digit appears the computer would know that a new alphabetic word had appeared. The computer can handle this problem easily because of the conditional sub-program operations.

A typewriter or teletype style of keyboard would replace the ten-digit decimal keyboard. Each key punched could, probably through a matrix switch, provide the five-digit binary code equivalent to it. These codes would be inserted in the keyboard register in sequence without conversion since it is desired to keep the information in base thirty-two.

It is desirable to have at least some punctuation marks since alphabetic information may consist of a number of parts; for instance a man's surname, followed by his given name, followed by his middle name. It is desirable to separate these sections, since in a comparison for alphabetic order, the first initial of a man's given name has a different meaning than if it were a corresponding last digit in his surname. In this case, a comma given a base thirty-two notation which is greater than any of the alphabetic numbers could be inserted between the surname and given name, giving the desired result. Also, it will be necessary to attach base thirty-two numbers to the alphabetic characters in descending order such that A will be the largest and Z the smallest numerically. The alternative is also possible of attaching numbers in increasing order instead of decreasing. In this case the comma should be smaller numerically than any of the alphabetic numbers.

2. I cannot see where it would be desirable to perform any arithmetic operations on the alphabetic data within the computer, since, in general, words and names have no quantitative meaning. The only operation I can see of value is the comparison operation; that is, the choice of whether or not two names or numbers are alike and, if they are not alike, which comes sooner in an alphabetic sorting. It is true that alphabetic order is obtained by assigning numerical meanings to the alphabetic characters but this is done merely for convenience in reference and does not mean there is any logical meaning to the sequence except in the particular case mentioned above of identity or equality between words or parts of words.

For instance, in examining a sequence of names, each one of which is represented in the surname, given name, middle name order, two names may be considered as belonging to the same person only if they are identical in all parts. However, two names can be considered as belonging at least to the same general family if only the first part of their alphabetic information, that is, their surnames, are alike.

The ability to compare two numbers written in binary code but in any base is already available within the Whirlwind machine. The difference between these two numbers will be arithmetically correct only if the numbers are truly binary, but will have the proper sign in any case.

This remark requires some clarification. First, by a number written in binary code but not in base 2, I mean that each digit of the original number is written in binary code, but not the whole number. For instance, in base 10, the first digit of the decimal number may be written in binary code requiring 4 binary digits. The second digit may also be so written requiring 4 more binary digits. If this process is continued, the result will be a binary coded decimal number requiring 4 n binary digits where n is the number of decimal digits in the original number. Now several things are apparent. Since four binary digits permit 16 possibilities and we are only using 10 of these, there are unused gaps in the resulting number. The number is thus not truly binary. If the base we are using happens to be a power of two as proposed above, then all the possibilities would be used and the number would be indistinquishable from a truly binary number; in fact, it would be truly binary. Our binary coded number has a distinct meaning as long as we know the process by which it was obtained. Any arithmetic operations on this number will also have to take this process into account.

Now, to see that the result of a subtraction involving binary coded numbers with non-binary bases will have at least the proper sign, consider the three possible cases:

a. The numbers are equal. If so, they are also equal if considered as truly binary numbers and will thus exhibit the configuration and sign associated with zero in the machine when subtracted.

b. The first is larger than the second. Consider the subtraction as being carried out in groups corresponding to the binary digits of the original number. Starting at the left a number of these groups may be equal, but eventually we will come to group in which the minuend is larger than the subtrahend. The difference in this group will be a positive binary number. Furthermore, since the smallest digit in this group has a greater significance than the sum of all digits to the right considered in binary or any other base, the result of subtracting groups to the right cannot affect the sign of this difference. The size of this group and the meaning of the result can be affected, but the sign will remain and it is the sign we are after. The subtraction can be thought of simply as a comparison process where the result can be obtained by examining the first unequal pair of digits starting from the left.

c. The second is larger than the first. This case is the same as b. except the signs are reversed.

Note that if base 32 is used for alphabetic representation the result of the binary subtraction will be arithmetically correct although meaningless.

An example is given below of the comparison by subtraction of two alphabetic names written in binary code. The code used is an ascending one with A=0, B=1, etc. Subtractions in the machine are carried out by complements but are done here directly for simplicity. The selection process for determining identity is omitted; the purpose of the example is simply to illustrate that the difference has the proper sign. The subtractions performed are truly binary and the magnitudes of the differences are alphabetically meaningless.

ADAMS=	0.00000	00011	00000	01100	10010
- ADLER=	0.00000	00011	01011	00100	10001
	1.11111	11111	10101	01000	00001

The result is negative; therefore ADAMS come before ADLER.

ADAMS=	0.00000	00011	00000	01100	10010
- ABORN=	0.00000	00001	01110	10001	01101
	0.00000	00001	10001	11011	00101

The result is positive; therefore ADAMS come after ABORN.

Since we are discriminating only on the sign of the result the binary subtraction is adequate. For example, if two names, considered temporarily as having the same number of alphabetic characters, are represented as suggested in paragraph 1 above and are subtracted one from the other with a positive difference as evidenced by a zero sign digit, then we know immediately that the first was greater. If the difference were negative or zero as represented by a one sign digit then we know that either the second name is greater or the two names are identical. By greater I mean comes sooner in an alphabetic sorting. Now if the latter case obtains we can determine if the two names are identical by a process equivalent to that used for determining the equality of two binary numbers. If a 1, that is, the smallest possible increment, is added in the right-most place to the difference, the difference will change sign if, and only if, it is zero. We can thus determine identity.

If we are comparing two names consisting of several parts, for instance surname and given name, we can examine for identical surname by first subtracting one from the other. In the check for identity, however, instead of adding the test one in the right-most place we will add it in the right-most part of those sections we are comparing, for instance, in the right-most digit of the surname part only of the words being compared. By shifting it is possible to put second or third parts of the alphabetic information in the first part section and to compare on the basis of these, having discarded the first part. Using these methods it is possible to take a string of random names and put them in alphabetic sequence or to sort through a sequence of alphabetic names correlating them according to the identity of given names or surnames, or middle names, or initials, or any other criterion desired.

3. The problem is complicated somewhat if numerical data is carried along with the alphabetic data. This problem is of considerable importance, however, for in general the alphabetic data will be in the form of names or tags or position marks along with which are carried pertinent numerical information. Once again it is necessary to set up some sort of a convention or criterion for handling this problem. If, for instance, the extra digit in Whirlwind I were used as suggested above for marking the beginnings or ends of alphabetic words requiring more than one register length in the computer, the convention might be added that information appeared only in pairs of which the first section was alphabetic and the second section numerical. It will in general be possible to assign a fixed number of register lengths to the numerical information since the range of numerical data for a given quantity is usually considerably less than the range of alphabetic data considered as numerical. This difference is due not to a preponderence of alphabetic words over numerical possibilities

but rather to the greater efficiency of numbers as compared to the written equivalent of spoken language. In any event it should be possible to dissociate the alphabetic and numerical parts of the information being handled either by index marks carried along with the information or by standard conventions. In particular, once the numerical part of the information has been extracted the problem of applying conventions is really no greater than that customarily met in ordinary computations.

Since the kinds of operations to be performed on alphabetic data appear to be very limited it should be possible to code most of them once and for all, the coding being simple enough not to present any particular problems if done infrequently. The use of sub-programs should also facilitate the construction of special coding sequences. The high speed and large storage capacity of Whirlwind computers would permit fast handling of alphabetical information. Several input tapes could be controlled simultaneously and the internal storage could be used for arranging blocks of information in order before reading to the output.

4. The output printers for the actual printing of the numerical results have not yet been given any consideration for Whirlwind. In all likelihood, however, these printers should be able to print alphabetic information as well in the form of headings, groupings, and special notes. The printers, therefore, must be able to decipher alphabetic information probably appearing as codes on film. If the printers are made to recognize alphabetic information given in base 32 coded binary such as is proposed for the handling of alphabetic information in the computer, they can be used essentially without modification for printing alphabetic information received from the computer. It will be necessary for the printer to discriminate between alphabetic and numerical information. I would suggest for this purpose that one of the spare channels on the film be used.

5. If large amounts of alphabetic information are to be handled, our presently proposed film input and output methods will probably not be satisfactory because of the large amounts of film required and the difficulty of processing. Particularly in certain types of sorting and collating processes where the total body of information must be transferred many times, an erasible output medium would be a great help. The presently proposed equipment should be satisfactory for handling small quantities of alphabetic information in occasional problems. If the machine is to be used for large problems of this type, as for instance in census work, an erasible output medium, probably magnetic tape, should be developed if not already available from other sources. The required modifications within the computer itself should not be serious.

Robert R. Everett

RRE:bb Robert R. Everett

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Memorandum M-111

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BLOCK DIAGRAM WORK

To: H. Fahnestock

From: R. R. Everett

Date: October 6, 1947

This memorandum is in response to your request made at a conference with Sylvania on Friday, September 12. It is an attempt to list the present objectives of block diagram work and to define the expected results of that work in sufficient detail to allow estimating its effect on Whirlwind I computer design.

I hope in the near future to produce concrete diagrams and timing studies, accurately defining these matters. This work will be greatly expedited by the return of P. E. Swain who is expected early this month. I would appreciate comments of any sort on the work, particularly on the order in which the different problems should be studied in order to best meet project needs.

SUMMARY: The block diagrams distributed to date and described in R-127 (expected publication date October 15) describe the elements of a working computer. The control and arithmetic element are essentially complete as they stand. The storage described is the test storage proposed for Whirlwind I. The input and output devices described are only those needed for this test storage. Before the block diagrams can be considered complete for Whirlwind I, the following work must be done.

1) The effects of adding electrostatic storage must be examined.

2) The input and output devices needed in order to use Whirlwind I with electrostatic storage at all efficiently must be described in fair detail.

3) Further work must be done on checking. This work should include specifying not only additional equipment required for continuously checking computer elements but also more or less complete analyses of all the checking methods to be used for determining and isolating failures. This latter information can

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be used for determining trouble-shooting procedures and necessary equipment as well as for discovering the information which must be brought from the computer to the control desk.

4) The additional orders required in the code must be fully investigated.

5) More exact methods and timing must be determined for generating restorer pulses for a c coupling.

These problems are discussed in the latter part of this memorandum.

The expected effects on Whirlwind I design are:

1) The requirement of a fair number of gate tubes and matrix space in the control beyond that now defined. This provision is, I believe, being made but should be adequate for additions beyond those conceived at present.

2) The possible addition of a special register for storing program counter numbers during automatic subprograms. It may be possible to avoid the use of this register. A study of this problem could probably be made in a few days if worthwhile at this time.

3) Modifications to the program counter to allow up to three special pre-set numbers. The problem is the same as that presented by pre-setting the step counter.

4) The design of a control for electrostatic storage. Although the necessary information for a final design is not available, an approximate design could now be made.

5) Design of shifting registers for input and output devices. These must be designed eventually and provision must be made for connecting them to the bus. Control cables to the registers and to the film devices themselves are needed.

6) Design of counter controls for storage buffers between computer and input and output devices as well as counters for film position. The same comments hold as for 5.

7) Modification of the step counter to provide restorer pulses during lengthy operations.

8) No discussion of checking or control desk problems is given in this memorandum.

ELECTROSTATIC STORAGE CONTROL: The possibility of considerable change and the uncertainty of time requirements have so far prevented any exact description of the electrostatic storage control but a possible sequence of events in using electrostatic storage has been given some consideration. An outline of this sequence and the necessary control equipment is as follows:

There will be 2 banks of 16 electrostatic storage tubes each. Two 32-way switches will be provided, one to set the vertical deflection voltage and the other to set the horizontal deflection voltage. These voltages will be applied simultaneously to all tubes. A 2-way switch will be provided for selecting which of the 2 storage banks is to be used.

On the output of each tube will be a 3-position flip-flop. When this flip-flop is set to its neutral position it will be switched to one position by a positive pulse and to the other by a negative pulse. This flip-flop is connected to the bus by read-in and read-out gates and is also connected to the screen of the storage tube.

The sequence for getting information from the storage is then:

1) Clear all storage flip-flops (i.e., return them to neutral).

2) Transmit the control order to the storage switches.

3) A period of time will be required for the deflection voltages to reach their final values.

4) The screens of the storage tubes will be set to neutral by the storage flip-flops. The beams of the tubes are now turned on. The selected spot will charge up or down depending on whether a 1 or a 0 was stored. The signal coming from the signal plate will thus be positive or negative and when applied to the 3-way flip-flop will change it to one or the other of the non-neutral positions.

The connections from screen to flip-flop are arranged to move the screen to the original potential of the spot charge. It is necessary to keep the screen potential at neutral during the entire reading step. Some sort of corrective delay must therefore be introduced between the signal plate and the screen setting.

The 2-way switch for selecting the bank may be used either to select which beams are to be gated or else to select which flip-flops are to be read onto the bus.

5) The flip-flops are then examined to make sure that none are in the neutral position. A flip-flop in neutral position would

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represent the failure of that particular tube to read out.

6) The row of flip-flops will then be read out onto the main bus and the check bus.

7) The flip-flops remain set to the position corresponding to the original contents of the tubes. The stored signal in the tube has been erased in the reading process. The screens are then set according to the flip-flop settings and the beams again pulsed. The signal will thus be replaced in the tubes.

The outputs from the signal plates during the rewriting procedure will be sent to the flip-flop inputs resetting them to their neutral positions. Examination of the positions of all flip-flops following the restoring will discover if any tube has failed to operate.

At the close of the operation, the original contents of the storage tubes remain. The number has been read out to main bus and check bus and all parts of the operation have been checked.

The use of a holding beam complicates the above sequence. It may be necessary to cut off the holding beam during writing and reading. It will be necessary to keep the screen at some potential other than neutral during the normal holding beam operation. It may even be desirable to provide 2, 3-way flip-flops, one for screen potential and one for the number, connecting them by gate tubes in order to have better control over screen potential.

Storing a number is done in similar manner. Depending on the timing, the old number may be read out, the flip-flops cleared and reset, and the new number stored instead of the old, or the new number may be stored without reading out the old.

Because of the complexity of the sequence and the lack of knowledge of the timing, the control for the electrostatic storage will be a separate entity from the main control of the computer. The control sequence will be inserted in the main timing sequence in the same manner as several of the other operations. In effect this special control sequence will be inserted in place of the delay counter delay. It is doubtful if the overlapping which will be resorted to in the case of Whirlwind II for the purpose of increasing operation speeds will be worthwhile for Whirlwind I.

INPUT AND OUTPUT DEVICES. The input and output devices, which are under development at Eastman Kodak Co., require some special equipment for connecting them to the computer.

A single mechanical housing and film drive design is planned, the device being suited to its particular purpose by differences in the optical and electronic systems. There will also be a separate design for a multiple-element graphical recorder.

DIGITAL INPUTS: The input readers consist of a film drive, a cathode-ray tube and optical system for sweeping a spot of light across the film, and a photocell. The film has stored on it both the number and its complement. The reader reads both number and complement and sends these out serially on a single cable. There is a clutch film drive which can be started or stopped on receipt of an order from the computer.

The computer equipment is as follows:

1). Two registers capable of shifting. The information coming serially from the reader is shifted into the end of the proper register, the number into the number register and the complement into the complement register. Following this shift the number is added to its complement in the complement register. Any reading errors will appear as discrepancies in the sum.

The number may then be read from the number register onto the bus.

2) It is desirable to allow the computer to continue calculations while the film is being read. A possible method of accomplishing this end and at the same time simplifying the ordering process is as follows.

Allocate a section of storage, perhaps 64 registers, to serve as a sort of flexible connecting link between the computer and the tape. Consider this section as a ring. Each new number coming from the tape is put in the first vacant space. Each number taken by the computer is taken from the first full space. Two counters keep track of the positions of these spaces. If the reader has gotten ahead to the extent that the ring is nearly full, a signal will be sent to the film drive to stop. If the ring is empty, the computer will be stopped to allow the reader to catch up.

3) Another counter will be provided for each reader to keep track of film position for use in scanning rather than extracting large blocks of information. Each transfer from the reader registers to storage should be checked. The computer must be stopped while the bus and storage are in use for this purpose.

4) An input typewriter and decimal-to-binary converter

will be attached directly to the bus. A number can be typed in along with the desired storage location. The computer will then stop its standard procedure long enough to store the new information.

<u>DIGITAL OUTPUTS</u>: The output writers are similar to the readers except that the spot of light from the cathode-ray tube is used to expose the raw film in the writer.

The computer equipment is as follows:

1) Two registers of the same type as used with the readers. The number from the bus is sent to these registers, the number being placed in one and its complement in the other. The number is shifted out serially onto a single cable to the writer. The writer records both number and complement, recording 1's in the number lines if the digits shifted in are 1's and 1's in the complement lines if the digits shifted in are 0's.

2) Photocells are provided to determine if the writer has recorded and whether it has recorded in the number or complement line. The recorded digits are shifted into the vacated end of the number register. If all digits have been recorded and all recorded properly, the exact number will have been replaced in the number register. This fact is checked by adding the contents of the number register into the complement register. The result should be all 1's.

3) A buffer section in the storage can be provided for each reader. Note that setting up these buffer sections does not prevent their use for internal computer needs. The size of the buffer section can be adjusted at will by setting the counter, or the section can be omitted entirely and the film controlled by direct stop and start orders.

<u>ANALOGUE INPUTS</u>: In general these will be measures of shaft positions or other mechanical or electrical amplitudes. One or more converters to binary code will be provided. The computer will obtain the desired information by transmitting to the converter first, an order to convert a certain quantity and, second, an order to transmit to the bus with the number of the register which is to receive the information. These orders will be separated by enough time (used for other operations) to allow the converter to select the desired quantity and perform the conversion. The time involved is unknown at present. The converter will be a self-contained unit with its own control.

<u>ANALOGUE OUTPUTS</u>: Such outputs will be used for positioning open-cycle or closed-cycle instruments or mechanical servos. In general the conversion will be from binary code to an electrical

magnitude which can then be transformed into any desired analogue quantity. Several converters will be provided depending on the number, sensitivity, and accuracy of the quantities converted.

The number to be converted will be sent to the converter unit along with an order designating the ultimate destination of the quantity converted. The converter will perform the necessary conversion and switch the result to the desired place. No further orders are required but care must be taken not to order another conversion by the same unit until the previous one is complete. If another conversion is ordered before the converter is ready or if the input converter is asked for information before it is available, the computer will be stopped until the orders can be carried out.

An alternative possibility is to retain the new order until it can be performed, the computer proceeding meanwhile. If the order storage is full, the computer can then be stopped. This method would reduce stoppage time for a given care in programming but does not seem whorthwhile for Whirlwind I.

Graphical recorders are but one form of analogue output and will be handled with the others except for the addition of start-stop orders and possible speed selection and scale factor recording. Scale factor recording might be carried out less efficiently by the use of another recording channel. Another possibility is to note scale factor changes by some definite trace in the recorded channel.

CHECKING AND CONTROL DESK: This category is probably the least understood and yet most important of all at this time. However, since this problem is to be discussed in detail by concerned parties in the near future, it seems preferable to defer its discussion.

ADDITIONAL ORDERS: These orders fall into three categories:

1) Extension of ca, ad, cs, su, to handle absolute magnitude of numbers. Absolute magnitude may be obtained using existing orders but the greater speed and simplicity of special orders seems warranted here. It is estimated that further equipment includes control connections and possibly two extra gate tubes in the operation timing matrix.

Into this category also go possible modifications in existing orders. The only modifications now under consideration are in rounding procedures. It is not expected that additional equipment except for control matrix connections will be needed for these orders even if they entail the actual construction of new orders for different rounding procedures (as mr and mh).

2) Orders required for the control of the input and

output devices.

For film readers -

a. Start film x - go to position marked by next order.

b. Desired film position.

c. Read in x words.

For film writers -

a. Start film x.

If buffer storage sections are used, no further orders are necessary. In fact, if buffer sections are permanently allocated to a film, no orders at all are needed. Such a system would be wasteful of storage, and would prevent scanning.

The above orders require control lines, control matrix connections and control gate tubes.

For analogue inputs -

a. Convert quantity x.

b. Store last converted quantity in storage register x.

For analogue outputs -

a. Convert quantity supplied and send to x.

b. Start film x, at speed x_2.

Scale factors can probably be recorded in the same channel by special marks or in a separate channel.

c. Orders for automatic subprograms.

The coding of Whirlwind I with its short register length would be simplified in many problems if multiple length number operations could be ordered as simply as single length. In Whirlwind II such a facility might also be desirable, for instance in ordering interpolations or multiple length number operations. The system proposed is basically a way of allowing the operator a small number of special operations to be selected at random by himself and handled as if they were built into the computer. The following method has been proposed.

Three orders are needed. One gives the number of the register holding the first half of the first number to be operated on. The second gives the number of the register holding the first half of the second number to be operated on. The third gives the number of the register which is to hold the first half of the result. The second halves of all numbers are assumed to be in registers immediately following the first halves. One of the three orders must designate the operation to be performed.

The 3-order register numbers are made available to the subprogram as follows:

A new order is derived which does the following -

1) Transmits the contents of AC to BR.

2) Transmits the contents of AR to AC.

3) Transmits the order itself to AR.

Two applications of this order will store the first two orders in AR and AC. Another new order is needed which -

1) Does the same as the above order.

2) In addition, transmits the contents of PC to some special register provided for its storage. This register will probably be a flip-flop register to be provided in addition to present registers. A little recent study has shown that it may be possible to store the contents of PC in electrostatic storage. If this is possible, and some timing studies should discover if this is so, the extra register as well as any extra order can be avoided.

3) Sets PC to one of several possible permanently (at least semi-permanently) selected register numbers. There must be as many of these orders as there are special operations to be provided. In Whirlwind I there might be 3 for addition, subtraction, and multiplication of multiple-length numbers. Note, however, that the kinds of operations that may be performed have not been specified, only their number. The operations themselves are as general as the subprograms stored in the register sequence beginning with the number set in PC. The subprograms may have subprograms of their own. The subprograms may be changed at will even at the behest of the machine itself.

The result of 2 applications of the first order above followed by 1 application of an order of the second kind is:

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1) The desired register numbers are stacked in AE, 1 in AR, 1 in AC, 1 in BR.

2) The starting register number of the subprogram to be used is in PC.

3) The order number to which the machine should return is in a known place.

The subprogram now starts. The first step is to remove the order in AC by a ts or td order. The order in BR is then transferred to AC and removed. The order in AR is transferred to AC using the same type of order as put in AR in the first place. The subprogram then proceeds.

When the subprogram is complete the last order is a subprogram order returning the control to the main program. If a special register is used for storing the return number, a special order is needed. If the return number is stored in electrostatic storage, the standard subprogram order will suffice, the number being transferred to it by a td order.

RESTORER PULSES: At present the restorer pulses are to be generated by the delay counter during storage setup. The high speed 32-position switch removes the necessity for the delay counter which remains, however, as a restorer pulse source. When electrostatic storage is added the restorer pulses can be generated by the storage control. Certain operations, particularly division, require sufficient time between storage operations so that restoring must be done while they are being carried out. The step counter may be used for this purpose, stopping the flow of clock pulses part way through the operation and generating a pair of restorer pulses in the off interval.

An alternative is a restorer pulse generator which counts clock pulses and generates restorer pulses at regular intervals. This possibility has been discarded in the past as wasteful since restoring can usually be done at times when the computer is normally idle. If more accurate information as to electrostatic storage control timing were available, a final decision as to restorer pulse sources and timing could be made.

Robert R. Everett

Robert R. Everett

RRE:has

c. JWF, HRB, SHD, FES, EB, DRB, NT, CW, JOE

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6345
Memorandum M-113

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BLOCK DIAGRAM PRIORITIES FOR WHIRLWIND I

To: Robert R. Everett

From: Harris Fahnestock

Date: October 9, 1947

The Sylvania schedule calls for starting design of cabinets November 3. This means we must have a good estimate of number of cabinets and their height by that time. A critical cabinet is that which will hold the Arithmetic Element and the Register Panel. Arithmetic Element design is under way. We must soon decide what the Register Panel must carry. The Sylvania schedule also calls for starting the Register Panel final design November 10. Accordingly with reference to M-111, I would recommend the following priorities for our information:

A) page 2, (2). Must we add special register for storing program counter numbers during automatic sub-program?

B) page 2, (8). Can we do high speed spot checking by using the present check register, 601, without adding the recently discussed "memory check register"?

C) page 2, (5). Must we add four registers for input and output or can we get along with two? Furnish complete functional specifications.

D) page 2, (3). Program counter modification details needed November 10.

E) page 2, (1). An estimate on amount of additional matrix space before Brown wants to start matrix design.

Harris Fahnestock

Harris Fahnestock

HF:vh
cc: JWF, HRB, SHD, FNS, EB, DRB, NT, CW, JOE, JAO'B

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Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: ADDITIONAL REGISTERS FOR WHIRLWIND I

To: Harris Fahnestock

From: Robert R. Everett

Date: October 22, 1947

In response to your request for further information about the number of additional registers needed for Whirlwind I beyond those already described in the block diagrams, I have made a brief study of the problem with the results given in this memorandum. These results may be summarized as follows:

1) A separate trouble-shooting register will not be needed. The present check register or the proposed input and output registers can be satisfactorily used instead.

2) A separate register for storing program counter contents as part of automatic subprogramming will not be needed. One of the regular electrostatic storage registers can be used instead.

3) One pair of stepping registers for input and output is needed but is probably enough, at least at first. Another pair, perhaps in a small package, could be added in the future if problems being handled seem to warrant it. This requirement should not arise for at least two years.

I believe these three points cover the problems in which you are most interested at this time. The special controls needed for these services as well as additional equipment to be added to existing registers have not been detailed and cannot be until the checking problem has received more consideration. I hope to have out next week for comment a preliminary memorandum on checking.

The rest of this memorandum consists of some discussion of items 1 and 2 above. This discussion is given to substantiate the conclusions drawn and for criticism.

THE TROUBLE-SHOOTING REGISTER

Purpose of Trouble-Shooting Register TSR: All elements of the computer including those not now so fitted are to have gate tubes for reading out to the main bus. A t-s register with gate tubes for reading in from the bus can then receive, upon request, the contents of any computer element. This reception can be carried out at high speed. If TSR is not immediately reused, its contents can be read from its neon bulb indicators. The contents of any part of the computer can thus be examined visually although the contents so examined occurred during high-speed operation. Manually set counters and switches must be provided for selecting the element and time for reading.

Advantages over Step-by-Step Operation: The advantages of this system over the step-by-step operation system are

1) Information is obtained during normal computer operation.

2) It should be easier and faster to set switches and get essentially instantaneous results than to push the single pulse button many times. The counter system can be used for getting the computer in some desired position for starting a step-by-step process or can be used to stop the whole computer for complete examination or for performing a step-by-step operation where the steps are no longer single time pulses but groups of time pulses, either regular or irregular in length. If this equipment only is added, the flexibility of single pulse operation is greatly extended but the additional equipment needed for TSR is greatly reduced. In fact, if TSR can be combined with CR, very little computer equipment is needed for the high-speed examination. The control equipment will be very valuable in examining control pulses and computer operating details in general.

Examining Multiple Quantities: With a single SR it will be possible to examine only one register at a time. It would be very desirable to be able to examine several, either the same one or different ones at different times. There are several possibilities proposed for this.

1) Provide several banks of neon bulbs along with TSR. These neon bulbs are driven from TSR but are provided with gate tubes and holding circuits so that they may register the contents of TSR at different times. TSR is probably still needed since it can be set in a microsecond while the neon bulbs are slower acting. It is at the moment undecided whether to provide sufficient counter controls to select all quantities to be registered in a single computer sequence or to perform the selection manually, requiring long time intervals. In the latter case, the neon bulb banks serve as storage elements and remove the necessity for writing down register contents for comparison.

Another desirable feature would be a comparison circuit which would automatically compare a neon bulb bank either with TSR contents or with a set of toggle switches.

2) Use the stepping registers for input and output to supply information to a cathode-ray tube. As many quantities could be examined as lines could be provided on the CRT face. A difficulty with this system is that the information would have to be available recurrently for continuous vision. The multiple control would be needed if more than one quantity were under consideration. Possible ways out of this difficulty are:

a) Continuous recirculation of a number in the stepping register. The register forms a delay storage element which could provide a continuous display with only one setting. The second stepping register might be used to give a maximum of two displayed quantities.

b) Use a long-persistence or dark-trace tube which would require only a single sweep for continuous viewing. A single control would suffice for this viewing means.

c) Use the regular film output device. With automatic development the approximate delay time between exposure and visual examination would be three to five minutes which is ordinarily excessive. It might be possible to perform a non-permanent developing job in less time.

Use of the stepping registers should be seriously considered. An automatic comparison can be easily made using the second stepping register with switch inputs since comparing circuits are required for normal uses.

<u>TSR Control</u>: The control for any of the TSR methods might be about as follows:

1) Type in on the direct input typewriter a subprogram order to start at some desired place in the sequence. If a standard trouble-shooting sequence is being used, this operation is unnecessary.

2) Set the order number counter for the operation number following the start in which the examination is to be made.

3) Set the TP counter for the TP number when examination is to be made.

4) Set high-speed TP counter for selecting TP not in TPD if desired.

5) Set selector switch for quantity to be determined.

When the time determined by the counters arrives, the clock is shut off. The desired quantity is read out to the bus and from there to TSR. The clock is then restarted and the sequence proceeds.

The multiple control would require several settings on each counter. When the first setting of the order counter is reached, a gate tube is opened which can then be pulsed when the TP counter reaches its first setting. The output of this gate tube can then open a gate tube for the high-speed TP counter first setting. The second settings are also lined up by gate tubes. The quantity selector switch can also be gated by the order counter setting. Assuming five possible measured quantities, five settings are required for each counter and the switch. If the settings are not completely distinct, i.e., use the same order number, clock pulse, or quantity, it is only necessary to make the proper settings the same. If less than five quantities are being measured, the unused settings can be left random or a switch for blanking unused settings may be provided.

Clearing and restarting pulses will be required as well as a switch for automatic comparisons.

<u>Conclusions</u>: It will be seen from the above discussion that the proposal for the use and control of TSR is still nebulous. Any thoughts, suggestions, or simply desires which anyone has would be very valuable. There is, I believe, enough information, however, to consider the present problem which is whether or not an additional register beyond those so far considered is needed for TSR functions.

There are two possibilities for performing TSR functions with present equipment:

1) Use the stepping input and output registers as described above. If the CRT display is used, these registers are not only possible but desirable.

a) They are thoroughly checked in their normal operation.

b) They are not a part ofnormal computer operation.

c) They not only receive from the bus but also step and compare.

d) It is possible to make automatic photographic records of the checking results. It might be desirable to make the computer or a separate comparator perform a comparison between the tape so obtained and a standard trouble-shooting tape made for the particular check problem.

e) If neon bulbs are wanted, they are already available for a single quantity and can be put in banks for multiple quantities.

2) Use the check register CR. The use of this register was the first thought for avoiding a separate TSR.

a) Although a part of the normal computer operation CR can be removed from the system without affecting computed results. The transfer check is lost but this check is complete enough so that if the trouble is there it can be isolated and corrected by other means. A small complication in the control is needed to allow removing the transfer check.

b) Multiple quantities can be examined using neon banks.

As considered at present there is no desirable function that could be performed by a separate TSR that cannot be done as well by existing equipment. It does not seem worthwhile to plan on a separate register for trouble-shooting. The control for trouble-shooting should be worked out in detail as soon as checking ideas have been crystallized.

SUBPROGRAM STORAGE REGISTER

Purpose of Subprogram Storage Register: The automatic subprogram described in M-111 requires for an important part of its operation some place where the contents of the program counter PC may be stored without requiring a separate order. It is also necessary that this place be always the same so that PC may be easily restored to its previous condition at a future time. It was originally proposed that this storage place be a separate flip-flop register which had no other use. A desirable alternate is to use one of the regular electrostatic storage registers thus gaining:

1) The same result with less equipment.

2) The ability to remove the stored information using orders already available within the machine.

There is no basic reason why electrostatic storage cannot be used. The question is simply one of whether the necessary operations can be fitted into the time available. The study is complicated by the fact that the timing diagrams for the automatic subprogram have not yet been worked out.

The operations that must be carried out during automatic subprogramming are:

1) Clear BR
2) Transfer AC to BR
3) Clear AC
4) Transfer AR to AC
5) Clear AR
6) Transfer Storage to AR
7) AR to Bus-transfer Check

This same sequence is used in the earlier orders of the automatic subprogram. See M-111, pp 8-10.

The storage switch is set on TP5. If steps 1 through 5 are then performed, the read in from storage cannot be done until TP3 of the next cycle which is very bad since the bus use is pretty well fixed. Step 6, the transfer on the bus from storage to AR must be done on TP7 if the whole computer timing is not to be disrupted. To accomplish this end note that the automatic subprogram order which actually determines the operation is different from the two which precede it and which simply insert orders in AE. These two orders, which are desirably identical, do not have the extra complication of the subprogram. Therefore, resequence these operations as follows:

1) Clear AR - Clear BR
2) Transfer storage to AR and AC to BR
3) Clear AC
4) AR to AC

The first application of this sequence puts the first order in AC with AR open. The second application puts the first order in BR and the second in AC, again with AR open. Now use the following sequence for the automatic subprogram.

1) Clear AR
2) Transfer storage to AC

The result is the first order in BR, the second order in AC, and the third in AR as before but now all bus transfers can be done as early as TP7 as desired.

The price to be paid for this change is that there is no longer any method available within the standard orders for getting the order out of AR. This step could have been performed in the other sequence simply by another application of that sequence. The price, however, is only another order; in fact, the order previously required to get information out of the special sp storage register may be used resulting only in less of a gain for the new system than at first supposed.

Returning now to this new sequence, the transfer to AR is

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checked on TP8. TP2 is used to transfer PC contents to the storage switch. TP1 is open and can be used for transferring PC contents to storage. There is no time available for checking this transfer if the main sequence time pulses are used. The transfer check can be omitted in this case (not very bad since all elements concerned are used and checked at other times) or the check can be accomplished while the storage control has charge.

The delay counter (or, actually, the electrostatic storage control) must be started if the storage is to receive the program counter number. The time required for this operation will thus be longer than normal but will do no harm.

In order to simplify the storage switch and also to remove the need for clearing the switch before the next order is set up, use the all 0's or cleared register position for storing the counter number. On present timing diagrams the storage switch clear pulse is put in TP1. It can just as well be in TP8. Then, for automatic subprogram start the delay counter or control at TP8 also. This will be done by the operation control. On TP1 read out of PC onto the bus and into storage. TP2 will find the storage switch clear and ready to receive.

The timing of this and, for that matter, all the other operations, is dependent upon the final timing of electrostatic storage. However, it seems reasonable to assume that if the new operation can be performed in the present timing sequence, there is as good a chance that it can be done later as any of the others.

The final sequence is then

TP6	Clear AR
TP7	Storage to AR
TP8	Transfer Check
"	Clear Storage Switch
"	Start Delay Counter
TP1	Program Counter to Storage
"	Set Program Counter (Delay 1/2)
TP2-3-4	Not used

The electrostatic storage can be used for the automatic subprogram return order storage and the operation fitted into the present timing sequence.

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Project Whirlwind
Servomechanisms Laboratory
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SUBJECT: CHECKING

To: Jay W. Forrester, D. R. Brown, N. Taylor, H. Fahnestock, C. W. Watt, J. A. O'Brien

From: Robert R. Everett

Date: October 27, 1947

The subject of checking has recently become of increasing importance for the final design of Whirlwind I. This memorandum outlines some thoughts on checking of various kinds. The presentation is rough and is intended mainly as a basis for discussion.

The memorandum first considers the elements of the computer in order with their possible failures and ways of checking. Consideration is then given to check problems and trouble-shooting problems.

LIST OF THINGS TO BE CHECKED:

100 CONTROL

101 Master Clock

a) Producing pulses without skipping.
b) Pulses of right size and shape.

102 Program Counter

a) Read out.
b) Read in.
c) Count

103 Program Register

a) Read out.
b) Read in.

104 Control Switch

a) Proper setting.
b) Unused setting.

105 and 107 Generation of Operation TP

106 Time Pulse Distributor

a) All pulses.
b) No extras.
c) Right sequence.

108 Generation of Program TP

200 STORAGE

Storage Switches

a) Switches.
b) Deflection amplifiers.

Storage

a) Read out.
b) Read in.
c) Storing

Storage Control

300 ARITHMETIC ELEMENT

301 AR

a) Receiving from bus.
b) Transmitting to AC.
c) Abs. value.

302 AC

a) Receive from AR.
b) Transmit to BR.
c) Add.
d) Carry.
e) Shift.
f) Divide shift.
g) Shift and Carry.
h) Abs. value.

303 BR

a) Receiving from AC.
b) Shifting r and l.
c) Examination of rt. digit.
d) Roundoff.

304 Signal Control Flip-flop

a) Set.
b) Reset

Arithmetic Check

Special Add

305 Step Counter

a) Clearing.
b) Setting.
c) Counting.
d) End pulse.

306 and 307 Flip-flop Controls

308 Divide TPd

400 and 500 INPUT AND OUTPUT

600 CHECKING

Transfer Check

OTHER

Mathematical Checks
Check Problems
Trouble-shooting problems

CHECKING:

101 Master Clock

Possible Failures

a) Complete Stoppage.
b) Missed pulse.
c) Frequency variation.
d) Loss of pulse shape.

CHECKING METHOD: - A pulse checker on the line from the Master Clock will check

1) For pulse height and shape (Checking (d)).

2) Time between pulses (Checking (a), (b), and (c)).

Small variations in frequency will be unimportant since the machine is asynchronous. If desired, a more accurate frequency check could be employed. Actually, a missed pulse would do no harm except as an indication of serious trouble.

If there are two frequencies, a missed pulse in one, not the other, could be very troublesome.

The check for space between pulses could be changed with the clock cut off. On single pulse operation it would be desirable to continue checking height and shape and also to check against generation of more than one pulse. With operating frequencies below normal (if used for trouble-shooting purposes) the check for pulse space could either be adjusted or omitted.

102 Program Counter

Possible Failures

a) Failure to count at all.
b) Miscount.
c) Improper read out.
d) Improper read in.

(c) and (d) are checked by the transfer check. An investigation should be made to make sure the transfer check is complete on all Program Counter operations.

(a) might be checked by mixing switching signals and checking to make sure at least one flip-flop switched.

(b) is most difficult to check without duplicating the counter.

A proposal is:

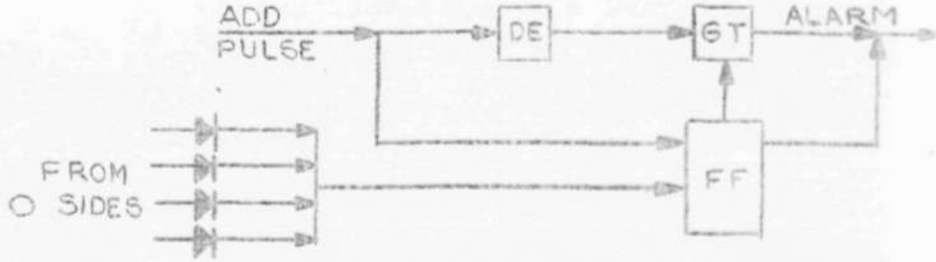
For checking a counter without high-speed carry -

Note the following:

1) For each addition there is exactly one flip-flop that switches from 0 to 1. An exception is the addition that overflows the counter.

2) No section of the counter can switch unless the previous section has switched.

Take the outputs of the 0 sides of the flip-flops (that is, the sides opposite from those that generate triggers for switching succeeding sections). Note (1) above states that one and only one of the flip-flops should generate a trigger on this side for each addition. Then, connect them as in the figure below.

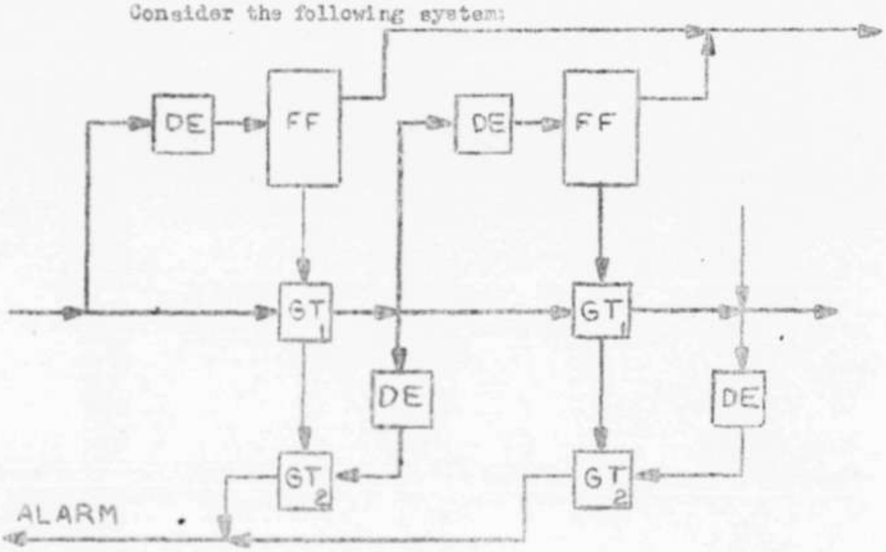


The add pulse comes in, resets the flip-flop, and opens GT. If no pulse comes from the 0 sides, the GT will remain on and the delayed add pulse will sound an alarm. If one pulse comes in from the 0 sides, the flip-flop will switch, GT will go off, and there will be no alarm. If two pulses come in, the second will reset the flip-flop, the reset signal going out the alarm line. More than two are unimportant since the alarm will have sounded.

For checking a counter with high-speed carry -

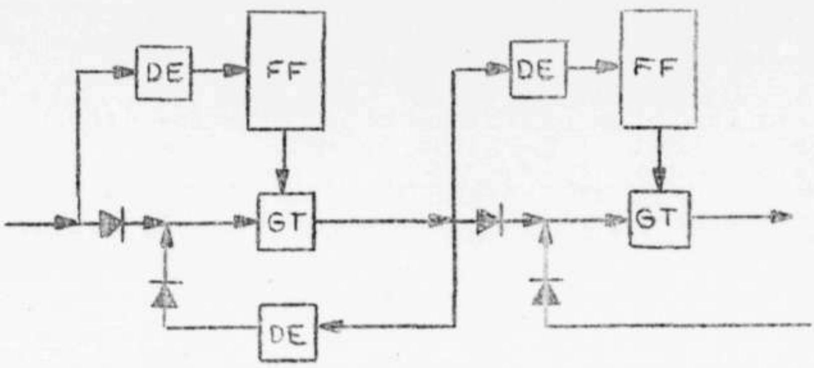
The above method can be used but is only a partial check since a flip-flop can fail to reset (go from 1 to 0) without affecting succeeding sections. Since the number of resets in an addition is a variable, a check similar to that above must be modified.

Consider the following system:



If a carry GT_1 is open, the add pulse will pass through and add into the next flip-flop. Meanwhile the pulse will have added into the first flip-flop and resetting to 0. If the reset fails to operate, the GT_1 and GT_2 will remain on. The pulse that has passed through GT_1 is delayed and sent back through GT_2. If GT_2 is still open, the alarm will sound.

A simpler version but roughly the same idea is:



If the first flip-flop is a 1, the add pulse will pass through the GT. The pulse will return through the delay and again supplied to GT. If GT is now shut, nothing further occurs. Diodes are provided to prevent improper additions. If GT is open, the pulse will pass back into the add line and will cause a set (0 to 1) on some flip-flop. This extra set will cause the one-set check to work.

This combined check seems to function under almost all considered types of failure.

Both output pulses from the last flip-flop, highest order, should be supplied to the check flip-flop.

103 Program Register

The operation of the Program Register seems to be thoroughly covered by the transfer check. This statement should be checked to make sure all operations are covered.

104 Control Switch

Possible failures

a) Failure to receive correct order data.
b) Failure to set according to order data received.
c) Setting of more than one line or of no lines.

The transfer check should catch type (a) failures. A coding matrix may be used in conjunction with the transfer check for checking both (a) and (b).

There is an automatic check against the failure of the switch to select a line at all. The final transfer is ordered by DC but the

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transfer check pulse comes from PC. If the DC does not order a transfer, the transfer check will discover it.

Note: Check on CR clear and correct settings.

If it appears desirable to check for simultaneous selection of more than one line, it can be done at the expense of some equipment.

105 and 107 - Operation Timing Pulses

The ready checking of the appearance of all operation timing pulses is very difficult without duplicating the equipment involved. The pulses appear at random times and in random order. The operation of the switch and the distributor are checked separately. Failures in the diode matrices themselves seem unlikely. The row of output gate tubes is a source of trouble.

A possible check:

Check for a control pulse out for each TP in. Insert dummy gate tubes and TP's for each operation to avoid blanks. Simultaneous pulses are not checked. Many of the simultaneous sets of TP's, however, are connected with the transfer check and can be omitted from this check.

Another possible check is to count total number generated for an operation and compare against the standard number for that operation. The operations could be grouped according to the number used, or by the use of dummy pulses the total for all operations could be made the same.

106 Time Pulse Distributor

Possible Failures

a) Missing a pulse with and without losing sequence.
b) Inserting an extra pulse.
c) Interchanging pulses.

(a) is pretty well checked by the transfer check. Seven TP's are used for three transfers with checks. The omission of any of these seven, with or without losing sequence, will signal an alarm.

The remaining pulse is simply a delay to allow storage setup. It is not checked at present. One possibility is to use a dummy transfer and the transfer check. Or, one flip-flop can be used to check the omission of the pulse.

It is possible to check TPD by its approximate equivalent perhaps by a ring of 8 or a counter of 8 counting time pulses and checking on the end carry.

Missing in sequence is probably gate tube or matrix failure.

Missing out of sequence is probably counter failure.

(b) will in general upset the transfer check.

(c) will in general upset the transfer check.

Some attention should be given to the non-transfer pulse. It is probably worthwhile to study the effect on the transfer check of all simple failure combinations.

108 Generation of Program TP

The checking of these pulses is essentially the same as checking TPD since the program TP are almost all transfer pulses checked by the transfer check.

The appearance of the add pulse can be checked as described in the counter check above by obtaining the counter check pulse from the program instead of from the add pulse.

200 STORAGE

Storage Switches and Deflection

Possible failures

a) Improper switch setting.
b) Improper output line selection.
c) Improper deflection voltage to any or all tubes.

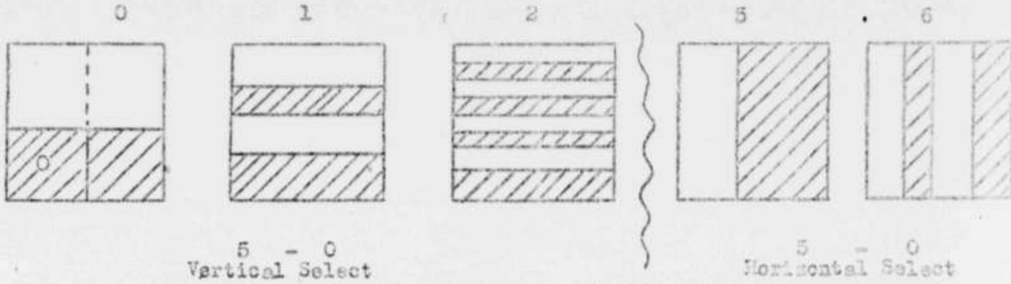
(a) is checked by the transfer check.

(b) can be checked by a coding matrix checking (a) also. See Section on Control Switch.

(c) is more difficult to check. One possibility is to recode the electrical magnitude taking the far end of the line. This check could include (a) and (b) except that (a) at least is very easy to check and probably worthwhile. (b) is easy to check visibly in case of a (c) check alarm.

A check proposed in the past is to provide an extra bank of electrostatic storage tubes used only to check deflection voltages. The tubes are set up and read out the setup number which can be checked against the original order.

One tube can be used in each axis if the entire setup number is read out by sweeping. This method is slow and requires a different type of storage. The patterns on the faces of tubes would look:



5 - 0
Vertical Select

5 - 0
Horizontal Select

There would be eleven tubes in the bank for Whirlwind I. The patterns would be actual stored charges in standard tubes. These tubes actually constitute a recoder for the electrical magnitude of the deflection voltage.

There is no check against the failure of the deflection voltage at some particular tube rather than all tubes.

A check against a single space out can be accomplished with one tube storing alternate $\pm$. A particular setup should be either $\pm$. A mistake of one position will result in the wrong polarity.

<u>The Storage Itself</u>

The storage can be thoroughly checked by some procedure such as described in M-111.

<u>The Storage Control</u>

The Storage Control has not been laid out in detail but can probably be checked readily by the storage checks which should operate if the control makes an error.

300 <u>THE ARITHMETIC ELEMENT</u>

The Arithmetic Element is difficult to check continuously except by duplicating equipment. The equipment is both fast and complicated. There is little time for checking since almost all the parts are working at near maximum rates.

A usual suggestion is to duplicate the Arithmetic Element. Such a duplication is quite expensive since the Arithmetic Element is a large part of the computer. It would be nice to go further and provide three arithmetic elements in order to determine not only the existence of a failure but which unit failed. An extension leads to the suggestion that two or three complete computers be provided and checked against each other at every step.

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All these methods require large amounts of additional equipment which must be kept running. It seems at this time better to check where possible with small amounts of equipment and low time loss. Then smoothness checks will be used for overall results and occasional check problems to pick up permanent failures.

301 AR

Possible Failures

a) Read in from Bus.
b) Transmit to AC.
c) Abs. value

(a) is checked by the transfer check.

(b) is not at present checked. One possibility is to put in a special transfer check for this on ca. The contents of AR are transferred to AC on this operation. If they are transferred back and added to AR, the result should be all 0's. This check would require gates for reading from AC to AR, add inputs to AR and a check for all 0's.

The check does not warrant this equipment. It is intermittent; it will check only about 20% of the transfers from AR to AC.

Check Problem check

Transmit 1.00. . . . . . 01 to AC

Add 0.11. . . . . . 11 to AC

The sum should be positive.

This check checks a lot of other things too.

(c) could be checked if a method were available for seeing if any of the AR flip-flops had not switched.

302 AC

Possible Failures

a) Improper reception from AR.
b) Improper transmission to BR.
c) Failure to add.
d) Failure to carry
e) Failure to shift left.
f) Failure to divide shift left.
g) Failure to shift and carry.
h) Abs. value

(a) is discussed briefly under AR.

(b) lies roughly in the same category as the transfer from AR to AC. The transfer is done only in multiplication. BR always is cleared before receiving. The number could be sent back to AC and added in using the adding ability of AC. The addition could be made after the carry gate tubes if checking for all 0's is desired. Either all 1's or all 0's is satisfactory since they both represent 0 or AC cleared.

It might be desirable to have a clear check on AC anyway since AR to AC will probably not be checked.

The row of gate tubes needed for transmitting BR to AC could be used instead of shifting when actual information is to be transferred but there seems little advantage to this modification.

(c). A possible partial check is to take the switching signal from the partial sum flip-flops in AC and transmit them to the complement gate tubes of the corresponding AR digits. Passing a pulse would represent the unwanted switching of a flip-flop. If another gate tube could be added to provide a pulse on non-switching, this pulse could be supplied to the direct gate tubes of the corresponding AR digits, checking for failure to switch which is much more likely. This check would also check (a).

A timing study would be necessary to discover if this check can be accomplished. The check does not consider the carry flip-flops.

(d) can be checked as is the high-speed carry in PC. The operation of the gate tubes on the carry flip-flops is not checked by this nor is the failure to operate of the carry GT's. It is also necessary to check the repassage of the carry pulses by some other method than PC, probably a method requiring one additional GT per section. The check does not look very satisfactory.

A second GT on the carry flip-flops could be used to check the proper carrying and clearing of these flip-flops. A second row of high-speed carry GT's could very easily check the carry. These GT's would be placed in parallel with the present ones and supplied with the same pulses delayed one flip-flop operate time. Passed pulses indicate errors of omission and commission.

(e) has several possibilities for checking. A definite shift pulse should appear on one or the other but not both of the shift lines leading from each digit. A check could be made of this but it would be expensive of equipment.

Another possibility is to send shifting pulses over to the next digit but interchanged to see if the flip-flop had set correctly.

(f). Same as (e) except check left digits also.

(g). A check could be provided for checking the appearance of a setting pulse somewhat as in g1.

For (h), see discussion under AR. It would be possible to check for proper clearing of AC.

304 Sign Control Flip-flop.

This device could be checked by duplication if desired. It does not seem particularly valuable to do so in view of the lack of checkingelsewhere in AE.

The arithmetic check and special add fall in about the same category.

305 Step Counter

Possible Failures

a) Clearing.
b) Setting.
c) Counting.
d) End pulse.

The clearing and setting from the bus (a) and (b) are both covered by the transfer check.

A possible check against failure to set properly on multiply or divide is to provide a setting system for CR. Then, the first time the bus is vacant (very soon) set CR and read out of Step Counter for a transfer check.

(c) may be handled like PC if there is sufficient time.

(d). The end pulse is one of the signals that actuate the check of (c).

306, 307, 308 - Flip-flop Controls - Divide TPD

These items fall in about the same category as the sign control flip-flop.

It is very difficult and expensive of equipment to provide any adequate continuous checking of the Arithmetic Element. The amount of checking that can be done easily is so sketchy as to discourage the use of continuous checks at all in AE.

400 - 500 INPUT AND OUTPUT

These will be checked separately. See M-111.

Bus Systems - These seem to be adequately checked by the transfer check.

600 CHECKING EQUIPMENT

All checking equipment must be checked itself. Wherever possible the checking equipment must take an active part in the proceedings so that any failures in the checking equipment will also sound the alarm.

An example is the transfer check where the equipment itself is part of the checking loop. Even here, however, failure of the checking register or of the equipment which examines the condition of the register following the check will completely destroy the entire transfer check.

The operation of the register itself can be checked by checking the cleared position as well as the sum.

The alarm circuit can be checked by gating the alarm pulse as well as the check pulse and checking on intermediate stages. If the check is made on the transfer of the order but before the repeat transfer and the all 1's position is omitted in the order code, the failure of an ungated alarm pulse to appear will signify an error. Since the orders contain 0's in all positions at different times, the check is complete and automatic, although infrequent. If desired, special superfluous orders can be inserted by the programmer for this check.

The arithmetic check should also be examined at intervals. The problem, in general, is to effect these checks automatically if possible and without requiring special orders. The difficulty arises in checking the alarm without stopping the computer. A check tape for which this is but one of many uses could be used which would check the arithmetic check by purposely overflowing it. The operator could restart the machine at each stop (there are only a few). If the machine stopped itself without an alarm, there is a fault. This and other checks could be performed regularly, perhaps at the start and close of each day.

In checking a counter, perhaps PC, by the method mentioned, each of the many possible errors must be committed and the alarm checked. It would be possible to gate this alarm and try a check pulse when there has been no add pulse to check for check flip-flop setting. This does not check against a high-speed carry failure. A check against the double-add failure may be obtained by clearing the flip-flop after each regular check by adding into the trigger input and noting the alarm. It is unfortunately true that these methods require gating the alarm pulses and that these gates are suspect and unchecked. A complete check is only possible if an actual error is committed and the alarm allowed to stop the machine. In this instance the alarm gates can be doubled or even tripled as a protection and checked, perhaps manually, at wide intervals only.

A tape input, possibly a combination of an order tape and a special tape, providing specific control pulses only, can be used to order checking procedures including non-standard orders and definite failures to check checking errors. In company with this can be a device which is put in operation when the checking is proceeding and which will clear all faults and restart the machine at each alarm. If an alarm fails to appear, the computer can stop without an alarm and the stoppage during check brought to the attention of the operator. This type of checking is in addition to the normal checking which is to find faults in the non-checking parts of the machine.

CHECK PROBLEMS AND TROUBLE-SHOOTING PROBLEMS:

Check problems discover the existence of an error without determining the nature of the failure or the location of the failed part. It is desirable in a check problem to cover the greatest possible amount of equipment in the fewest possible operations so that the check problem may be carried out frequently without appreciably reducing the efficiency of the computer.

A check problem is mentioned on page 10 which consists of:

Transmit 1.00. . . . . 01 to AC

Add 0.11. . . . . 11 to AC

The sum should be positive.

This problem checks:

1) Read gates from AR to AC. If any gate fails to transmit, the sum will be negative. Throughout it is still assumed that only one failure occurs at a time.

2) Proper reception by AC of single digits per section.

3) Proper addition in AC15 only.

4) Carry operation AC15 only.

5) High-speed-carry in all digits.

If the answer is negative, there is no way of telling from the check problem where the error occurs. A possible trouble-shooting problem procedure for discovering the error source might be:

First try

Transmit 1.00. . . . . 010 to AC

Add 0.11. . . . . 111 to AC

Examine sign of sum.

Then try

Transmit 1.00. . . . . 0100 to AC

Add 0.11. . . . . 1111 to AC

Continue until a positive result is obtained. This test will limit the failure to a single digit. The fault is in the first successful column if there is a high-speed-carry failure. Otherwise, it is one column to the right.

Then, to check whether the failure is in AR read out gates or in AC reception:

Transmit minus(cs) 0.11. . . . . 10 to AC

Subtract 1.00. . . . . 00 from AC

Result should be positive if AR gates were at fault since only the AR complement gates have been used.

Then, to check whether the failure has been in AC reception or in high-speed-carry, if the fault is not in AR

Transmit 0.00. . . . 010. . . . 00 To AC

where the 1 is in the last unsuccessful digit column as determined by the test above.

Add the same 0.00. . . . 010. . . . 00 to AC

Then add 1.11. . . . 100. . . . 00 to AC

If the column is receiving, the sum will be positive and the fault will be in the high-speed-carry. Otherwise, the digit tested will be known to be faulty.

All five possible failures can be isolated by the above sequence. The computer could, if desired, try the check problem and on discovering the failure go on through the trouble-shooting sequence automatically. When the failure is determined, the computer can stop either sending its last order number to an output decimal printer or leaving it to be read from the neon banks. The operator can then tell from a code book both the kind of error and the panel in which the failure is located.

I do not suggest that the above sequence has a real value except as an example.

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The trouble-shooting register can be used to accomplish the same end with the help of the operator.

In this case the machine would stop when the check problem failed. The operator would read PC and get from a code book the test being run and the proper settings for the TSR controls. The machine would then be started and go through the check problem over and over again while TSR extracts the following information:

1) AR contents for first addition.

Should be 1.00. 01

2) AC contents after first addition.

Should be 1.00. 01

3) AR contents for second addition.

Should be 0.111. 11

4) AC contents after second addition but before carry.

Should be 1.11. 10

5) AC contents after carry.

Should be 0.00. 01

The different failures have a distinctive appearance. It is not possible, however, to tell whether AR has read out incorrectly or AC has received incorrectly if one of these errors has occurred. It is necessary to repeat with complements as described above under trouble-shooting problems in order to use the other AR gates and isolate the error.

Much work must be done in designing both check problems and trouble-shooting problems in order to get thorough and efficient checks. Wherever possible, those parts of the machine which are undamaged should be used to reduce the load on the operator by automatically carrying out trouble-shooting procedures.

Robert R. Everett

Robert R. Everett

RRE:has

Copies: SHD, HRB, FMS, EB, JOE.

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6345
Memorandum M-129

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND I TROUBLE SHOOTING, COMMENTS ON MEMORANDUM M-123

To: Robert R. Everett

From: Jay W. Forrester

Date: October 28, 1947

The following comments occur to me after reading Memorandum M-123 on the Trouble-shooting Register.

The Stepping Register normally used for input and output sounds like the best bet for the trouble-shooting requirements.

To simplify equipment, I would suggest that we not use more than one set of coincidence circuits and therefore read out only one number per cycle of the check problem.

It should be possible, if desired, to channel the trigger, which is obtained from the coincidence circuits for operation of the trouble-shooting register, into the clock-stop system. It should then be possible to readily restart the check problem at its beginning. The stop order and the restart facility would make it possible to progress through the check problem one step at a time until trouble is detected. This is desirable since trouble might result in strange and unexpected computer operation which would prevent it from restarting on the test problem.

If no appreciable amount of extra equipment is required, it might be desirable to have the coincidence pulse from the counting circuits restart the check problem at its beginning in order that the test problem up to a given point can be solved cyclically. An error signal from the check register could then be used in the clock-stop circuit so that the computer would stop only if a mistake were made on the number being observed. This would be useful for transient troubles.

I feel we should consider both neon lights indicating the contents of the stepping register and a cathode-ray tube with double trace for indicating both the number and its complement in the stepping register. Normal permanent failures would be picked up on the neon lights but the cathode-ray tube and stepping register reading both numbers and complements could be used for detecting transient disturbances which would result in a wrong number only occasionally.

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Automatic comparison of the number read into the trouble-shooting register with the pre-set correct value would be of considerable help and facility is probably already available for this operation.

I would suggest considering the use of punched cards on which can be entered the proper quantities for a check test. Reading would be done in a simple, manually operated contacting device. The card could be punched with the order number, counter initial setting, the time pulse counter number, the high-speed time pulse counter number, and the selection of the quantity to be determined as well as the proper value of this quantity which would be fed into the check register. Checking could then be done by inserting cards, one at a time, into the reader until the trouble sequence is located.

Jay W. Forrester

JWF:has

copies: H. Fahnestock
H. Boyd
N. Taylor
D. Brown
C. Watt

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: CONTROL DESK, WHIRLWIND I

To: Harris Fahnestock, Robert R. Everett, David R. Brown, Norman Taylor and C. W. Watt

From: Jay W. Forrester

Date: October 17, 1947

The following miscellaneous thoughts occur to me regarding the control desk and its interconnection to Whirlwind I. These ideas are all subject to discussion and correlation with other information.

The control desk should include a decimal keyboard and conversion circuit in order that numbers in the computer can be altered as required in simulation problems and in trouble shooting. It also provides a means for inserting special orders and numbers for checking purposes.

A special register, perhaps the same one as used for normal checking purposes, should indicate any number selected from a repeating check problem in the computer. Monitor registers and setting switches should be available on coincidence counters for selecting the proper point in the test problem as a function of the program counter setting and the clock pulse distributor position. The output of this multiple coincidence system should be available as a trigger for various scopes as required on the control desk and also should be piped to convenient points throughout the computer perhaps in each cabinet of the Whirlwind I system so that test equipment can be operated.

Trouble indications should if possible be of the double acting kind indicating both the satisfactory state of operation and the unsatisfactory state of operation to guard against pilot light and associated circuit troubles. However, during normal operation it should not be required that the operator observe a large array of lights which are on but rather that his attention be attracted by lights which come on only when trouble exists. A single light indicating that everything is satisfactory should be so interlocked that any trouble light will turn off the normal indication and be substituted by one of several trouble indicators.

Trouble indicators should indicate the source of clock stop orders arising from various checks in the computer, should indicate filament power plate supplies, bias, etc. arranged in some sort of coded system to use the smallest practical number of lights. For example, one light might be used to indicate plate supply difficulty while another light would indicate the cabinet in which trouble has arisen. Likewise a bias supply indicator might initiate the same light for a given cabinet. Interlocks where necessary should be so arranged that trouble is indicated at the primary source. For example, failure of a bias supply should perhaps automatically trip various plate supply voltages. Trouble indication should appear only on the bias supply light until that fault has been cleared. Control switches should include an emergency stop circuit which can be located at various parts of the computer in case of fire, etc., perhaps also interlocked with thermostats.

The control desk should provide for stand-by operation, a definition for which must be established, probably meaning filaments on and plate supply voltages turned off.

If at all possible, starting of the computer should be a single switch operation and probably should have a key type lock to prevent unauthorized use. Proper interlock circuits must be available for starting motor generator sets and turning on filaments first and in proper order.

Filament voltages should be increased gradually unless we have information to indicate this unnecessary.

D-C power supplies should probably be equipped with ripple monitors which are essentially a-c amplifiers operating lock-in relays to indicate ripple or transient voltage disturbances. These should be sufficiently broad-band to catch video spikes appearing in the d-c lines and probably should operate through gas tubes so that single transients will be recorded. Likewise regulated power supplies should have voltage monitors possibly of the type that compare the supply voltage with a standard cell through a vibrator circuit, converting the signal to a-c and amplifying for operation of indicating circuits.

Scopes on the control desk should include one for clock pulses, probably a separate one for indication of restorer pulses, and the possible continuous presentation of time pulse distributor and operation control output signals which can be triggered from the coincident circuit or from any other source which will give a useful output. Perhaps for example, one might initiate the scope for each multiplication or each addition and watch a sequence of output pulses to check for jitter and irratic operation.

Should a push-button for inserting single pulses into the restorer system be available in order that the triggering of flip-flops can be observed?

The system must be interlocked with the air conditioning for temperature control probably with thermostats in each cabinet. Cabinet doors should have interlocks so that open doors are indicated in order that the operator may know that air flow is interrupted in that cabinet.

Considerable attention should be given to the location and grouping of neon indicator lights considering their relative importance to one another and the problem of easy reading. An output register from the decimal keyboard should probably line up with the display of register lights so that easy comparison can be made between any decimal number and the binary indication from the registers. To avoid confusion, slide shutters or other devices might be considered for masking of the zero position lights of the flip-flop except when necessary for checking the individual flip-flop operation. The control desk must provide indicators for the film supply in the output unit and for the controls necessary for these units, especially the one providing graphical recording where the start-stop and speed controls may be manual in many cases.

Consideration must be given the cockpit simulation problem to decide whether any control for that system will be on the control desk or merely interlocked with the on and off controls of the computer itself.

It is probable that a cathode ray tube should be provided on the control desk which will be deflected by the deflection voltages of the storage tubes and which will be triggered by the storage tube triggers. It should also be possible to use the coincidence counter system for triggering this indicator scope at any desired storage operation in the check problem. The scope could have ruled or indicated on its face the proper locations of the various storage positions.

JWF

Jay W. Forrester

JWF:vh

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6345
Memorandum M-135

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BLOCK DIAGRAMS, ELECTROSTATIC STORAGE

To: Jay W. Forrester

From: Robert R. Everett

Date: November 10, 1947

Drawings:

B-39391
B-39392
B-39393
B-39394

Block diagrams in this memorandum on electrostatic storage are prepared for discussion purposes. They are supplied as illustrative information and will be considered in detail, revised, and extended before use in the system.

There are many changes which can be proposed for the system about to be described. Some of these are listed at the end of the memorandum. The system described is complete within its limitations, however, and improved designs should wait for more exact storage specifications.

Drawing B-39391 is a block diagram of a single electrostatic storage tube and its associated equipment. The box labeled "One Electrostatic Storage Tube" includes any necessary output amplifier. The output of the storage tube is sent through a delay to a three-position flip-flop. This flip-flop is assumed to have the following characteristics:

1. It has three stable states.

2. It can be set to any of these three stable states by the application of triggers to the proper points.

3. The application of a positive trigger to the trigger input will cause it to switch in one direction; i.e., from 2 to 1. The application of a negative trigger to the same trigger input will cause it to switch in the opposite direction; say from 2 to 3.

4. It is possible to pick off positive signals from vacuum tube plates to correspond to the three stable states of the flip-flop. Furthermore, there must be at least one point with three potentials corresponding to the three states.

This flip-flop, and for that matter the whole system to be described, has been mentioned in Memorandum M-111. The positions of this flip-flop are labeled write plus, read, and write minus where read is the middle position.

The action of the storage tube during reading or writing is determined by the potential of one of its elements, either the screen in front of the storage surface or the signal plate behind it. The action of the tube, except for polarities, is unaffected as far as these block diagrams are concerned by which element is chosen. In drawing B-39391, the screen or plate is shown connected through a buffer amplifier to the output of the three-way flip-flop. It is assumed that this line will have a different voltage level for the three positions of the flip-flop. When the tube is not being used for reading and writing, the holding beam will be on, and the screen or plate should be held in the write plus position. It will probably be desirable to turn off the holding beam during the operations of read and write minus. The holding beam is thus shown connected to the same line as the screen or plate in such a fashion that when the screen or plate is at the write plus potential the holding beam will be on, while if the screen or plate is placed at some other potential the holding beam will be turned off.

The sequence of events for using the tube is then as follows:

1. Set the switches which determine the deflection voltages for all the tubes in the bank. Two or three microseconds must be allowed for these voltages to reach their final values. During this time it is desirable to keep the holding beam on. The screen of the tube will thus be left at the write plus position, as will the three-way output flip-flops.

2. Set to read condition. When the deflection voltages are almost set and just before the high velocity beam is pulsed, it is necessary to set the three-way flip-flop to the read condition; thus setting the screen or plate voltage to the read condition and turning off the holding beam.

3. The high velocity beam is then turned on.

4. After the reading time has elapsed, the high velocity beam is turned off. The delay element in the signal line from the tube to the flip-flop is made large enough, if necessary by the use of additional tube elements, so that the screen or plate potential may be held in the read position until the tube has been completely read. When the beam has been turned off, the three-way

flip-flop must have been set into one of its write positions because either a positive or a negative output must have come from the tube. It is thus possible to check to see whether the three-way flip-flop is in one of its write set positions. This is shown schematically as diode mixing onto a check for write line which connects to all tubes in the bank.

5. Send a single pulse to the main-control time-pulse distributor. It is assumed that the control pulses for the electrostatic storage tube bank are derived from a special electrostatic storage control which has no information as to whether the tubes are to be read or written on. The single pulse sent to the main-control time-pulse distributor will return read-out, read-in or clear signals to the three-way flip-flop and, at the same time, pulse the necessary gates in the other equipment of the computer. If the storage is to be read out, the read out to bus line is pulsed and the information is sent out through the gate tube and the bus driver to the bus. The three-way flip-flop and screen are left set so that the previous signal will be restored when the high-velocity beam is turned on. If the tube is to be stored on, the read in from bus signal first sets the three-way flip-flop to the write minus position. It also gates the in gate tube. If a one comes in from the bus the three-way flip-flop will be reset to the write plus position; otherwise, it will be left in the write minus position.

6. The high velocity beam is again turned on.

7. After the proper time has elapsed the high velocity beam will be turned off. The signal should have set the three-way flip-flop back to the read or neutral position, a fact which can be checked using the check for read-in gate tube.

If the check is successful the three-way flip-flop should be reset to the write plus condition thus turning on the holding beam and leaving the tube in its normal condition. A pulse should also be sent to the main control restarting it and stopping the electrostatic storage control.

The electrostatic storage control presents some special problems since the times involved are not finally established and operation should be made adjustable over wide limits if possible. Drawing B-39392 shows one possible method for accomplishing the control of the electrostatic storage.

It uses an eight way time pulse distributor which can be identical with the ones used in the main control of the computer. The clock pulses to this distributor are not supplied directly, however, but through a counter. The counter shown here is a 24 or 16 position counter allowing time intervals between outputs of the time pulse distributor of from 1 to 16 microseconds.

The start signal from the main control switches the flip-flop, opening the gate tube, and allowing the one megacycle low frequency clock pulses to reach the counter. The counter has been preset to some particular value. When it reaches its all ones position the next pulse will travel down the high speed carry gate tube line into the eight way time pulse distributor and go out the first position. The first line can be connected to any or all of the flip-flops in the counter by the vertical lines. If no connections are made, the counter will be at zero and no pulse will reach the time pulse distributor for 16 counts. If all connections are made, the counter will be set at all ones and the next clock pulse will reach the time pulse distributor. Intermediate sets of connections allow any time delay desired between 1 and 16 microseconds. When the second pulse reaches the time pulse distributor it will go out the second line which is again connected back into the counter as desired to produce any desired delays. The whole system, therefore, provides pulses in sequence on the lines coming from the time pulse distributor with delays between them which can be arbitrarily selected. The connections can be made through diodes soldered in place.

Drawing B-39393 shows a complete control of the electrostatic storage. The tubes are connected to the bus, there being two tubes corresponding to banks 1 and 2 connected to each line of the bus. With the system in its normal position, the three-way flip-flops of all tubes will be at the write plus condition and the holding beams will be on. The switches in the selection devices will all be at their cleared position as will the electrostatic storage control time pulse distributor. When the storage is to be used the main control will send a read-in pulse to the switches on the horizontal and vertical deflection amplifiers and the single position flip-flop switch which is used for bank selection. This will read in the 11 digit address section of the order which has just been read out of the program register, see R-127. At the same time the main control will send a start pulse to the electrostatic storage control and will also stop the flow of clock pulses to its own time pulse distributor. The deflection amplifiers will then begin to set up the proper deflection voltages in all the tubes including both banks. When the delay, determined by the initial setting of the counter in the electrostatic storage control has elapsed, the first pulse will appear out of the electrostatic storage control. This pulse is to set the three-way flip-flops in the bank to be read to the read condition. The outputs of the bank selection flip-flop are thus supplied to the gate tubes 01. The initial pulse coming from the electrostatic storage tube control will thus go out only that bank line which has been selected, and will switch only those flip-flops in the selected bank.

After another selected delay the second pulse will appear whose purpose is to turn on the high velocity beam in the selected tube. Once again it is necessary to use the output of the bank selection flip-flop to set the gate tubes 02, thus allowing the beam pulse to turn on only those beams in the selected banks. Since the beams are to be kept on for an appreciable time, holding flip-flops are provided which set up a voltage through the buffer amplifier on the line going to the selected bank for holding on the high velocity beam.

After another selected delay, the third pulse will appear from the electrostatic control and will be applied to the reset inputs of both the beam flip-flops; thus turning off the on beams but not affecting the off beams. This pulse will also go to the gate tube on the check-for-write line, sending out an alarm if any of the flip-flops have failed to be changed from their read position.

After another delay, probably of short duration, the next, or fourth pulse, appears from the electrostatic control. This pulse is sent to the main control time-pulse distributor and provides the reading and writing pulses to the storage tubes. It may or may not be necessary to channel the read and write pulses to gate-tube pairs selected by the bank selection flip-flop, depending on the particular polarities needed during the holding action.

The fifth pulse from the electrostatic control turns on the high velocity beam again through the gate tubes 02 and the holding flip-flops. After a suitable delay, pulse number six will appear and turn off the high velocity beam. It will also check for read using the check-for-read line and gate tube and send out an alarm if any of the three-way flip-flops on the selected bank have not been returned to the read condition. This pulse is also used after a delay to clear the three-way flip-flops back to the write plus condition; thus turning on the holding beam and leaving the tube in the holding condition. This sixth pulse also clears the switches in the horizontal and vertical deflection and bank selection systems, restarts the main control time pulse distributor, and resets the electrostatic storage control time pulse distributor to its zero position.

The tubes can then remain in a holding condition as long as desired or may be read again immediately.

Drawing B-39394 shows the additions to the present computer system caused by electrostatic storage. The rest of the computer is not shown but is the same as in Figure 46 in Block Diagram Report R-127. The electrostatic storage tubes and the selector switches are connected to the bus. While there is no connection between the bus and the electrostatic control, the control must be supplied with clock pulses.

The control pulses from the main control to the electrostatic storage are already almost all present in test storage. The read-out read-in for the switches, the read-out read-in for the electrostatic storage tubes themselves, the start for the electrostatic control, and the restart for the main control are already present. The start and restart are at present used for the delay counter.

These block diagrams are not only tentative but incomplete. Provision has not been made for using the transfer check on either the storage switch settings or in using the storage itself, except in the case of reading out. When reading in to either the switches or the storage, it is necessary to read out again immediately to the main bus for checking purposes. This difficulty can be easily avoided in the case of the switches by not stopping the main time pulse distributor until one pulse time after the electrostatic control has been started. This one pulse time can be used for ordering the transfer check. In the case of reading in to the electrostatic storage, one possibility is to send two pulses to the main time pulse distributor instead of the one proposed at present. It should be easy to work out these details.

I think that the electrostatic storage control is probably flexible enough for our purposes. Not only does it possess the advantage of adjustable delays between pulses but it uses our standard and already designed eight way time pulse distributor and provides two spares for unforseen operations.

Among the many possible changes in this system are the following:

1. The use of a single output three-way flip-flop system for the two tubes in each digit column. For systems with more than two banks of storage tubes, all the tubes in one digit column could be connected to one output system. Some special equipment would be required for mixing but a net saving of tubes should result.

2. The delay in the tube output line could be avoided by providing a special holding flip-flop for the screen and triggering this flip-flop from the output three-way flip-flop.

3. The characteristics of the output flip-flop and the checking procedure could be changed to avoid the effects of switching transients on the tube output.

4. If the write time on the tube is appreciably longer than the read time, the sequence can be changed to only provide the long write time when a signal is being stored. Only part of

the charge need be removed when reading thus allowing relatively rapid restoring if the data is not changed.

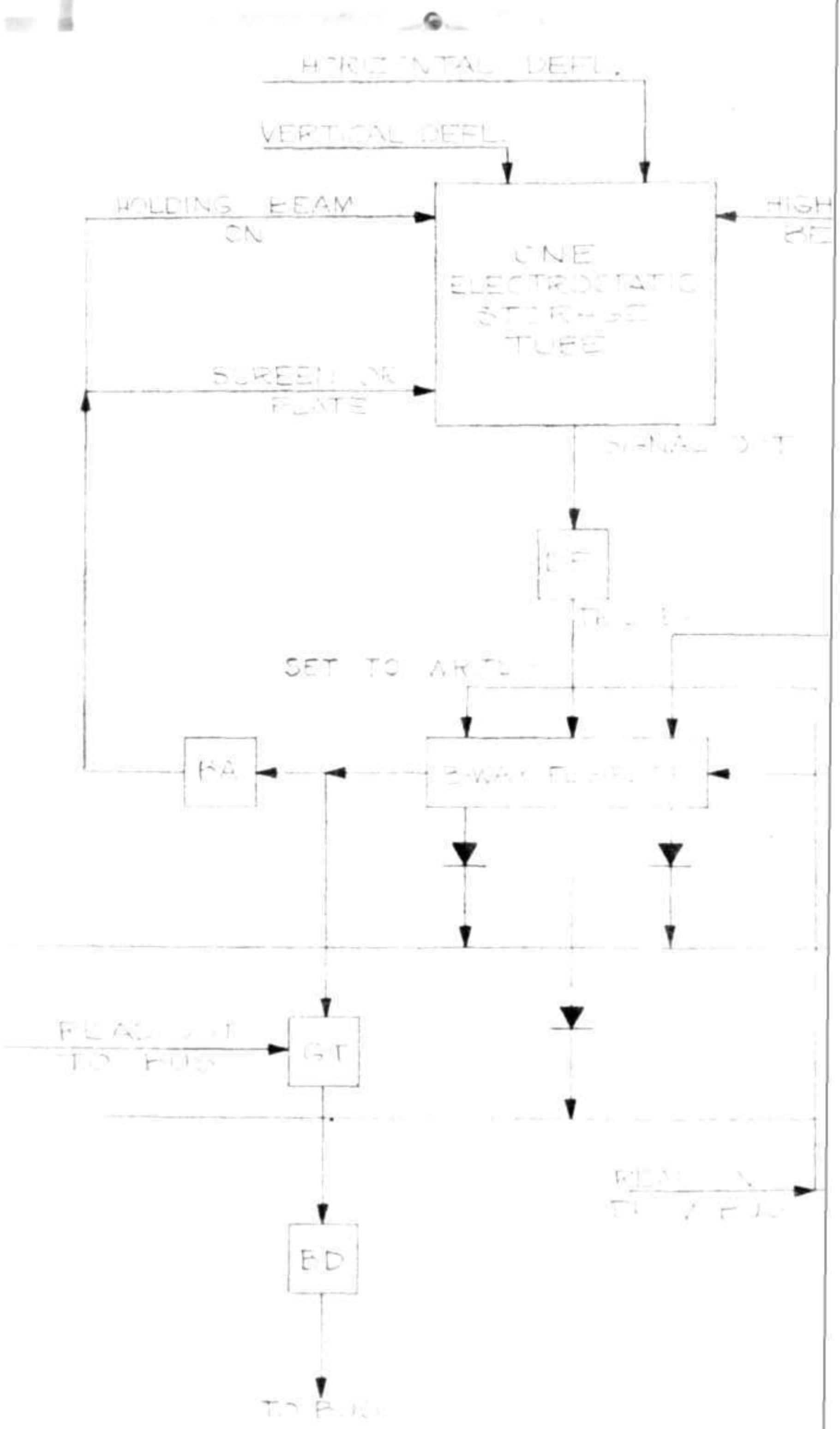
Robert R. Everett

Robert R. Everett

RRE:bo:vh

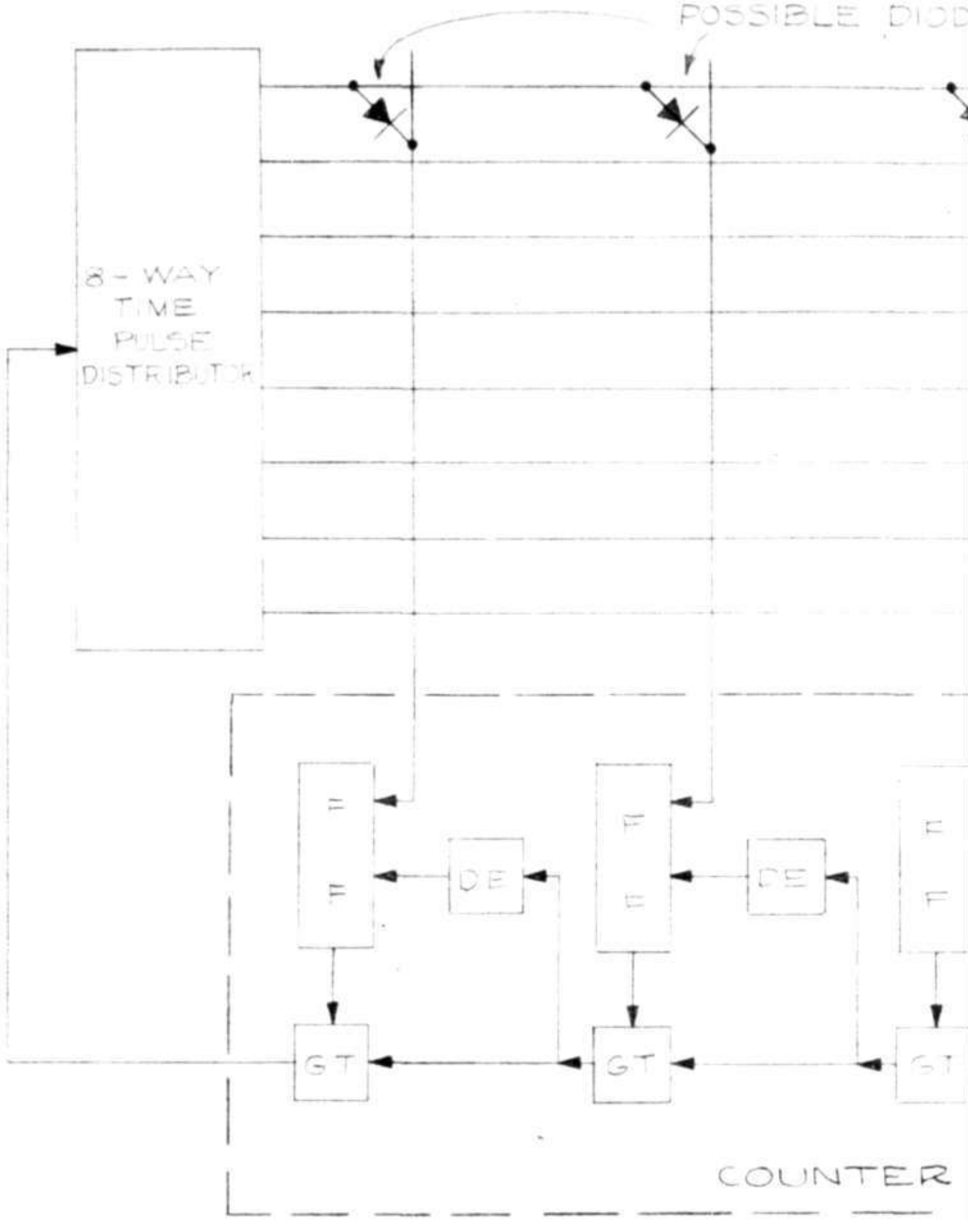
APPROVED FOR PUBLIC RELEASE. CASE 06-1104.

B-39391



USED IN MEMO 135

B-39392



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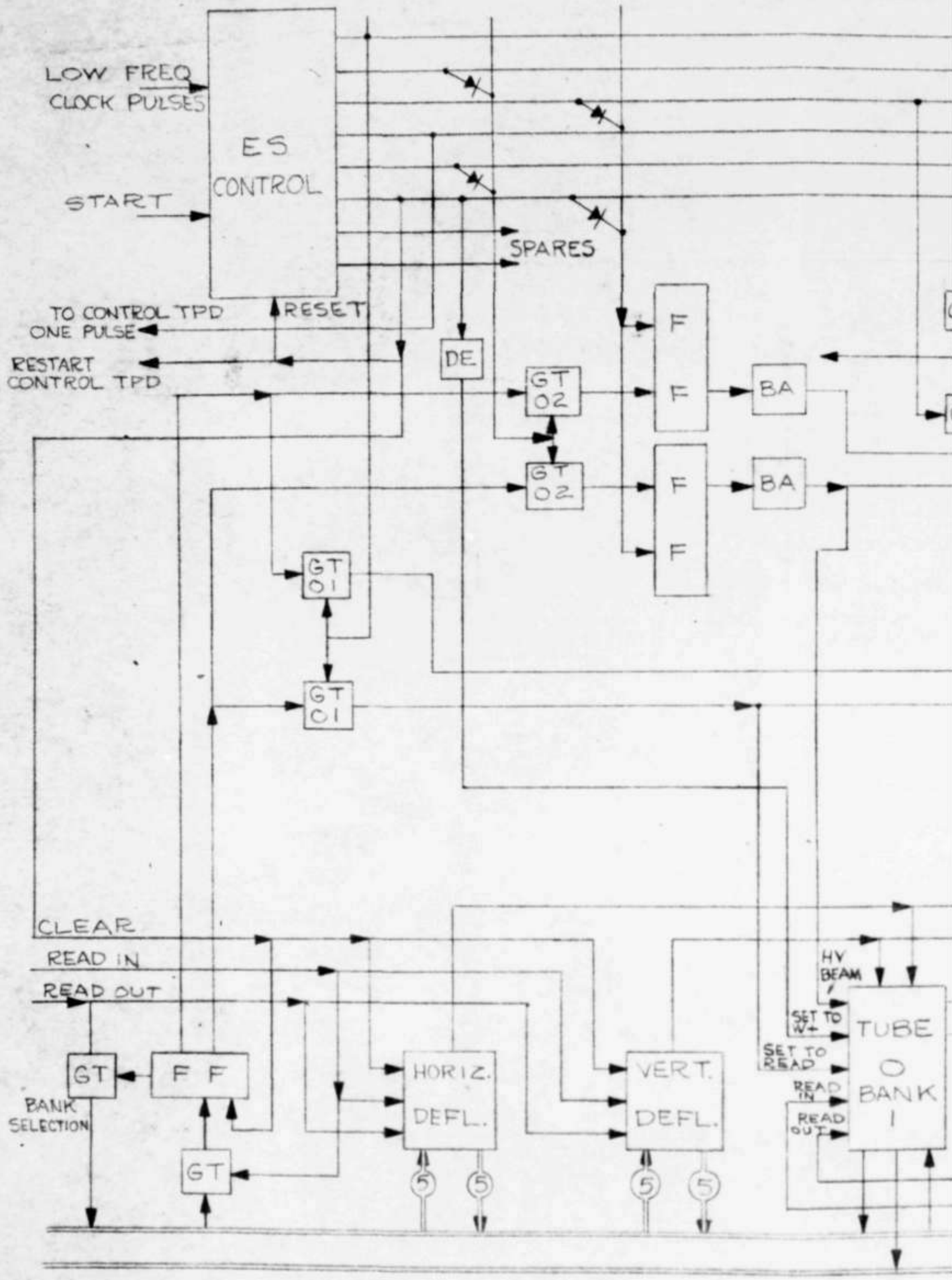
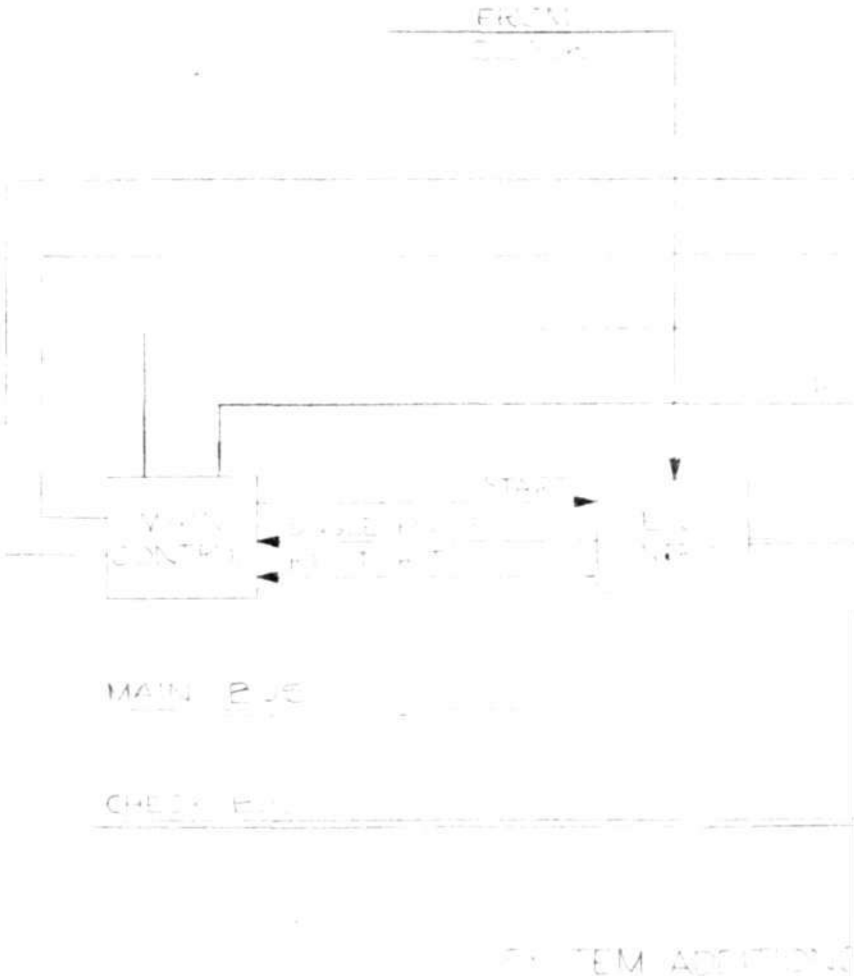
B-39393



USED IN MEMO 135

B-39394

USED IN MEMO 135



Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: ACCUMULATION OF PRODUCTS IN THE WHIRLWIND I COMPUTER.

To: Jay W. Forrester

From: Robert R. Everett

Date: November 10, 1947

This memo considers briefly the problem of accumulating products in WHIRLWIND I without the necessity for storing the partial sum in the memory at each step of the process. Such accumulation of products will not be included in the original construction but can be added later or included in future designs for any application for which the operation is sufficiently valuable. I would suggest the following:

1. That the problems be accumulated in a sixteen digit shifting register similar to the B Register which is so arranged that on shifts and carries it will shift one step to the right and at the same time insert its right-most digit into the left-most digit position of the accumulator. Suppose then that we are in the middle of the product accumulation process. The sum of the products to date is in this special register which I shall call the Holding Register, HR. We will now order the next multiplication by a special multiplication order which I shall call <u>ma</u> for multiply and accumulate. I think at the moment that it would be better to use a special multiplication order for the accumulation process rather than use a special storage order later on for clearing the holding register. This will enable us to carry out sequences of other operations, including normal multiplications, between steps of the accumulation process. The <u>ma</u> operation proceeds as in the normal multiplying round-off operation, <u>mr</u>, up through time pulse 1 when the multiply pulse turns the control over to the multiplication control inside the arithmetic element. The multiplication process is exactly the same as far as the existing arithmetic element is concerned but in this special case the shift and carry pulses are also supplied to HR, shifting its contents one step to the right and shifting its right-most digit into the AC^0 position of the accumulator. The next multiplication addition will add the multiplicand on top of the shifted partial product plus whatever has been inserted from HR. When the multiplication process is over, the entire contents of HR will have been added into the accumulator in proper sequence. The carry will have been properly cared for and no additional time will have been required for this accumulation.

Consider now Figure 76 in the Block Diagram Report R-127. This figure is the timing diagram for the multiply and round-off operation. The multiply pulse occurs on time pulse 1. Following the additions of the multiplication, the control is returned to the main time pulse distributor.

Time pulse 2 orders the carry and round-off operations which are still needed. In order to get the extra time required for replacing the sum in the Holding Register, we will move the product sign pulse from time pulse 4 to time pulse 3, where it will occur at the same time as the clear BR pulse. At the end of time pulse 3, the correct sum of products to date will be in the accumulator. On time pulse 4, therefore, we can transfer this sum back into the Holding Register. It will be necessary to invert the shifting of zeros and ones from the right end of the Holding Register to the left end of the accumulator, depending on the position of the sign control flip-flop in the arithmetic element. Or the contents of HR can be complemented as well as AR and AC.

2. I can see no objection to this process at the moment. Very little change is needed in the main control. The extra Holding Register which can be made identical to a B-Register must be added, as well as connections from its right digit to the left digit of AC. The greatest change required in the computer is a set of gate tubes which will allow reading the contents of the accumulator back into HR at the completion of the <u>ma</u> operation. A possibility to be considered, particularly if this device is added after WHIRLWIND I has been completed, is to shift the contents of the accumulator back into HR, particularly since, if HR is made like BR, it will be able to shift left. Then, if we provide a special shift-left line, including a pair of special shift-left gates on AC zero, that is, gates which are different from the divide shift-left gates, we can shift the entire contents of AC back into the Holding Register without the necessity for adding an extra row of gate tubes. If this is done, it will be necessary to use the step counter to count the number of operations. This can be accomplished by resetting it to its -16 position, using probably the same line that is used for the multiplication operation. Under these circumstances an extra flip-flop will be required in the arithmetic element which can be pulsed on time pulse 4 which will in turn shut off the main control, reset the step counter, supply Holding Register shift-left pulses to both Holding Register and Accumulator, count up 16 shifts, then clear the Accumulator and return the control to the operation control. The transfer pulse can be delayed a half-pulse time and used for clearing the accumulator.

3. We still need a means for getting the product sum out of HR to send it to storage, when the summation is complete. This can be done in several ways:

(a) Provide a special order which will transfer the contents of HR into AC by shifting on request.

(b) Provide another multiplication and accumulate order which, instead of transferring the sum back to HR on completion, will instead leave it in AC.

(c) If it is considered not undesirable to lose the advantage suggested above of being able to carry out other multiplication operations between summations, the standard multiplication order can be modified. Always shift in the contents of HR, it being the special ma multiplication operation only which replaces the sum in the Holding Register. A normal sequence for summing multiplications will then consist of all ma's except for the last one which would be a standard mr and would end up with the total sum in the accumulator.

Robert E. Everett
Robert R. Everett

RRE:hcs

CONFIDENTIAL

6345
Memorandum M-158

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BLOCK DIAGRAMS, INPUT AND OUTPUT

To: Jay W. Forrester

From: Robert R. Everett

Date: November 10, 1947

The film input and output to be used with Whirlwind I is described briefly in a report by the Eastman Kodak Company entitled "Progress Report #1: Film Reader-Recorder for use with Computer" by R. D. O'Neil. A single unit with modifications is used for both purposes. Reader-Recorders are needed at the set-up typewriters, at film comparison stations, at the inputs and outputs from the computer, and possibly at output printers. These uses plus an estimate of the total number of units required for Whirlwind I are discussed in M-73.

Briefly, these machines consisted of a clutch controlled 35 mm. film drive plus an optical system and a combination of a cathode ray tube and several photocells for putting information on the film or taking information from the film. In writing, the beam of the cathode ray tube is swept across the surface of the tube which is supplied with a mask and focussed on the surface of the film. Both numbers and their complements or inverts are stored on the film. If all is being stored, the beam is left in the number row while if a zero is to be stored, the beam is deflected to the complement row. Information is stored in binary notation as a series of opaque or transparent squares on the surface of the film. Approximately 50 channels are to be used. A beam-splitter is used to deflect some of the beam's light to a pair of photo-cells, which both determine whether a zero or a one has been stored and supply control pulses for indexing the beams.

In reading, much the same system is used except the beam is swept across the face of the tube without vertical deflection, first across the number line and then across the complement line. Photo-cells behind the film pick up signals whenever the beam strikes a transparent spot. For further details see the Eastman Report.

The characteristics of this system are as follows:

1. Since the beam is swept in time across the face of the film, the digits are stored or read in time sequence and must be supplied to and received from the reader-recorder in time sequence, that is, serially.

2. When recording the recorder can transmit back to the computer the actual number stored.

3. When reading, the reader sends to the computer not only the number but the complement of the number. 2. and 3. may be used to give a quite thorough check on the reader-recorder.

4. As each digit is stored or read the reader-recorder can supply a pulse to the computer requesting the delivery or reception of the next digit.

5. The film stores about a hundred lines of data on a linear inch of film. A word may require either one or two lines depending on the length of the word being stored. A twenty-five binary digit word, satisfactory for Whirlwind I, could be stored effectively in one line although actually the word itself will be stored on half of one line and the complement of the word on half of a succeeding line. The lines being interleaved in such a fashion as to use all the surface of the film. If fifty-digit data were being recorded two whole lines would be needed although these lines might again be cut up into four or more lines interleaved so as to cover the entire surface of the film.

6. The film moves at a speed of approximately twenty inches per second allowing a reading rate of the order of 1,000 words per second. The beam of the cathode ray tube, however, in sweeping serially across the film, sweeps in approximately fifty micro-seconds. This time is short enough so that the linear travel of the film during the sweep does not produce an appreciable alignment problem. Information must be supplied to the reader-recorder or received from it either at .5 megacycle rate or at a 1 megacycle rate depending upon the number of digits being stored and the particular storage arrangement being used.

7. In recording, a glass wheel in the recorder contains an index mark which is used for spacing the words equally along the film. In reading, an index placed in the margin of the film during the recording is used to indicate when a word is in the reading position. In both cases the reader-recorder supplies the ready information to the computer. Since about one millisecond elapses between readings of words, the computer has adequate time for its own control operations.

Since the reader-recorder is relatively slow in operation when compared with the rest of the computer, it has been felt desirable to build special equipment for connecting the reader-recorder to the computer. This special equipment will allow the transfer of information in either direction with only a very short interruption of the main computer cycle. This extra equipment can be avoided if the loss of time resulting from using the main computer equipment can be tolerated. A proposal is discussed in this memorandum for automatically obtaining information to be recorded from or read to the main storage of the computer without the intervention of the main control. It is still not clear whether this additional equipment is desirable. It may be that at first at least, the Whirlwind I computer will avoid this special automatic equipment. The equipment can be added later if desired. The decision must wait until further study has been made both of the cost of the special equipment in extra computer complexity and size and the saving in operating speed and in coding. The system will be described here plus mention of how the same operations can be carried out using normal computer orders and equipment.

D-39395 shows a pair of reader-recorders and the equipment necessary for connecting them to the bus of the computer. This equipment consists largely of a pair of stepping or shifting registers which have a number capacity equal to the digit length of the machine. This will be sixteen digits in the case of Whirlwind I. A pair of registers is needed for checking purposes. The pair of registers is referred to as SR, the particular registers being called SRN for the number stepping register and SRC for the complement stepping register. One pair of these registers will suffice for handling both reader and recorder although more stepping register pairs can be added if higher input and output speeds are desired.

The recording process is as follows:

1. The number to be recorded (the source of this number will be discussed later) comes in from the bus to the number stepping register through GT01. From there the complement of the number is transmitted to the complement stepping register through GT04.

2. When the index mark in the recorder shows that the film line is in the right position, the recorder will send out a stepping pulse to the number stepping register thus shifting its right most digit off into the out lines and from there to the recorder.

3. The recorder will store a 1 in either the number or the complement line depending upon whether the number shifted in was a 1 or a 0. The beam splitter photo tubes will send a signal back to the left end of the number stepping register, transferring a 1 if a 1 were stored or a 0 if a 0 were stored. If the system is working properly the digit shifted off the right end of the stepping register will be replaced in the left end.

4. The beam-splitter signal will also generate another stepping pulse to the number stepping register. This process continues until the entire number has been sent to the recorder. When the beam has finished sweeping, it will actuate a photo-cell which will stop the stepping process and send out a signal on the complete line.

5. The number which has actually been recorded will have been replaced in the number stepping register. The actual stored number is again added to the complement stepping register clearing it to all zeros unless a mistake has been made in the recording process. A check pulse to the complement stepping register will check to make sure that the register has been cleared and will produce an alarm if any error has been made.

The reading process is as follows:

1. Both the number and complement stepping registers are cleared to begin with.

2. When the index mark of the next word has reached the reading position, the reader cathode ray tube will start to sweep. Assume for the moment that the number line is swept first and then the complement line, although this process may be different when the final interleaving method has been determined. The reader will then first provide ones or zeros to go into the left end of the number stepping register.

3. As each digit is read, the reader will send a stepping signal to the number stepping register and will at the same time, insert the read digit in the left end of this register.

4. When the beam has finished sweeping the actual number read will be in the number stepping register. The beam will then start over and read the complement line.

5. Stepping pulses are then sent to the complement stepping register and digits inserted in its left end until the entire line has been swept.

6. The number is now in the number stepping register and the complement in the complement stepping register. The number can then be read through its complement output gates to the complement stepping register clearing it unless there is a discrepancy between the two readings. Once again a check pulse is sent to the complement stepping register causing an alarm if an error has been made.

There are also stop start lines to the reader and recorder for engaging and disengaging the clutch drive on the film.

It would be possible to use the accumulator in the arithmetic element as the stepping register for recording, comparing it later with the actual number to be recorded, once again extracted from storage. The accumulator can also be used in reading, the number being read into the accumulator first and stored and then the complement being read into the accumulator, which is also used for the comparison process.

It is possible with only slight modification to the existing control to use the standard orders already available for supplying information to the stepping registers when recording and extracting information from the stepping registers when reading. Signals from the readers and recorders could be transmitted to the control, breaking into the main sequence at come strategic point and calling in a sub-program particularly designed for the reading recording process. The computer could keep indexes in the storage for locating the source of numbers to be recorded or the destination of numbers read. Certain special input and output orders would be needed for starting and stopping the reader-recorders and for transmitting information to and from the stepping registers. Once the relatively small group of operations necessary to set up a new word had been performed, the computer could then return to its regular computing sequence.

A possible way of taking care of the reading and recording sequences automatically will now be discussed. This way has the following characteristics:

1. A section of the regular electro-static storage is designated as a sort of buffer between the main computer and the input and output equipment. The size of this buffer storage is arbitrary and depends upon the amount of reading or recording being done. The use of part of the electro-static storage for this purpose does not in any way prevent its use for normal computer purposes except at those specific times when the input and output are being used.

2. The number of registers in this storage would probably be a power of two. The register section could then be considered as a ring or sequence. Numbers going into the storage would go into the first empty register in the top part of the sequence while numbers being extracted from the storage could come from the first full register on the lower part of the sequence. If the sequence is considered as a ring, this process can continue as long as there are any full registers or any empty registers in the amount of storage allocated.

3. In order to use this ring automatically, it will be necessary to keep track of three things:

   a. the register number of the first full register, used for extracting information from the storage.

b. the register number of the first empty register, used for entering information into the storage.

c. the number of full registers in the storage. This number must be kept track of since special steps must be taken if the storage section becomes either completely empty or completely full.

Drawing B-39396 shows this system as applied to the recording operation. The in-counter keeps track of the first empty register position in the storage and is indexed every time a new number is entered. The out-counter keeps track of the first full position in the storage and is indexed each time a number is extracted. The difference-counter counts positively for numbers added and negatively for numbers extracted. The recording process is as follows:

1. Whenever the computer has a number it wishes recorded it transfers this number to the storage, using the in-counter reading to select the register in which the number is to be placed. The difference-counter keeps track of these insertions and when the storage ring has been filled to a certain pre-determined amount, it starts up the recorder. When the index mark in the recorder has reached a recording position, the recorder sends a complete signal to the control, thus, setting the flip-flop shown in the lower left-hand part of the drawing and opening GT05. It is not possible to break into the standard computing sequence at any time because so doing may destroy a part of an order incompletely carried out. However, when time pulse number 1 occurs a new operation is just starting. The arithmetic element may be working on some old information but the arithmetic element is not needed for the recording process about to be described. Time pulse No. 1 therefore is supplied to GT05, and thus produces a pulse to initiate the recording operation only at this selected part of the operation cycle.

2. The pulse coming from GT05 first stops the main time-pulse distributor, thus stopping the computing process. This pulse also reads out the information from the out-counter as to the first full register in storage and also goes to the electrostatic storage control where it initiates the extraction of this register number.

3. The storage switch automatically accepts the out-counter reading and no further action occurs until the electrostatic storage has been set up.

4. The single pulse from the electrostatic storage control, which is normally used to index the main time-pulse distributor for selection of reading or recording

in the storage, is instead supplied to GT06. This gate tube is normally open but is shut when the recorder flip-flop has been set. Instead, GT07 is on and the single pulse from the electrostatic control passes through this gate tube, returning as a read-out signal to the electrostatic storage control and opening the input gate tube on the number stepping register. The information in the desired storage register is thus transferred to the stepping register.

5. The electrostatic control then proceeds with the re-storing operation in the electrostatic storage. When this operation is complete the control returns a restart pulse to the main control clearing the recorder flip-flop and re-starting the main time-pulse distributor. This distributor will proceed with time pulse number 2, the interpolation of the recording selection process having had no effect upon the main computing sequence.

This process proceeds, the computer inserting new information in the storage ring and the recorder extracting information from the storage ring. If the difference-counter finds that the ring has filled up, thus showing that the computer has gotten ahead of the recorder, it will stop the computing process. The recorder will continue. When the ring has been emptied the difference-counter will again start up the main computer. If the recorder gets ahead of the computer to the extent of emptying the storage ring the film recorder and the recording process will be stopped and not re-started until the difference-counter shows that the ring has at least partially filled.

Drawing B-39397 shows how this system can be applied to the reading process. The in-counter again keeps track of the first empty register in the ring except that now it is supplied with pulses from the reader and not from the control. The out-counter again keeps track of the first full register in the range but it is now indexed from the control since it is the computer itself which is extracting information from the storage ring.

The difference-counter is again indexed with plus pulses from the in-counter and minus pulses from the out-counter. Gates are now provided for reading numbers in from the bus to the difference counter. It is sometimes desirable for time economy to read in only a few numbers from the reader, perhaps as few as one. The computer can then transfer a number to the difference counter sufficient to merely fill it. If the reader is then started, it will read only enough numbers to fill the counter, thus stopping the reading process. The counter must then be cleared.

An index counter is also provided for selecting a particular number or group of numbers on the film being read. The computer can read into this counter the number of words from the word last read to the next desired word on the tape. As the reader film moves past the index photo cell, it will send out index counts to this index counter. When the desired number of words has passed by the index photo cell, the index counter will send out a start order beginning the reading process. If this counter is used in connection with presetting the difference counter any desired number of words can be read at any place in the film. Orders are necessary for running the film in two directions. Check numbers can be inserted on the films at desired points so that the computer can have a check on whether the film is in the desired position.

It is not planned at present to provide scanning speeds in the film readers and recorders. Thus it is possible to read or record at the maximum speed at which the film can travel. At the expense, therefore, of a certain amount of computing speed, it would be possible to accomplish this scanning process using only the standard orders in the computer and allowing the actual numbers to be read from the film at each step. The computer would simply not put the information in storage until the proper word had been reached. The computer could keep track of the index number itself using the arithmetic element as the counter.

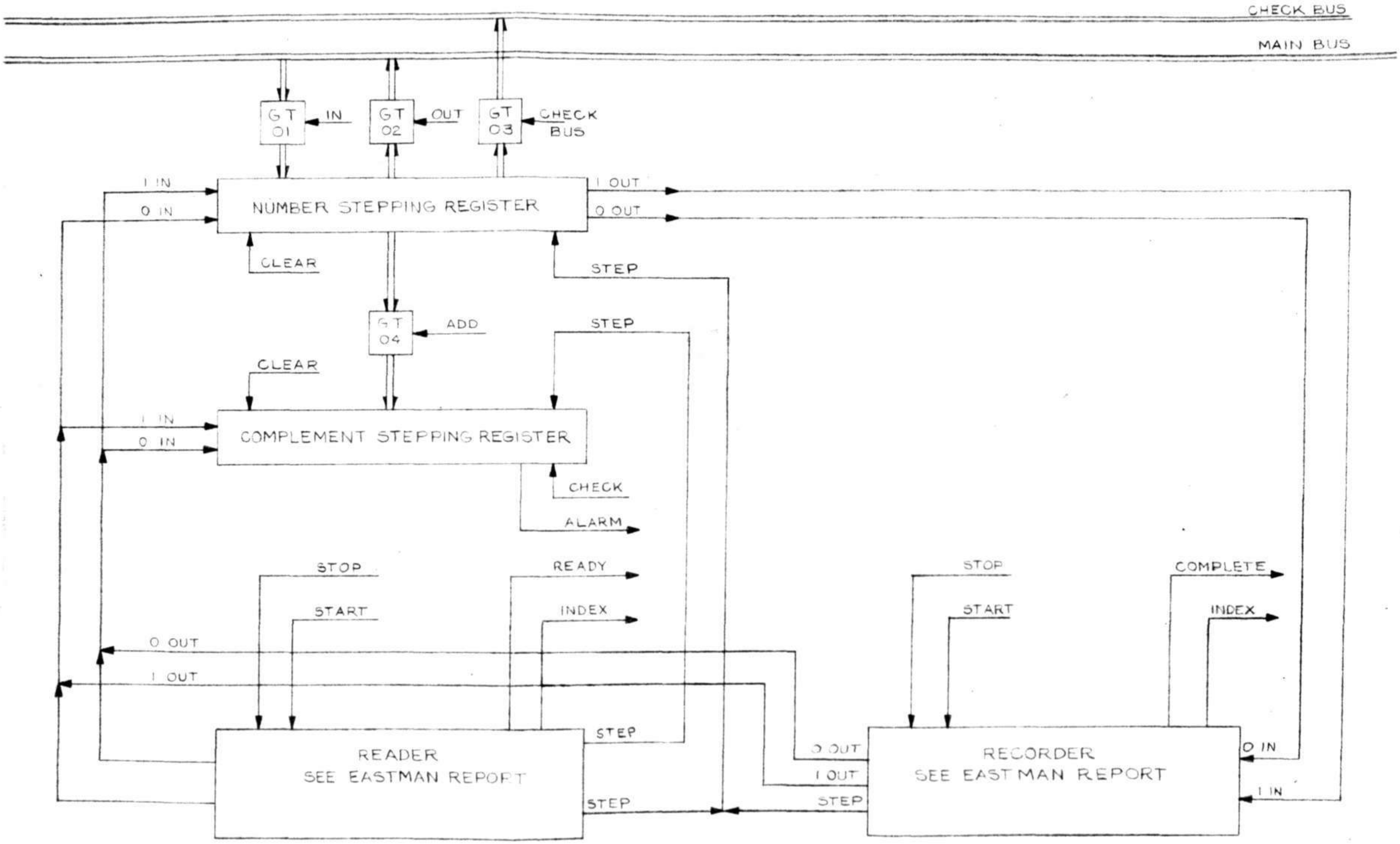
Robert R. Everett

Robert R. Everett

Drawings: B-39395
B-39396
B-39397

RRE:BB

B-39395

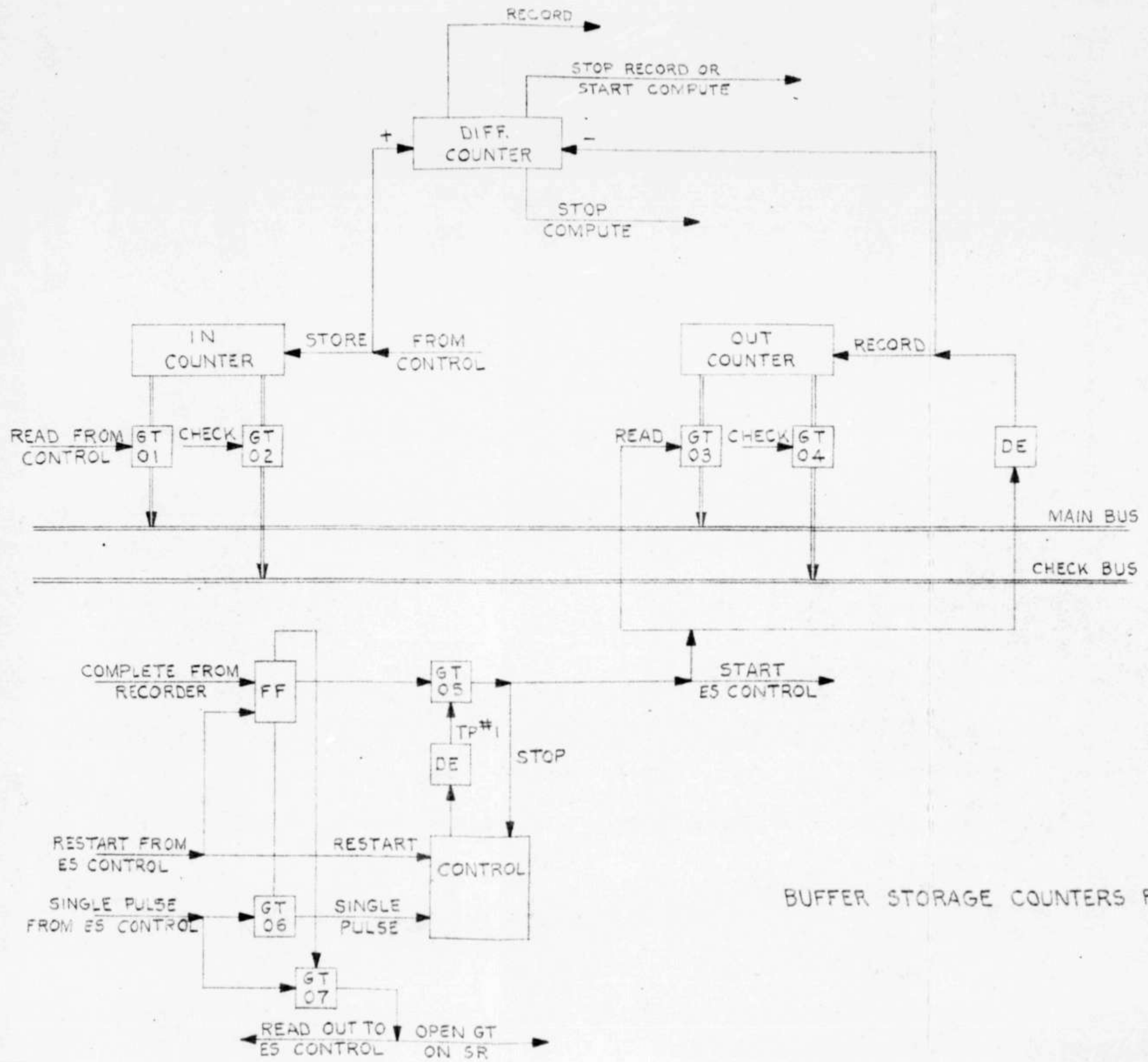


FILM READER & RECORDER FOR
WWI

USED IN MEMO 158 6345

B-39395

B-39396

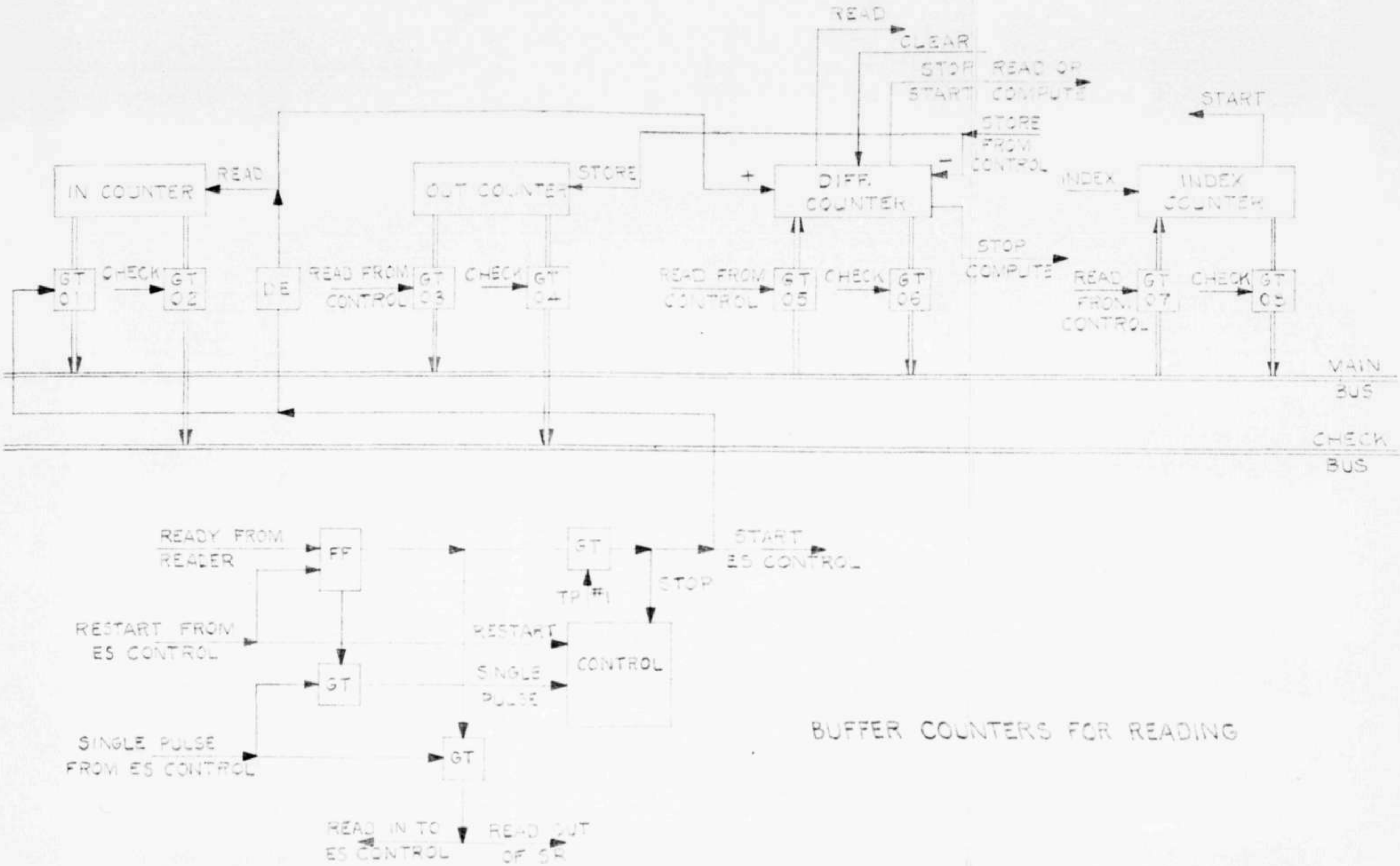


BUFFER STORAGE COUNTERS FOR RECORDING

USED IN MEMO 158 6345

B-39396

B-39397



BUFFER COUNTERS FOR READING

USED IN MEMO 158 6345

B-39397

CONFIDENTIAL

ENGINEERING NOTES NO. E-26

TO: Engineers of Project 6345 — Project 6345

FROM: Peter D. Tilton —

SUBJECT: Description of Computer System - Type IA

DATE: August 12, 1946

FORNWORD

This description of a particular form of high-speed computing system is not intended to be a complete discussion of the many problems of electronic digital computation and does not attempt to fully explain the considerations leading up to the result presented. This is simply a description of what the system is and how it works.

Nor, does this outline consider fully the fact that even a complete result is not necessarily final. One possible modification to expand the power and usefulness of the system is given in Appendix A, and further additions and improvements are already in prospect. Future trends, as well as past deliberations, are deemed to be beyond the scope of this description of the system's characteristics.

As a guide to a better understanding of the system, it is recommended that the reader be familiar with the terminology used in the computing field in general, and by this project in particular.

The predication of this system upon types of physical equipment still under development has made a considerable number of "assumptions" necessary. These assumptions are given as such, and, in general, it is not possible to justify them as being anything more than guesses. When more reasonable information is available in the form of physical experimental data, a re-evaluation of the system can easily be made.

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DESCRIPTION OF COMPUTER SYSTEM - TYPE IA

1. General Objectives of System

1.1 To provide a simple system which can be used to study more complicated operations in terms of what can be accomplished with the basic tools of addition, subtraction, multiplications, and sub-program cycles.

1.2 To provide a basic system arrangement for performing simple arithmetic operations to which equipment for the more complicated or specialized operations of division, square rooting, integration and interpolation may be added.

1.3 To provide a specifically defined system for a study of timing considerations, and the functional relationship of the various types of specialized equipment now envisaged. To this end many of the system characteristics have been arbitrarily defined more specifically than is reasonable at the present stage of development, with the understanding that changes will have to be made as more information becomes available.

2. Specifications Which Are Derived from the Basic Assumptions of Summary Report No. 1, April, 1946

2.1 Serial operation will be used insofar as possible.

2.11 Serial digit transmission will be used.

2.12 Words transmitted to computing element will use parallel channels.

2.13 Serial order transmission and serial switching set-up means will be used.

2.2 Binary base will be used for number representation.

2.3 A Fixed Point System will eliminate the need for automatically handling the location of the point in the machine.

2.31 The reference point will be taken as one digit in from left side of number register.

2.32 A scale factor of some power of 2 (for binary base) is used to reduce all positive numbers to appear in the register as lying between 0 and 1.

2.33 Scale factors are introduced in problem preparation and must always be accounted for although they never appear in the machine.

2.331 Numbers to be added(or subtracted) must have the same scale factor, which is also the scale factor of the answer.

2.332 Any two numbers may be multiplied but the scale factor of the result depends on the rounding-off process as well as the scale factors of the multiplicand and multiplier.

2.333 Scale factors must be chosen to avoid a result which runs off the number register in either direction.

2.4 The digit PRF is assumed to be 1 MC, with 1/4 microsecond pulses.

3. Numerical Treatment

3.1 The number register will consist of 32 digit spaces(excluding intelligence pulse).

3.2 Digit pulses will be transmitted in time sequence with the least significant coming first, and the sign digit being the last, i.e., right end of number register comes first.

3.3 The number register will be preceded in transmission by a single Intelligence Pulse, IP, making a transmitted length of 33 digits.

3.4 All negative numbers will appear as complements on two, thus looking like positive numbers between 1 and 2. They are distinguished by the presence of a pulse in the sign digit space, which is the last one transmitted.

3.5 The arithmetic operations of addition, subtraction, and multiplication will be provided.

4. Further Assumptions Regarding Electrostatic Storage Tubes

4.1 Dynamic storage elements (ST type) will be capable of being "read" several times to permit use of the same number several times in a problem without the necessity of restoring it every time it is used. (There is at present no experimental confirmation of this possibility.)

4.2 Storage elements will be able to receive and interpret their "set-up" orders even while still in the process of executing the previous order. It is to be understood that execution of the later order will not be initiated until after completion of the previous one.

4.3 Storage elements are each assumed to hold 32 "words" of at least 32 digits.

5. Equipment

5.1 Computing Element Characteristics

5.11 The operations of addition, subtraction, and multiplication will be performed as follows:

5.111 For addition, a basic adder will be modified with an added provision to give a warning if improper scale factors have been used on the numbers being added.

5.112 For multiplication, a whiffle-tree multiplier which will accommodate negative as well as positive numbers is used for high speed. Rounding-off normally occurs at the middle of the product but can be done at other points. The last partial sum of the product is made in the adder.

5.113 For subtraction, the complement on two of the minuend will be formed andthis is added to the subtrahend in the adder.

5.12 The computing element will act like a 40 microsecond delay for all operations, i.e., there will be 40 μ sec. from the start of the numbers in until the start of the result out. This delay is necessary to allow a time of one word length for erasure of the storage tube which is to receive the result, plus enough extra time to insure full recovery of the sweep circuits (here arbitrarily assumed to be 8 μ sec.)

5.121 Additions and subtractions are purposely delayed more than one word length.

5.122 A multiplication is normally delayed one word length and in this system, the result is delayed a little more to make a total delay of 40 μ sec.

5.2 Storage Capacity

5.21 Live storage will be used to store partial answers or transient results.

5.211 ST, electrostatic type (cathode-ray tubes) will be used.

5.212 Seven tubes will provide storage for 224 words.

5.22 Program and sub-program storage will contain the orders for solution of a problem.

5.221 OR, oscilloscope reader type (card readers) will introduce the coded orders into the system from a set of punched cards or a similar medium.

5.222 Sixteen units will provide storage for 512 words.

5.23 Dead storage will contain constants and tabulated data.

5.231 Oscilloscope Reader type used here also.

5.232 Seven tubes will provide storage for 224 words.

5.24 Recording, for results.

5.241 For simplicity only one unit is provided.

5.242 Type is not specified, but it might be electric typewriter, curve plotter, or oscillograph.

5.3 Switches will be high-speed electronic type.

5.31 A 15-way program storage switch is used to select each order from the program storage tubes.

5.32 A 15-way storage selector switch sends the storage tube orders to the proper live or dead storage tubes.

5.33 A computer switch separates the order to the computing element.

5.34 A sub-program switch separates a sub-program order if one is present.

5.35 Others are shown as required in the various components.

5.4 Timing devices for synchronizing the operation.

5.41 A timing pulse generator provides pulses at master clock PRF of 1 MC.

5.42 Trigger generator provides synchronizing pulses at 25 KC PRF for timing various parts of the operation cycle.

5.5 A program selector controls the sequence of orders.

5.51 It chooses program orders in numerical sequence and produces the corresponding switching orders.

5.52 It also provides a means for interrupting the main program sequence with a sub-program cycle and returns control to the proper place in the main program at the end of the sub-program cycle.

5.53 A reset order will start a new program cycle by returning the program selector to the beginning of the program.

6. Operation

6.1 Fundamental Circuits are described and explained on the following drawings, which should be studied in the order given for best results. The symbols used throughout are shown and defined on B-37000.

6.11	Gate Generator(GG)		Drawing B-37012
6.12	Gate Tube(GT)		" B-37011
6.13	Pulse Cutoff(PC)		" B-37014
6.14	Digit Inverter(DI)	See	" B-37017
6.15	Electronic Switch(ES)		" B-37013
6.16	Basic Adder		" B-37015

6.2 Components

6.21	Computing Element	Drawing B-37022 C -37023
6.211	Adding Element	" B-37016
6.212	Multiplier	" C-37018 C-37019
6.213	Complementer(CC)	" B-37017
6.22	Storage Units	
6.221	Oscilloscope Reader(OR)	Drawing C-37021
6.222	Storage Tube(ST) (Electrostatic)	" C-37020
6.23	Program Selector	Drawing B-37026

6.3 Orders and Timing

6.31	Composition of Standard Orders	Drawing B-37024
6.32	Time Cycle	" B-37025

6.4	System	" D-37030

The following sections, 6.41, 6.42, 6.43, and 6.44, trace through a complete operation, which can be followed on the Time Cycle Drawing B-37025, as well as on the system Block Diagram D-37030. Other characteristics and features of operation are described in the subsequent sections.

6.41 Program Order Selection

6.411 Program selector counts the triggers on Trunk T'.

6.412 The order is selected by a tube number and its position on the tube according to the count registered by the program selector.

6.413 The counted number represents a switch order and a tube line number on the tube selected by the switch.

6.414 This coded line number from the selector is switched to the proper program storage tube and sets up the proper deflection voltage for the order desired (Line 4 of Time Cycle, B-37025).

6.42 Initiation of Program Order

6.421 Alternate triggers appear on trunk lines T' and T''.

6.422 Trigger on T' reads first word of program order onto trunk line O. (Line 5 of Time Cycle)

6.423 Trigger on T'' which is more than one word length later than that on T' reads second word of order onto O.

6.43 Disposition of Order (See also Composition of Orders, B-37034)

6.431 First section of order, which is to set up the storage tube to read one number into computing element on trunk line A operates storage selector switch to send the rest of the section, designating the tube line number, to the proper storage tube.

6.432 Second section of order sets up the tube to read the second number into the computing element on Trunk line B.

6.433 Computer switch and gate separate the third section of the order and send it to the computing element to select the operation desired.

6.434 Fourth section of order is similar in action to first two sections but sets up the storage tube to receive the result from the computing element on trunk line C.

6.435 Fifth section of order is present only when next order is to be taken from a sub-program cycle. It is separated by the sub-program switch and is used to arrest the normal counting procedure in the program selector as well as to select the proper program storage tube and line number for the sub-program order desired.

6.44 Execution of order

6.441 A trigger on Trunk T'' causes two numbers to be read out of storage, one onto Trunk A and one on B. (Lines 6 and 7 of the Time Cycle).

6.442 The same trigger causes the live storage tube on Trunk C to erase, preparatory to receiving the result to be stored. (Line 8 of Time Cycle)

6.443 The numbers from A and B are held in the computing element until the tube on C is ready to store the result.

6.444 The elapsed time between the initiation trigger on T' and the storing of the result from the computing element is about 200 μ sec.

6.45 Characteristics of Orders

6.451 The first and second sections, designated A and B, may set up either electrostatic storage tubes or oscilloscope readers on trunks A or B. The tubes on these trunks will always be set up for reading.

6.452 The fourth section of order, designated C, always must set up an electrostatic storage tube or the recording instrument to receive the computer result on Trunk C.

6.453 The fifth section, designated S, which will select the next order to be read when a sub-program cycle is used, is included only in those orders which require the next order to be part of a sub-program. Each sub-program order, <u>except</u> the <u>last</u> one of the cycle will contain this section specifying the next step in the cycle, but the other sections will be similar to those of regular orders. The use of section S means that sub-program orders need not be stored consecutively in the program storage.

6.454 The last order of the main program cycle sets the storage selector switch to a unique position reserved for it and is fed back to the program selector to reset the counters to zero, thus starting the program over at the beginning.

6.46 Timing of Operation

6.461 Triggers spaced at 40 microseconds appear alternately on trunk lines, T' and T''. Hence each trunk carries triggers spaced 80 µ sec. apart.

6.462 The triggers on T' are counted in the Program Selector except for sub-program interruptions. Reading of the counters is timed to start after the sub-program section, "S", of the previous order has been read, so that when a sub-program is to start, the counter can be stopped to permit return to the proper place when the sub-program is completed.

6.463 A trigger on T'' starts the sweep of first tube where order is stored.

6.464 The next trigger on T' in addition to starting the program selector for the <u>next</u> order, starts the sweep of the second tube where the rest of the order is stored.

6.465 The second trigger on T'' goes to all computing storage tubes as well as starting the sweep for the first part of the <u>next</u> order. The two tubes which were set up by Sections A and B of the order, sweep and produce the two numbers for the computer on trunks A and B. A tube, set up by section C of the order, sweeps to erase, preparatory to receiving the answer on Trunk C. All other tubes, though triggered, do not produce numbers because they have not been "set-up" by an order.

6.466 While the "C" storage tube is erasing, the "A" and "B" tubes read numbersinto the computing element. The result is held in the computing element until the "C" tube has had time to erase and recover from the erasing sweep, about 40µ sec.

6.467 The answer is stored on the "C" tube when its IP is used as a trigger to start the "writing" sweep.

6.468 A fixed cycling rate of 12.5 KC is used with a provision for overlapping portions of the operations. By staggering things this way, a new operation can start every 80 microseconds in spite of the unnecessary 40 μ sec. delay of additions and subtractions in the computing element.

6.47 Treatment of Sub-program Cycles

6.471 Section "S" of an order contains the coded information designating the location of the next order to be read, i.e., the position of program storage switch to select the desired tube switch and the line number on the tube itself.

6.472 Section "S" is switched off to re-enter the program storage through the program storage switch, where it selects the next order to be used.

6.473 Section "S" also goes to the program selector where it prevents the counters from being read as in normal selection procedure, although the count has already been increased for the next program order.

6.474 When sub-program cycle is complete, the last order has no section "S" and the program selector is released to read the count which was held during the sub-program, thus returning control to the main program sequence without discontinuity in the counting.

6.48 Storage

6.481 The electrostatic storage tubes are always "erased" just before they are required to store a number, guarding against spoilage of the number by possible remains of a previous storing.

6.482 A storage tube can be used in two successive operations, but cannot supply both numbers to the computer.

6.483 Transfer of storage may be made by sending the value to be restored through the adder in the computing element where it is not altered but comes out enough later to allow for erasure of the tube to receive it.

6.484 A [illegible] on an electrostatic storage tube can be used several times but if the signals "run-down" or get weak, the value will have to be restored for further [illegible]

6.485 All operations, except transfer from storage to the recording device will be terminated by the storage of the result on an electrostatic storage tube.

Drawings:

B-37011

B-37012

B-37013

B-37014

B-37015

B-37016

B-37017

C-37018

C-37019

C-37020

C-37021

B-37022

B-37023

B-37024

B-37025

B-37026

D-37030

Peter D. Tilton

Peter D. Tilton

PDT:vc

A.2232 When triggered by the special pulse from a storage tube the switch should change for 40 μ sec. to connect the delay between trunks A and B.

A3. Operation

A.31 Tube is "set-up" by first order, and second order is held.

A.32 Extra trigger admitted from T' is 40 μ sec. ahead of the normal trigger on T'' and reads first number off tube onto Trunk A.

A.33 This first number on A is delayed 40 μ sec. in the added delay before it appears on Trunk B.

A.34 Tube resets to the second order received as soon as the first order is executed.

A.35 Normal trigger on T'' reads second number required onto Trunk A which is now clear of the first number.

A.36 The two numbers appear simultaneously at the computer on A and B and are operated upon and stored in the normal fashion.

APPENDIX A

COMPUTER SYSTEM TYPE IB

A1. Distinguishing Characteristics

A1.1 Type IB will be able to use an electrostatic storage tube in successive operations.

A1.2 Both numbers to the computing element can be supplied from a single storage tube (of either type). It is not possible for a single tube to supply both numbers and store the result in the same operation, or to supply one number and still erase in time to store the result.

A1.3 All other features will be the same as those of Type IA.

A2. Modifications Required of Type IA

A2.1 Storage tube modifications

A2.11 All storage tubes of both types must contain circuits which will be able to hold two set-up orders received one after the other, so that the second order can be "remembered" while the first one is being executed.

A2.12 Associated with the above provision there should be a means for sending a trigger pulse out of the storage tube whenever a double order is received.

A2.2 System modifications

A2.21 A single trigger pulse should be admitted from Trunk T' to all computer storage tubes through a gate controlled by the pulse sent out from the tube receiving a double order.

A2.22 Trunks T' and T'' must be isolated from each other when the trigger from T' goes to the storage tubes to prevent accidentally triggering an undesired program storage tube as well.

A2.23 A 40 μ sec. delay line is required between trunks A and B, connected through a switch as follows:

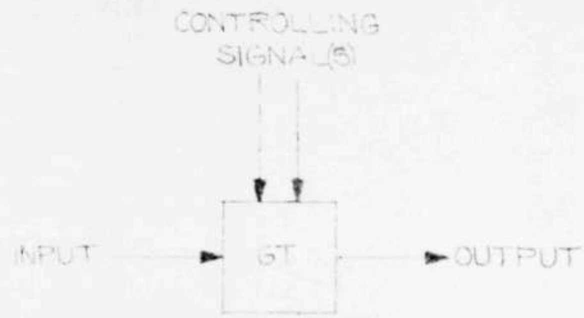
A.2231 Normally Trunks A and B are connected to computing element inputs.

B- 37011-1	TOLERANCES NOT OTHERWISE SPECIFIED:
WO-	DECIMAL ± .005 FRACTIONAL ± 1/64

GATE TUBE (GT)

A Gate Tube is an on-off switch stimulated by an external signal. It may be either normally open or normally closed. In either case presence of the signal causes the opposite connection to be made and when the control signal is removed the switch reverts to its normal position. When the control signal is a pulse the Gate Tube acts as a coincidence timing device to emit a single pulse if a pulse arrives on the input line at the same time as the single pulse control signal. If there is no coincidence there will be no output.

In some cases the switch may be required to operate only when two external signals are applied simultaneously, operation starting whenever both signals are on together and stopping whenever either of the control signals ceases. This is possible only in the case of tubes which are normally off.



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ITEM	MATERIAL - DESCRIPTION	PART NO.	QUAN.

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GATE TUBE - GT

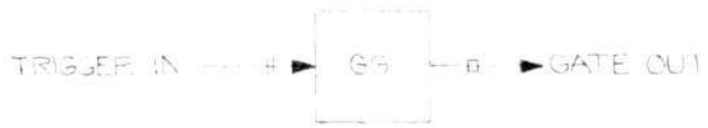
SCALE: DR T. Leary Jr. 6/19/46
TR. PDT 6/27/46 CK. APP.

B- 37011-1

B- 37012 WO-	TOLERANCES NOT OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64

GATE GENERATOR (GG)

The Gate Generator is a device to produce a gating signal of a fixed length, upon stimulation from a single pulse or the leading edge of another gate. Once triggered it will be unresponsive to other pulses or signals appearing on the input line for the length of the gate. The first signal appearing after the end of the gate will start a new gate.



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ITEM	MATERIAL - DESCRIPTION	PART NO.	QUAN.

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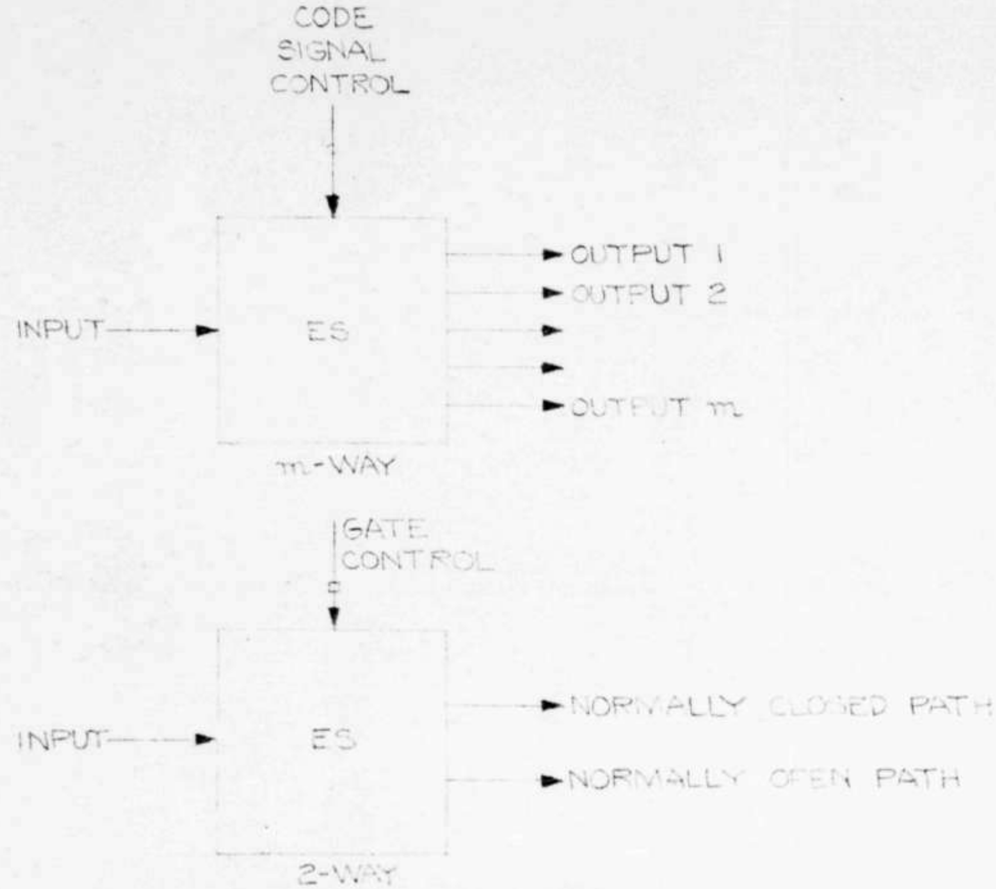
GATE GENERATOR (GG)

SCALE	DR T. Leary [illegible] 6/10/46		B- 37012
TR PDT 6/27/46	CK.	APP.	

B- 37013	TOLERANCES NOT OTHERWISE SPECIFIED:
WO-	DECIMAL ± .005 FRACTIONAL ± 1/64



ELECTRONIC SWITCH - (ES)

A multi-polar contactor which makes a direct contact between an input line and one of a number of output lines, or conversely. Where there is only a two-way choice one way will be normally closed and the other will be normally open. The presence of a positive gate signal on the control line will reverse the normal connections; when the gate is removed the switch will revert to its normal position. In the general case of an m-way switch the control order will consist of a binary number representing the desired connection, i.e. a series of pulses in binary code for a number between 1 and m preceded by an intelligence pulse.

The multi-position switch is shown with a separate input channel for the control order, but it is equally feasible to have the order arrive on the input line in advance of the word to be routed in the switch. In this other arrangement the order would set the switch and hold it long enough to allow the word to pass through, before releasing the switch so that a new order could reset it.

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ITEM	MATERIAL - DESCRIPTION	PART NO.	QU

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ELECTRONIC SWITCH - ES

SCALE	DR. [illegible]	
TR. PDT 6/27/46	CK.	APP.

B- 37013

B- 37014	TOLERANCES NOT OTHERWISE SPECIFIED:
WO-	DECIMAL ± .005 FRACTIONAL ± 1/64

PULSE CUTOFF - (PC)

The Pulse Cutoff is an arrangement for separating the first pulse of a stream of pulses from the rest. It consists of a Gate Generator (GG) and a 2-way Electronic Switch (ES) controlled by the gate. The first pulse arriving on the line triggers the gate which in turn throws the switch, such that the first pulse is passed down one line out of the switch and any following pulses are sent down the other. Because of the nature of the Gate Generator once it has been triggered it emits a gate of fixed length regardless of any successive stimuli for a given period, thus permitting the rest of a group of pulses to be passed on the second switch-output line.

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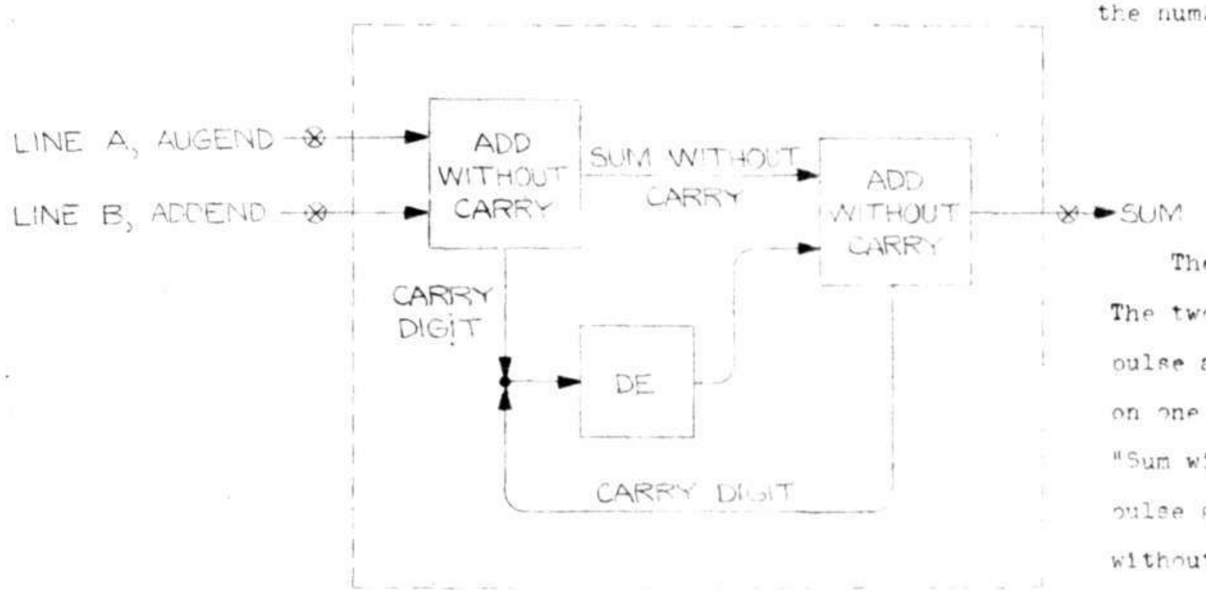
PULSE CUTOFF PC

SCALE: | DR. T. Leary Jr. 6/18/46 | B- 37014
TR. PDT 6/27/46 | CK. | APP.

B- 37015	TOLERANCES NOT OTHERWISE SPECIFIED:
WO-	DECIMAL ± .005 FRACTIONAL ± 1/64

BASIC ADDER



The Basic Adder is a circuit for adding the pulses representing two binary numbers such that the pulses resulting will correctly denote the number that is their sum. To add binary numbers.

1 + 1 = 0 with a carry of 1

1 + 0 = 1 with no carry

0 + 0 = 0 with no carry

The elements labelled "Add without Carry" perform this operation. The two numbers to be added are fed in coincidentally, and when no pulse arrives on either line nothing is the result; if there is a pulse on one line but none on the other a pulse goes out on the line marked "Sum without Carry"; and, if two pulses arrive simultaneously, a single pulse goes out on the "Carry" line but nothing goes out on the "Sum without Carry" line. Carry digits are delayed one digit time in the Delay Element (DE) and are then added to the sum in the second "Add without Carry" unit.

The adder will not properly add two numbers if each has an Intelligence Pulse, because of the generated carry, but when only one number has an IP the answer will have the same IP and will be numerical correct.

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BASIC ADDER

SCALE | DR T. Leary Jr. | TR PDT 6/27/46 | CK | APP. | B- 37015

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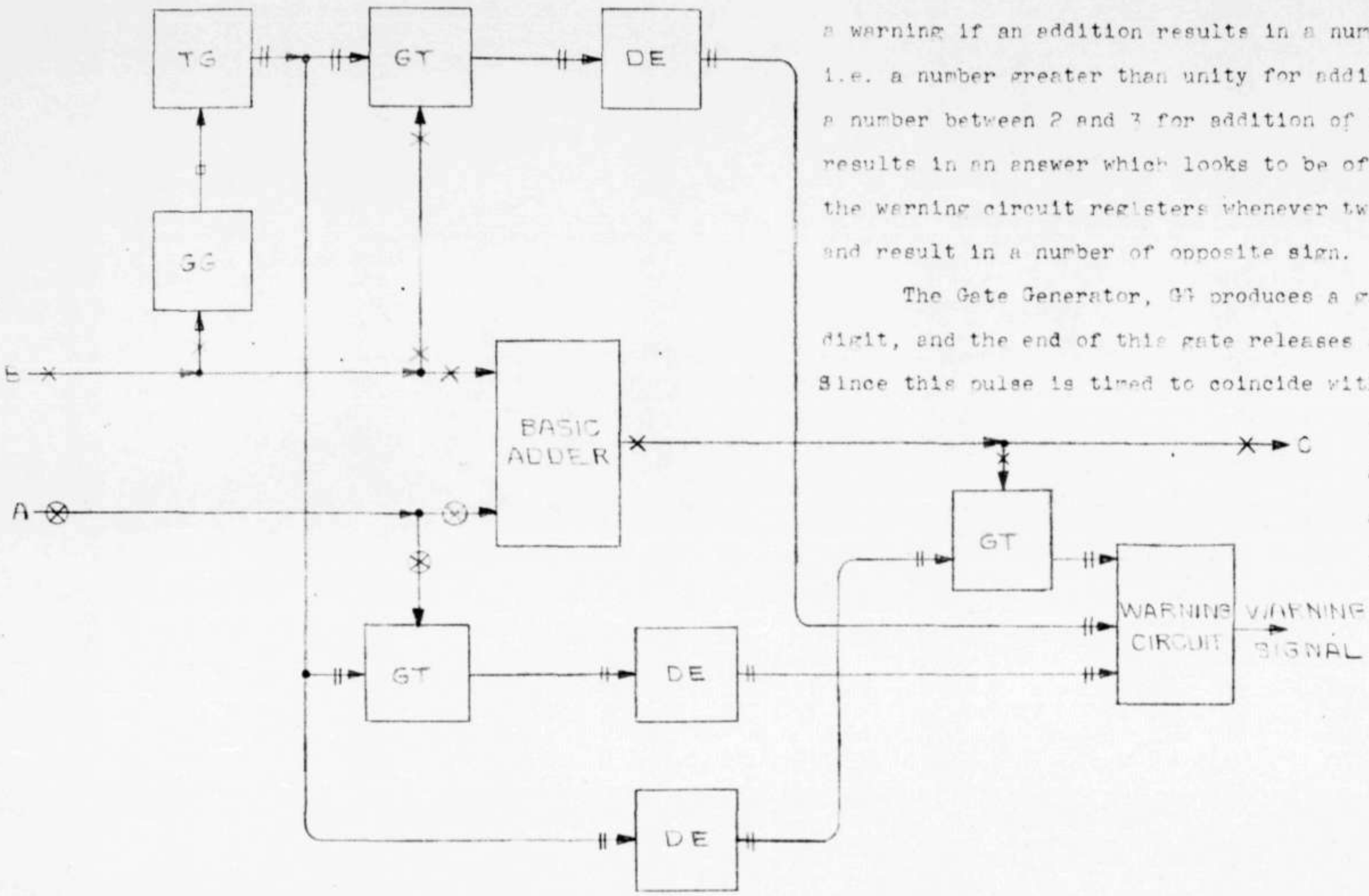
TOLERANCES NOT OTHERWISE SPECIFIED:
DECIMAL ± .005 FRACTIONAL ± 1/64



ADDING ELEMENT

The Adding Element consists of a Basic Adder and a circuit to provide a warning if an addition results in a number which overflows the register, i.e. a number greater than unity for addition of two positive numbers or a number between 2 and 3 for addition of two negative numbers. Since this results in an answer which looks to be of opposite sign from the two originals, the warning circuit registers whenever two numbers of like sign are added and result in a number of opposite sign.

The Gate Generator, GG produces a gate one word-length long less one digit, and the end of this gate releases a trigger from the Trigger Generator (TG). Since this pulse is timed to coincide with the sign digit the two Gate Tubes (GT) make known the sign of the augend and addend. Similarly, the third GT ascertains the sign of the result on trunk C. The warning circuit is actuated only by those time or space combinations which indicate a discrepancy.

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ADDING ELEMENT

SCALE: DR. D.L.O. 5-20-46
TR. PDT 6/10/46 CK. APP.

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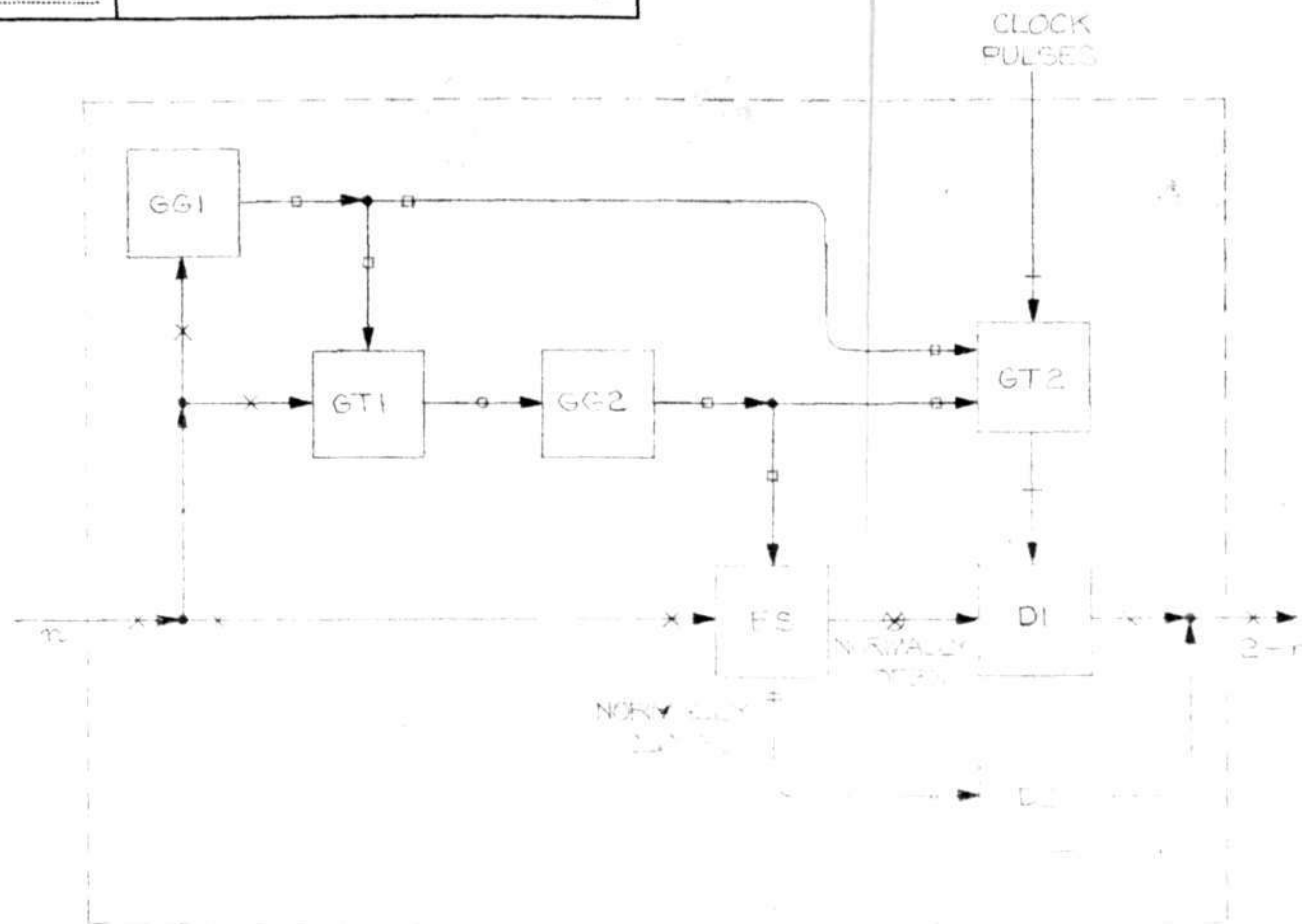
B- 37017	TOLERANCES NOT OTHERWISE SPECIFIED:
WO-	DECIMAL ± .005 FRACTIONAL ± 1/64



COMPLEMENTER - (CC)

A Complementer is used to form the complement of a number with respect to 2, i.e. from a binary number n to form another number 2-n. The complement of a binary number 0.0011011001 is 1.1100101001 where the extreme right hand digit represents the Intelligence Pulse (IP) in both cases and the extreme left hand digit of the complement signifies that it is a negative number. In the complement the IP and all digits up to and including the next digit pulse are the same as in the number while all the rest of the digits are the opposite.

The IP of the number n triggers the Gate Generator GG-1 which actuates the Gate Tube (GT-1) and sends a one-word-length gate to GT-2 as well. The next pulse in n does not affect (GG-1) but starts the gate of (GG-2) which changes the position of the Electronic Switch (ES) thus diverting the rest of n to the Digit Inverter (DI). At the same time, the actuation of GT-2 is completed admitting Clock Pulses to DI.

The DI passes clock pulses for every empty digit space in the number and blocks all the digit pulses. In other words, if a digit space was blank it is given a pulse in DI and conversely. The IP and the first digit pulse which were through the switch before it changed are delayed in a Delay Element (DE) which is just long enough to compensate for the few digit-lengths lost in DI. From DE these two pulses are sent out just ahead of the rest of 2-n. The number 2-n is completed when the gate of GG-1 stops and blocks GT-2.

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COMPLEMENTER (CC)

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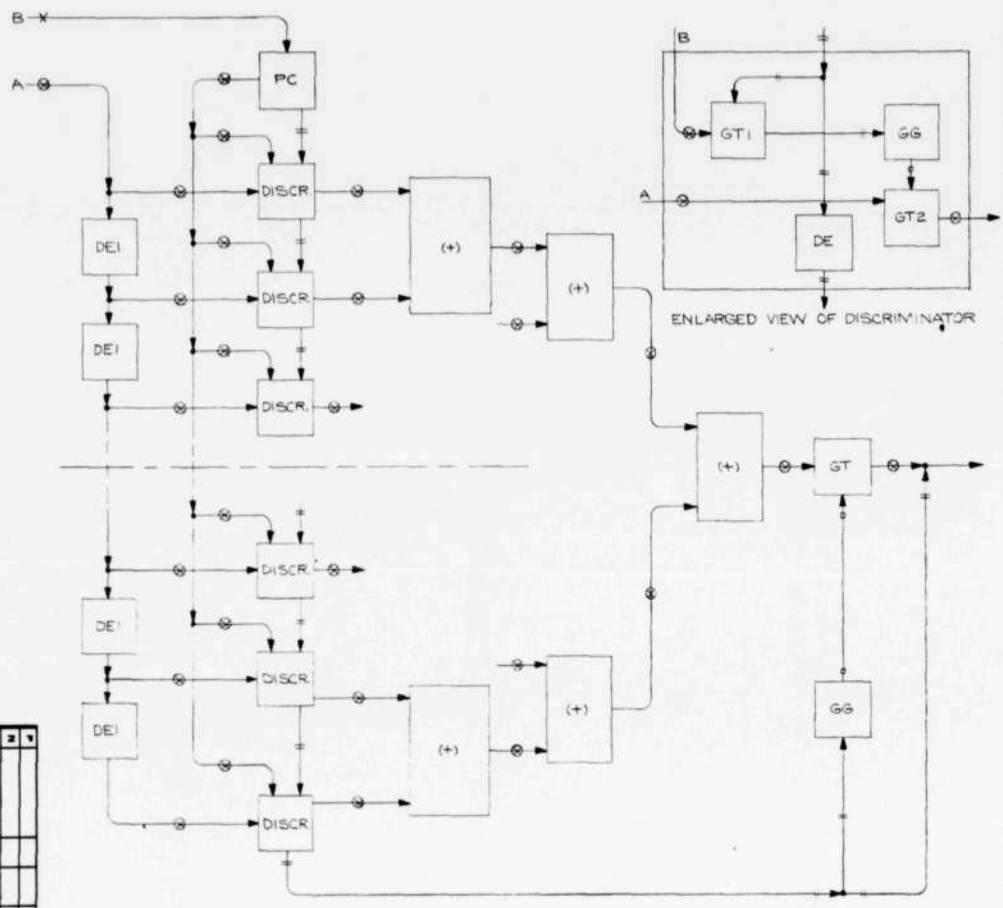

BASIC MULTIPLIER (x)

Multiplication is accomplished by taking the partial sums formed by multiplying the multiplicand by each successive digit of the multiplier and then adding these partial sums in proper time relation to get the total product.

The multiplicand on Trunk A is delayed one digit length in each Delay Element DE-1 for proper timing or staggering in the summing. The multiplier on Trunk B first has its *Intelligence Pulse* removed by the Pulse Cutoff (PC) and then is fed simultaneously to all the discriminators which also receive The I P after it has been delayed one digit length in each. The IP trigger to the Discriminator is thus one digit later in each successive Discriminator and triggers the Gate Tube (GT-1) in each at a time when the next later digit column of the multiplier is on Trunk B. If any such digit column contains a pulse the Gate Generator (GG) of the discriminator opens the Gate Tube (GT-2) to admit the entire multiplicand to the bank of adders, the multiplicand being already timed properly for each line of entry.

After the partial sums have passed through the bank of adders they produce the product which now contains twice as many digit places as the original numbers. *Rounding off without a correction is accomplished by* allowing the first part of the product, (the small or least significant end) to be blocked off by the Gate Tube (GT) which is opened by a gate set off by the IP of the multiplier which has been delayed one number-length in the column of discriminators. This lets the usable half of the product through and at the same time provides the IP for it, completing the operation.

ITEM	MATERIAL - DESCRIPTION	PART NO.	SIGNAL

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BASIC MULTIPLIER

SCALE | DR. T.L. 6/13/46
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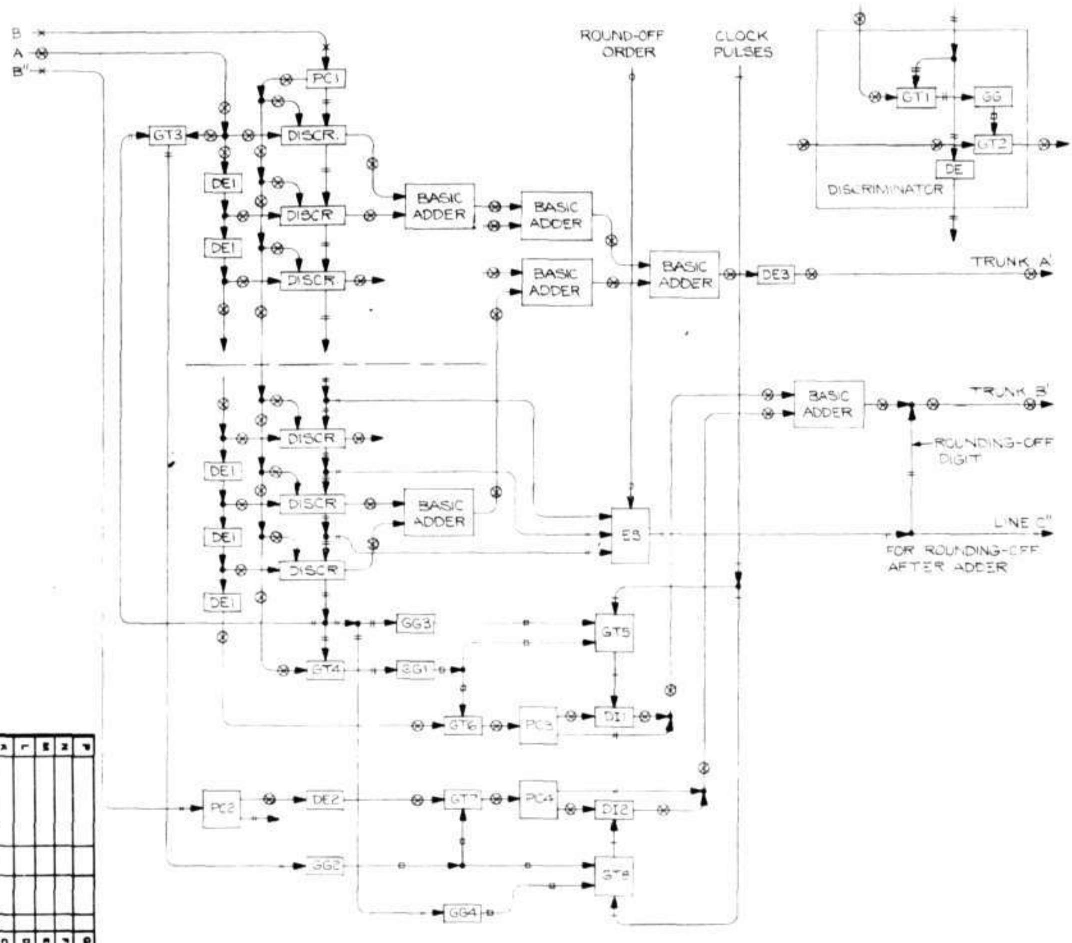
TOLERANCES NOT OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64



MULTIPLIER (x)

The multiplier shown here has been modified to be able to multiply when either or both of the inputs are negative numbers. It also contains provision for rounding-off any result to fill more of the number register with significant digits, i.e., to alter the normal scale factor of the product.

A negative number, n_1 on Trunk A means that the multiplicand is actually $2-n_1$. A negative number on Trunk B, however, acts like a multiplier $1-n_2$, since the sign digit is not admitted to a discriminator. Thus, the resulting products will actually represent:

$$n_1 \times (1 - n_2) = n_1 - n_1 n_2$$

$$n_2 \times (2 - n_1) = 2n_2 - n_1 n_2$$

$$\text{or } (2 - n_1) \times (1 - n_2) = 2 - 2n_2 - n_1 + n_1 n_2 .$$

The proper result can be obtained if the following corrections are made:

For number on A negative	add Complement of twice the multiplier
For number on B negative	add Complement of multiplicand
For both negative	add both corrections above.

The corrections are made when Gate Tube GT-3 and GT-4 detect negative numbers by coincidence of a timed trigger with the last digit column of the multiplicand and multiplier respectively.

The multiplicand is saved in the column of delays DE-1 and if multiplier was negative GT-4 opens GT-6, letting multiplicand through for complementing in DI-1. Multiplier is saved in an external delay and arrives on Trunk B'' where it is doubled by a one-digit delay DE-2 and then is let in to be complemented in DI-2 through GT-7 which is controlled from GT-3. After being complemented, the corrections are added to Trunk B' before going out to be added to the original product.

Shifting the usable portion of the product in the number register is accomplished through selecting the timing of the pulse which performs the rounding off, the choice being made in a Switch ES. This pulse, selected in time relation to the answer from the column of delays in the Discriminators is put on Trunk B' to be added in the last partial summing, and is also sent out to open the gate which will start the number register from the last adder.

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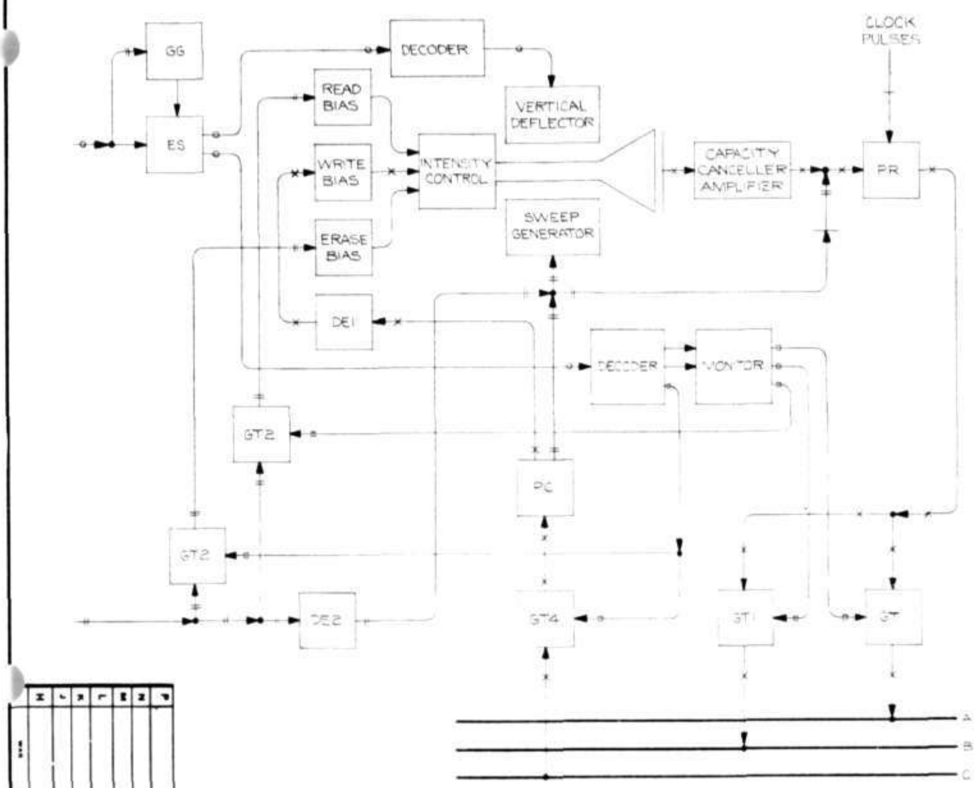
TOLERANCES NOT OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64



STORAGE TUBE (ST)

A Storage tube is composed of the electrostatic cathode ray tube upon which the pulses forming numbers are stored and the associated circuitry required to perform all the necessary functions when used as a part of a complete computer system

The storage tube is assumed to contain 32 storage spaces each capable of holding one number, or word, and as used in a system it must be able to produce one of these numbers on either of the trunks A or B or it must be able to store a number coming in on trunk C. To control these actions an order must consist of two parts, one being a code number designating the line of the tube desired and the other controlling the condition of the tube and determining which line it is to be connected to. The order is shown here as being separated into its two parts by the switch ES with each part being interpreted by its own decoder, but it would be equally possible to have a single decoder which would provide the two separate controlling functions from one order.

If the order is one for reading, a Gate Tube GT-1 will be turned on connecting the tube to one of the Trunks A or B and GT-2 will likewise be turned on admitting a trigger to stimulate the proper bias voltage for reading. After a slight delay in DE-2 the same trigger starts the sweep to produce the number and is itself sent onto the line just after the Capacity Canceller Amplifier to serve as an Intelligence Pulse.

If the order is to prepare the tube to receive a number on Trunk C the Gate Tube GT-3 is opened allowig the trigger to erase the proper line before the number to be stored arrives. When the number comes on Trunk C its Intelligence Pulse is removed by the Pulse Cut-off PC and is used to start the sweep, while the rest of the number is fed to the intensity control circuit.

The arrangement shown is but one of many possibilities, and no significance should be attached to the particular choice used here. Other methods of providing the necessary internal functions will still permit the same scheme for utilizing the storage tubes in the system and the method of control will be the same as that shown here.

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STORAGE TUBE (ST)

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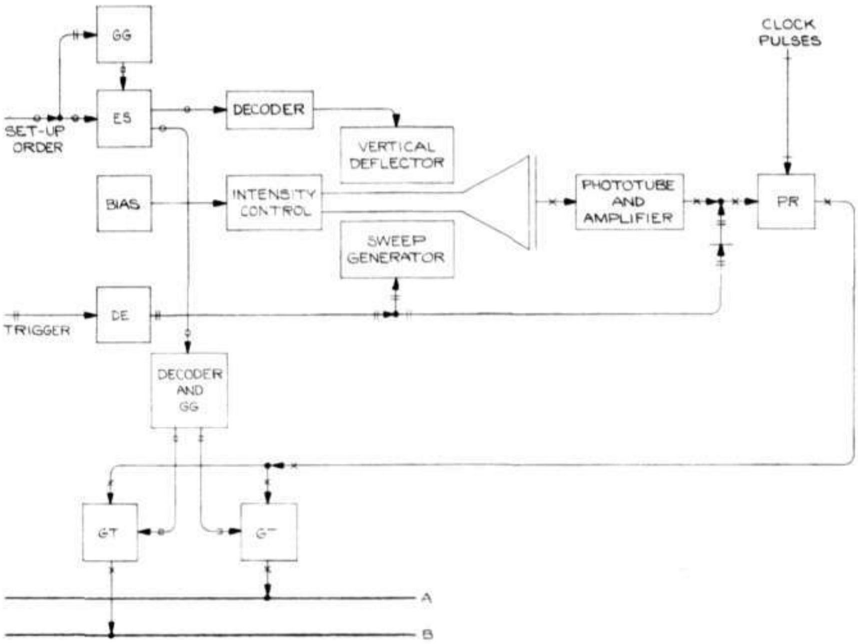

OSCILLOSCOPE READER (OR)

The Oscilloscope Reader is a modification of the Storage Tube to permit reading or scanning data which can be stored in the form of punched cards which are placed in front of the cathode ray screen. Like the storage tube the 'scope reader will hold 32 numbers or words and will be able to produce any one of the 32 on either trunk A or B, though the only method of changing the stored data is to change the card itself.

Like the storage tube the set-up order determines the line to be read and selects the output connection, and then an externally timed trigger starts the sweep to produce the number for which it also serves as the Intelligence Pulse. The delay element DE is necessary to have the outputs of OR's and ST's appear simultaneously.

TOLERANCES NOT OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64

C-37021

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OSCILLOSCOPE READER (OR)

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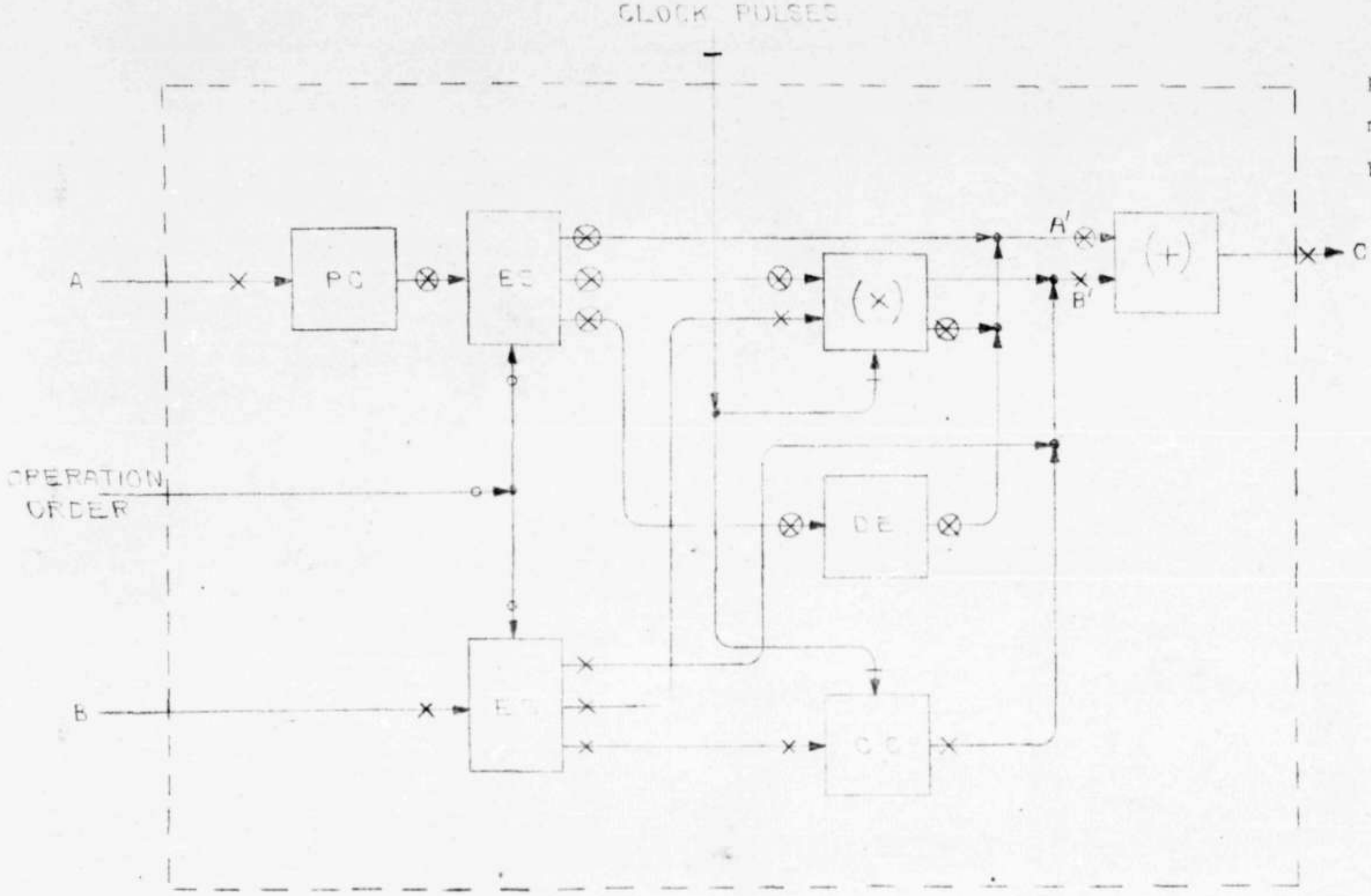
TOLERANCES NOT OTHERWISE SPECIFIED:
DECIMAL ± .005 FRACTIONAL ± 1/64



BASIC COMPUTING ELEMENT

The basic computing element shown will perform the functions of addition, subtraction, and multiplication. The operation desired is selected by the switch order to the Electronic Switch ES. One number supplied retains its Intelligence Pulse which is used in the answer but the other has its extracted in the Pulse Cutoff PC. For an addition both numbers are put directly through the adder. In Subtraction the minuend is complemented in the Complementer CC while the subtrahend is put through a slight compensating delay in DE. The Multiplier(x) is only partial, the last sum of the product being made in the adder.

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BASIC COMPUTING ELEMENT

SCALE: DR. D.L.C. 5-20-46
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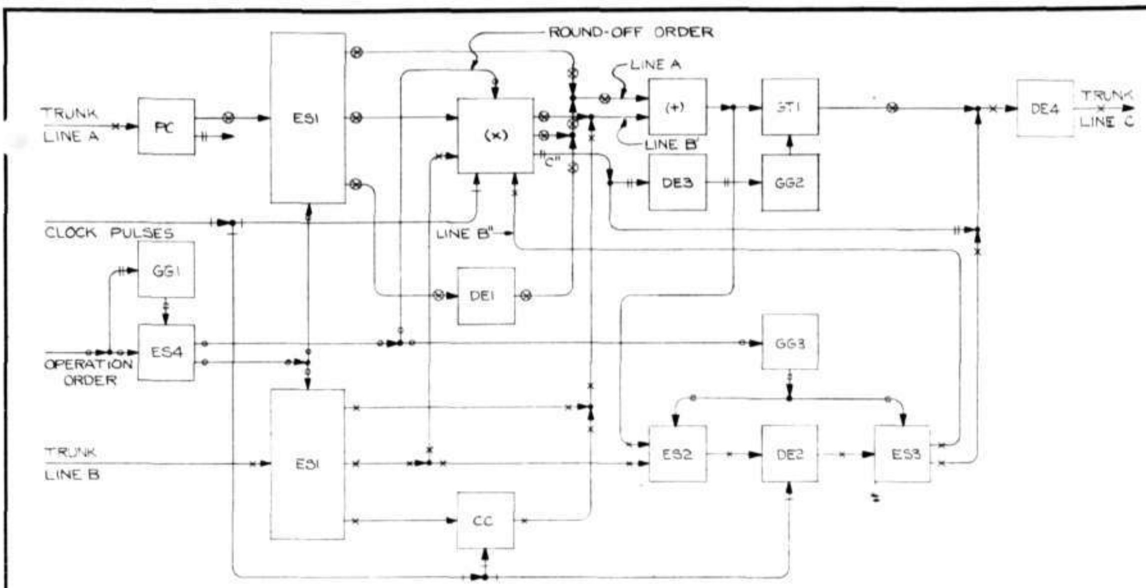

COMPUTING ELEMENT TYPE 1

The complete computing element shown here is suitable for incorporation into a computer system for performance of the functions of addition, subtraction, and multiplication to any desired length. The adder has provision for indicating improper addition of positive or negative numbers. The computing element as shown is intended for use in a system with a synchronized trigger to start each operation, such that the same length of time is available for each operation. In this system the results of additions and subtractions are delayed one word-length in a Delay Element DE-2 thus taking as much time as a multiplication. This time taken in the computing element can be used elsewhere in the system for erasing the storage tube that is to receive the answer.

The operation order to the computing element is split by an Electronic Switch ES-4 into two parts, one part specifying the type of operation desired and the other giving the desired rounding-off position if the operation is a multiplication. The former part sets the two switches ES-1 making the proper connections to adder, multiplier, or through DE-1 and the Complementer CC for subtraction. As normally set, the Gate Tube GT-1 and the switches ES-2 and ES-3 pass an addition or a subtraction through DE-2 before the result comes out on trunk line C. Actually the order need not be split into two parts by ES-4 since extra code digit readers can be provided in the switches ES-1 to interpret the rounding-off order.

For a multiplication the rounding-off order which is sent to the multiplier also appears at GG-3 where it actuates ES-2 and ES-3 to connect the input from trunk line B to the multiplier through DE-2 where it is delayed one word length as required by the multiplier for multiplication of negative numbers. The multiplier has as its outputs the two partial sums which added together will produce the correct product, and a trigger pulse on line C" which is timed by the rounding-off order within the multiplier. This pulse is sent directly to line C to be the Intelligence Pulse of the product and after a slight delay in DE-3 goes also to a Gate Generator GG-2 which opens GT-1 at the proper time for rounding-off in accordance with the rounding-off order. Thus, the first part of the product, which is the least significant is blocked by GT-1 which opens to let the usuable part of the number through to follow the IP out on Trunk C.

DE-4 is an additional delay to make the total delay time through the computing element equal to the system cycling time for all types of operations. In other words, a number starts to come out at C more than one word length after the numbers producing it started in on A and B. This time delay is made to correspond to the requirements of other components of the system, especially the storage elements.

ITEM	MATERIAL - DESCRIPTION	PART NO.	QUAN.

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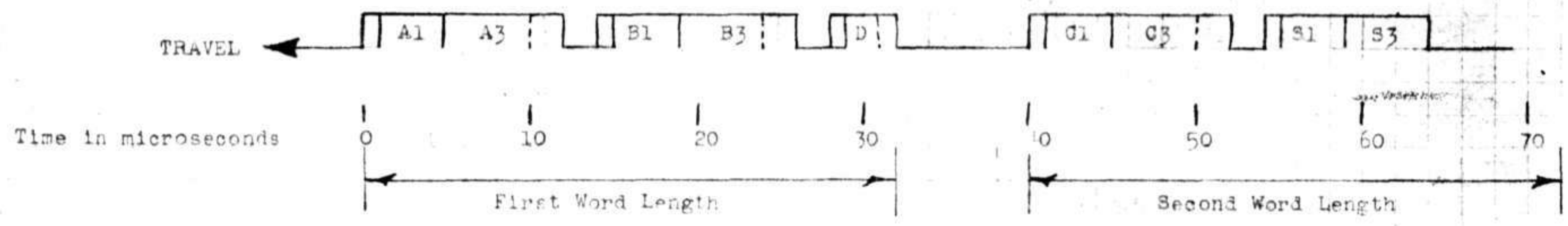
COMPUTING ELEMENT TYPE 1

DR. T. Larry

C-37023

B - 37024-1



DESCRIPTION OF ORDERS

A1 - Order setting the first switch necessary to select the Storage Tube which is to produce a number on Trunk A of the computer system. Composed of 4 digits to connect one out of 16 possible switch positions.

A3 - Order selecting the tube line to be used to produce a number on Trunk A. Composed of 5 digits to set up deflection voltage on one out of 32 possible storage lines, and 2 digits to connect the tube to one of the three trunks in the computer system, A, B, or C. Tubes on Trunks A and B will always read; tube on Trunk C will always erase first and then prepare to write an incoming number.

B1 - Same as A1 but designating the tube on Trunk B.

B3 - Same as A3 but for the tube on Trunk B.

C1 - Same as A1 but selecting the tube on Trunk C.

C3 - Same as A3 but for the tube on Trunk C.

D - Order defining the computer operation to be performed. Composed of 2 digits to select one of four possible arithmetic operations, and 1 digit extra for specifying an alternative rounding-off length, or position if the operation is a multiplication.

S1 - Switching order similar to A1 but for the purpose of selecting a Sub-Program Storage Tube to start a sub-program cycle.

S3 - Similar to A3 but without the 2 digits for specifying the line connection, and for the same purpose as S1, namely to designate the starting point of a sub-program.

NOTE 1 The Intelligence Pulse has been included in all orders where necessary, and is shown at the left-hand or leading edge of each order.

A two-microsecond gap has been left between orders where necessary to permit a timing or resetting tolerance of plus or minus one microsecond.

Orders designated A2, B2, C2, and S2 have been omitted since Type IA has but one stage of switching, but in systems with two stages needed these orders would be included and would be of the same composition and use as their counterparts A1, B1, C1, and S1.

The eight-microsecond gap between word lengths is for the purpose of Storage Tube recycling.

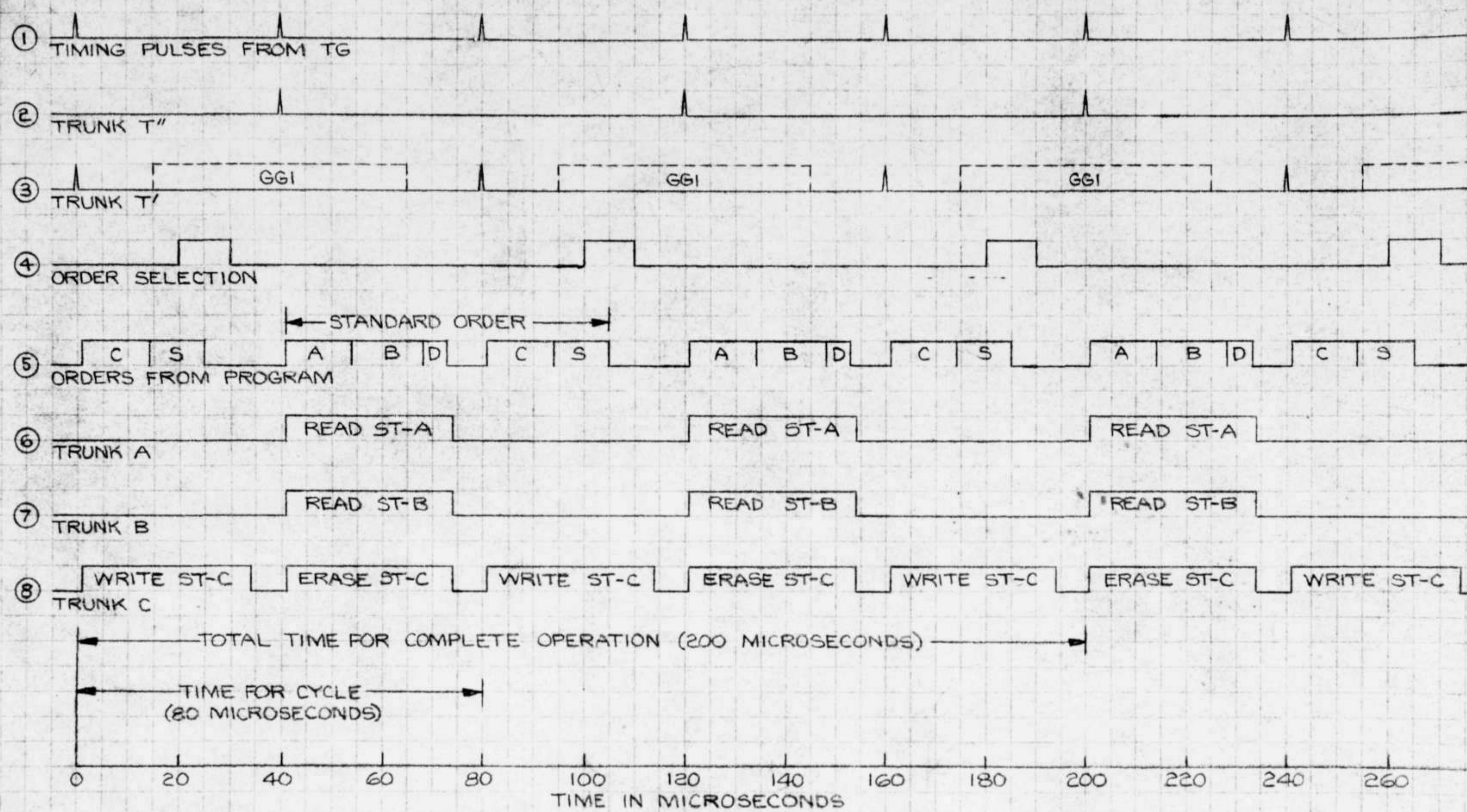
TITLE CHANGED PDT 7/10/46 -1

SERVOMECHANISMS LABORATORY OF THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

COMPOSITION OF STANDARD ORDERS FOR TYPE IA COMPU

SCALE:	DR. Tilton 6/6/46		B- 37024-1
TR. PDT 6/25/46	CK.	APP.	

B-37025-3



NOTE:- Word length is assumed to be 32 microseconds long, and Storage Tube speed such as to permit one sweep every 40 microseconds.

- For detailed composition of Standard Orders see Dwg. B- 37024

- It is assumed that storage tubes will be capable of receiving and interpreting orders while still in the process of executing a previous order.

REVISED PDT 7/30/46 -3
TITLE CHANGED PDT 7/10/46 -2
REVISED PDT 7/5/46 -1

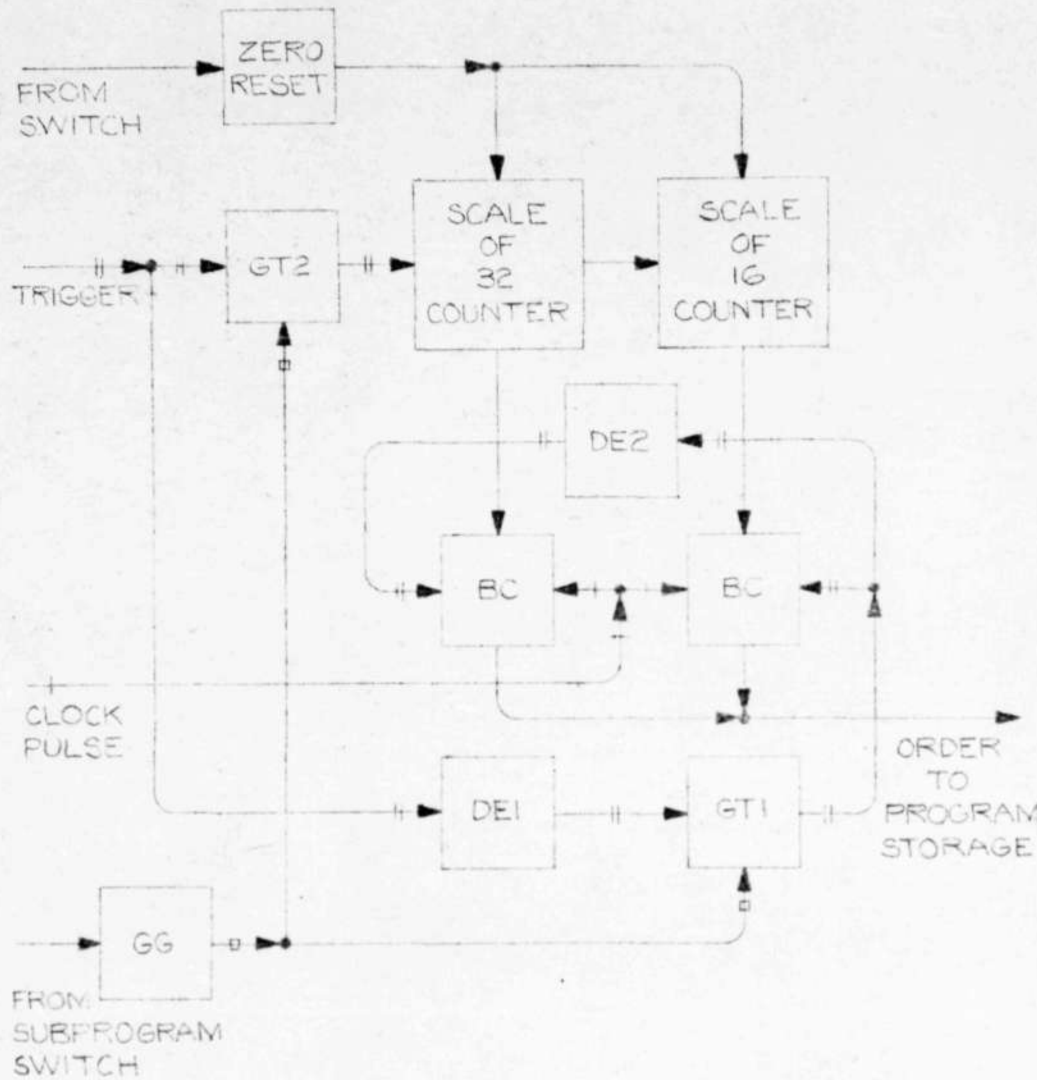
SERVOMECHANISMS LABORATORY OF THE MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

TIME CYCLE FOR COMPUTER SYSTEM TYPE IA

SCALE:	DR. T. Leary Jr. 6/20/46	
TR. PDT 6/28/46	CK.	APP.

B- 37025-3

B-37026	TOLERANCES NOT OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64
WO-	



PROGRAM SELECTOR

The Program Selector is a control unit to determine the sequence in which the program orders are read. As shown, it provides a means of counting serially and will select the orders in numerical order.

The first scale-of-32 counter counts triggers and governs the output of its Binary Coder, BC in accordance with the count. After 32 triggers, it resets to zero and sends a pulse to the scale-of-16 counter which counts these pulses and governs the second BC accordingly. The trigger pulse is delayed to allow for the counting and then triggers the coders successively to send out first the scale-of-16 count which is a switch order to select the program storage tube desired, and then to send out the scale-of-32 count representing the tube line to be read to get the program order. The last program order to be read switches itself out of the rest of the system into the reset unit which resets both counters to zero for a new program cycle.

When a program order contains an order selecting a tube and line of a sub-program cycle this order is separated and is used to start the Gate Generator, GG, which closes the normally open Gate Tubes GT-1 and GT-2. Timing of this subprogram order within the main order insures the blocking of triggers to the program selector while a subprogram is in progress and insures continuity in reading the orders of the main program when the subprogram is completed.

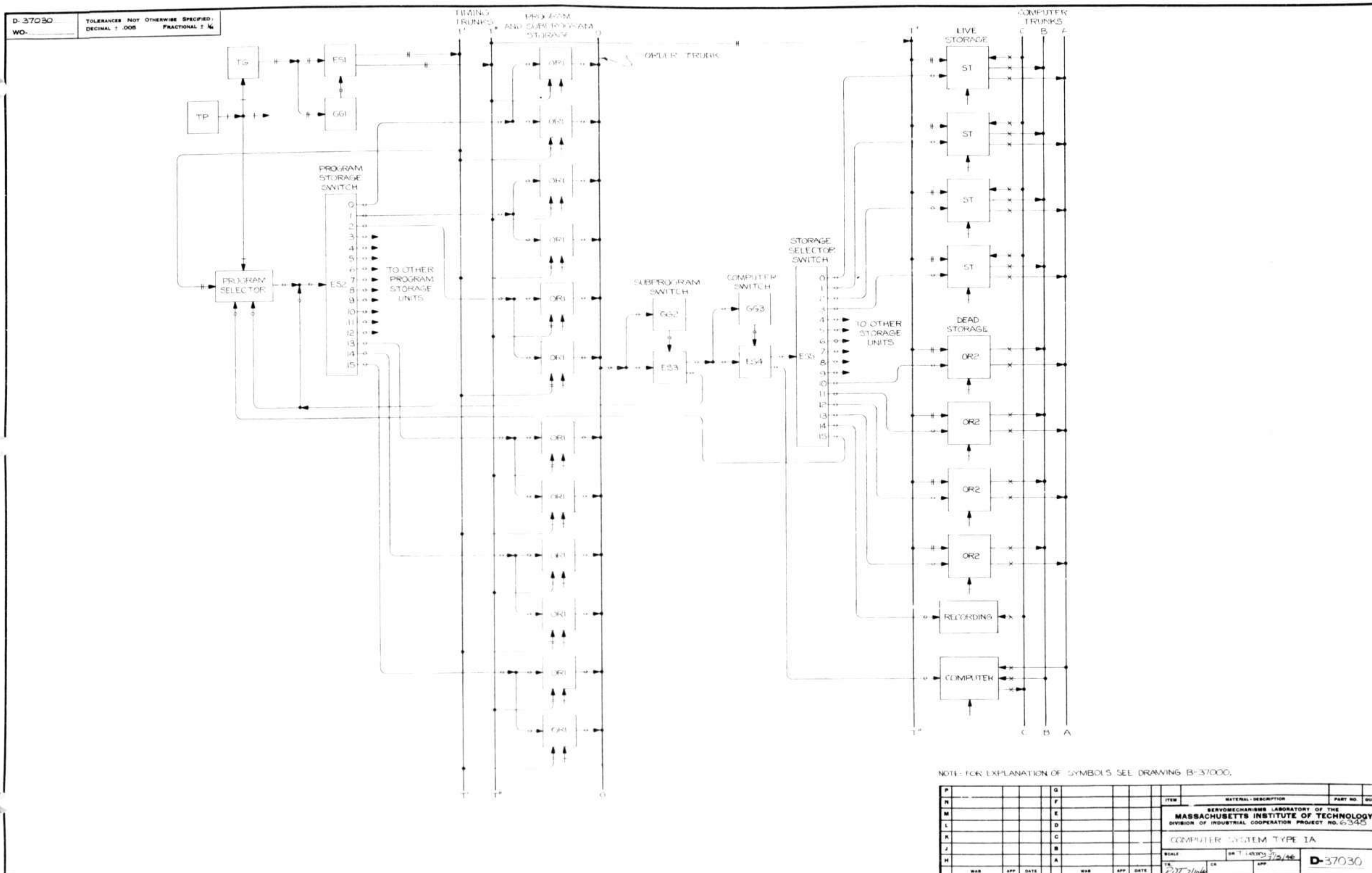
P				G			
N				F			
M				E			
L				D			
K				C			
J				B			
H				A			
	WAS	APP.	DATE		WAS	APP.	DATE

ITEM	MATERIAL - DESCRIPTION	PART NO.	QUA

SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345

PROGRAM SELECTOR TYPE I

SCALE	DR T. Leary Jr. 6/19/46		B- 37026
TR. PDT 6/27/46	CK.	APP.	


D-37030
WO-
TOLERANCES NOT OTHERWISE SPECIFIED: DECIMAL ± .005 FRACTIONAL ± 1/64
TIMING TRUNKS
T' T''
PROGRAM AND SUBPROGRAM STORAGE
O
ORDER TRUNKS
TG
ES1
TP
GG1
PROGRAM STORAGE SWITCH
PROGRAM SELECTOR
ES2
TO OTHER PROGRAM STORAGE UNITS
OR1
SUBPROGRAM SWITCH
GG2
ES3
COMPUTER SWITCH
GG3
ES4
STORAGE SELECTOR SWITCH
ES5
TO OTHER STORAGE UNITS
LIVE STORAGE
ST
DEAD STORAGE
OR2
RECORDING
COMPUTER
COMPUTER TRUNKS
C B A
NOTE: FOR EXPLANATION OF SYMBOLS SEE DRAWING B-37000.
ITEM
MATERIAL - DESCRIPTION
PART NO.
QUAN.
SERVOMECHANISMS LABORATORY OF THE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345
COMPUTER SYSTEM TYPE IA
SCALE
DR
TR
CK
APP
WAS
DATE
D-37030