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SUBJECT: XD-1 EVALUATION, 13 JULY 1955

To: N. H. Taylor

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Date: 12 SEPTEMBER 1955

Approved: J. A. O'Brien

Abstract: The second evaluation of the CD addressable drums was performed on 13 July 1955. Drum operation has improved since the last evaluation on 20 May 1955, but noise problems existing in the drum system caused a prohibitive number of drum parity alarms and error halts during the evaluation test run.

Records indicate that the reliability of the central computer has increased rapidly during the past two months. The computer was operable about 95% of the assigned time and the time between failures was 8.4 hours during the period of 2 - 16 July 1955.

Margins on the central computer circuits and drum circuits are adequate except for cFF's used in counting applications.

A device to sense transients and drift on power supply lines is needed on XD-1. This device is being designed for installation in XD-1.

The main difficulties noted during the evaluation were noise problems in the drum system and lost time resulting from difficulties in the power supplies and power supply distribution system.

The research reported in this document was supported jointly by the Department of the Army, the Department of the Navy, and the Department of the Air Force under Air Force Contract No. AF 19(122)-458.

I. Physical and Logical Status of XD-1

The drum entry section of the manual input frame has been connected to the drum system since the last XD-1 evaluation was made. This section contains the manual input card machines and is through system tests. The core input section of the manual input frame is still undergoing system tests.

The OD sides of the MI and DD drums are through system tests, as are the CD sides of all drum fields. This evaluation covered just the CD side of the addressable fields and the card machine inputs to the manual input system.

Program RCC 03 was run during this evaluation. This program tests certain sections of the central computer that we have not been able to test before.

Core Memory II has been fixed so that it will work when RMM 204 (worst pattern) is run.

The "master reset" button no longer causes the card reader to feed one card when the card reader is "ready".

The "air" and "temperature" alarms are still not connected to XD-1. Some of the alarm and power supply indicator lights that are connected are so dim that they cannot be seen.

Except for these changes, XD-1 has not changed since the last evaluation (see 6M-3669).

II. Reliability

In order to determine the reliability of the central computer portion of XD-1, a study of log book entries has been made and an evaluation test run lasting six hours was performed.

1. Log Book Data

A summary of the log book data which was placed on IBM punched cards for the period of 2-16 July 1955 is as follows:

Assigned time - 252.93 hrs.
Lost time - 10.1 hrs.
Failure or alarms - 29

Percentage of useful assigned time: $100 \times \frac{(242.83)}{(252.93)} = 96\%$

Mean good-time between failures: $\frac{242.83 \text{ hrs.}}{29 \text{ failures}} = 8.4 \text{ hrs.}$

A comparison of reliability figures for the four evaluation tests performed on XD-1 is as follows:

Percentage of Usable Assigned Time

1 March 1955 - 73.5%
18 March 1955 - 91.5%
20 May 1955 - 90.4%
13 July 1955 - 96.0%

Mean Good-Time Between Failures

1 March 1955 - 4.72 hrs.
18 March 1955 - 3.8 hrs.
20 May 1955 - 4.2 hrs.
13 July 1955 - 8.4 hrs.

A decrease in core memory parity alarms, card machine failures and component failures (1% precision resistors) was responsible for the increased reliability. Table I shows the division of lost time for various failure categories.

TABLE I

Lost Time Failures, 2-16 July 1955

Failure Category	Number of Incidents	Time Lost (hours)	Percentage of Total Lost Time (%)
Mechanical failures (motors, clutches, relays, etc.)	2	2.75	27.5
Broken wires, connections, card assemblies, etc.	4	2.00	20.0
Unexplained alarms (except parity alarms)	4	1.76	17.6
Circuit components (other than tubes)	5	1.25	12.5
Unexplained core memory parity alarms	6	1.09	10.9
Tubes	1	.84	8.4
Other	4	.32	3.1

Data on the reliability of the drum system was not included in this report because many unexplained failures occurred on the drums and many changes were made on the drum system so that records of performance were not useful. For these reasons, a special log to be used with the new log system has not been issued to the drum section at the present time. According to IBM engineers, noise is being introduced on the low level signal lines. This interference between drum fields was the cause for drum parity alarms and halt errors during the evaluation test.

Power supplies, power control distribution, marginal control distribution, motor generator switchgear, and a.c. switchgear caused 9 interruptions and 14.35 hours of lost system time which was not included in the computation of central computer reliability. Improvements in these areas are being investigated by the MIT power group.

2. Evaluation Test Run - 13 July 1955

An evaluation test lasting eight hours was conducted on the equipment scheduled for test on 13 July 1955. Results of this test are presented in Table II.

TABLE II

Evaluation Test, 13 July 1955

Program:	RDR 09 (checking all CD addressable fields except the radar data fields)
Useful Time:	1 hr. 10 min.
Lost Time:	30 min.
Eight Failures:	Fields 05, 21, 26, 27, and 41 gave drum parity alarms and fields 05 and 42 had failures which were detected by an arithmetic check.
Program:	DDR 01 (checking all nine radar data fields using manual mode)
Useful Time:	20 min.
Lost Time:	15 min.
Three Failures:	Three error halts were attributed to a failure in bit L5, field 70.
Program:	DDR 01 (sequencing through all CD addressable fields)
Useful Time:	31 min.
Lost Time:	1 min.
One Failure:	One error halt attributed to a failure in bit 15, field 70.

Program: RDR 30 (checking drum field switching)
Useful Time: 20 min.
Lost Time: None
Failures: None

Program: SY 001 (checking central computer functions)
Useful Time: 1 hr. 28 min.
Lost Time: 11 min.
Five Failures:
1. A core memory parity alarm occurred.
2. An unexplained alteration of the state of the disconnect flip-flop was noted.
3. Punched cards failed to check correctly on three occasions because of incorrect punching.

Program: RCC 03 (checking manual operations)
Useful Time: 58 min.
Lost Time: 11 min.
Four Failures:
1. The continue button failed to operate correctly on two occasions. It seemed that the release time of the continue button was somewhat critical.
2. One failure during read-in was noted.
3. The printer failed to print "0" in three positions of one line.

Program: RCM 03 (checking card punch)
Useful Time: 30 min.
Lost Time: None
One Failure: A core memory parity occurred as a result of accidental drum power switching.

Program: DMI 10 (checking manual input card machines)
Total Time: 35 min.
(all useful)

Program: DMI 08 (checking manual input interlocks)
Total Time: 12 min.
(all useful)

Percentage of Usable Assigned Time: $100 \times \frac{(7.2 \text{ hrs.} - 1.13 \text{ hrs})}{7.2 \text{ hrs.}} = 84.5\%$

Mean Good-Time Between Failures: $\frac{6.07 \text{ hrs.}}{22 \text{ failures}} = .28 \text{ hrs.}$

3. Group 61 (MIT) Operation of XD-1

Programmers from Group 61 (MIT) used the central computer and AM drums for six hours and thirty-nine minutes during the two week period ending 13 July 1955. A summary of computer operation during this time is included in Table III.

TABLE III

MIT's Assigned Time on XD-1

Lost Time Attributed to:	No. of Failures	Time Lost
Core memory parities (unexplained)	2	10 min.
Printer	2	
a. Per 73 failed		none
b. Spurious X's and W's were printed		none
Interference from drums (power switching and drum disconnect line).	2	2 min.
	6	12 min.

Percentage of usable assigned time: $100 \times \frac{(6.45 \text{ hrs.} - 2 \text{ hrs.})}{6.4 \text{ hrs.}} = 97\%$

Mean good-time between failures: $\frac{6.25 \text{ hrs.}}{6 \text{ failures}} = 1.04 \text{ hrs.}$

III. Margins and Margin History

For the two week period ending 13 July 1955 margins were taken on the central computer, magnetic drums (all CD addressable fields), and the drum entry portion of manual inputs. A list of the programs used and the means employed to take margins (manual or automatic) are as follows:

Program Used	Equipment Group	Mode of Checking
RCC 03	MC-3(Program & Control Elements)	Manual
RAE 01	MC-2 (Arithmetic Element)	Automatic
RMM 204	MC-1 (Core Memories I & II)	Automatic
DDR 01 & RDR 09	MC-5 (Addressable Drum Fields)	Manual
DMI 06	MC-6 (Manual Inputs -- Card Readers I & II)	Manual

Margins taken by the automatic or computer control are taken to prescribed limits on a weekly basis; margins to failure are taken each month.

Program RAE 01 was modified to decrease the time required for each pass. Failure points found by automatic means agreed with values found during manual test.

Some difficulties were encountered when RMM 204 was used for marginal checking purposes in either the automatic mode or the manual mode. The margins on core memory were dependent on the speed with which the margin was applied. This condition is not as severe since the core memories received major improvements during the months of June and July. Margins taken by both automatic and manual means were in agreement.

A review of margin check data has shown that the following circuits failed to meet the arbitrary ± 20% variation of supply voltage:

Line	Circuit	Margins +	Margins −	Description
5 -150 volts A-1	bFF	16	23	CD Read-Write Control
5 -150 volts A-4	bFF	21	23	CD Information
5 -300 volts D-4	cFF	20	38	APC Register
6 -300 volts A-2	cFF	41	39	MI Area Discriminator
2 -300 volts A-1	cFF	17	52	Real-Time Clock Freq. Div.

It seems that the cFF's in the APC and the real-time clock frequency divider have low margins both from the standpoint of absolute value and percentage of supply voltage variation (only 6.66%); these margins should be improved. The bFF's in the CD read-write control and CD information registers have low margins. These margins, however, seem reasonable for bFF's. Margins on the MI area discriminator cFF's are below the ± 20% criteria, but they are not too low.

Margins on the gate tubes in the adder circuits, parity circuits, and the accumulator have maintained margins of about + 25 volts and -20 volts. These margins have remained about the same since the first XD-1 evaluation.

Sense amplifier margins for core memory I have improved and they are now ±40 and -40 volts as compared to ±34 and -19 volts on 1 June 1955. Margins on the same circuits for core memory II have improved from ±21 and -23 volts to ±45 and -25 volts. Program RMM 204 was used for taking these margins.

An effort is being made to determine the margins of some individual lines at the logic level instead of taking margins on many logic groups which were expected to have very similar margins.

IV. Shock Tests

Tubes and plug-in units on the drum frames and manual input frame were tested for shock and vibration. During shock tests on the drum, the only failure occurred when a 5965 tube failed during tube tapping. This failure was complete enough to warrant a plug-in unit replacement. A list of the number of plug-in units and tubes involved in this test is as follows:

Plug-in units: 91

Tubes: 5965's - 263
5998's - 41
2120's - 157

A power-off, power-on sequence was performed. All AC and DC power was shut down after RAE 01 had been stored in core memory I and a pattern of "1's" and "0's" written on fields 02, 10, 20 and 41. After the power had been off for five minutes, an attempt to turn the power on failed. A 5% sensitrol indicated that something had not cycled on correctly during the power-on sequence. This sensitrol was reset and power was turned on with no other failures noted during the power-on phase.

After all computer power had been restored, an attempt to run RAE 01 without reloading showed that the parity bit in address zero had changed. This was the only error attributed to core memory due to power shut-down. Program RAE 01 ran correctly except for this fault.

A check of information stored on the drums showed that bit L4 of all fields was in error. These errors occurred in blocks of consecutive addresses on the drums. Bit L4 had given trouble before and it seemed to be a fault in a digit position instead of a deficiency in the systems ability to retain information.

Diode can assemblies on the magnetic drums were not included in the shock tests. This omission was requested by IBM because they felt that these assemblies need an improvement in mechanical design.

The 10% sensitrols on the XD-1 power supplies are not adequate for indication of power supply drift because some circuits fail with less than a 10% change in power supply voltage. Also, the response of sensitrols is not sufficient to indicate line transients. A device desinged to furnish adequate monitoring is being designed for future use.

Sometimes the card punch feeds cards and the printer feeds paper when computer power is turned on. Additional circuitry can be added to remedy this situation which is not a card machine failure.

V. Conclusions

The reliability of the central computer has improved considerable since the evaluation on 2 May 1955. About 95% of the assigned time was useful and failures occurred on the average of about every 8.4 hours. No excessive component failures in the central computer area were noted and margins seemed to be adequate except for cFF's used in counting applications, both in the drums and in the central computer.

All of the drum programs ran successfully but they could not run for any extended period because of error halts and drum parity alarms. These failures indicated that switching interference caused by switching on the output buffer drum fields is prohibitive and must be corrected before the system will operate reliably.

The drum was able to retain information during a power-off, power-on sequence on all bits except L4.

The card entry portion of the manual inputs operated without failure during the evaluation test.

Diode cans in the drum frames require additional support to insure mechanical stability.

A device to monitor the supply voltages for variations less than $\pm$ 10% of the supply voltages is needed and has been ordered for XD-1.

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