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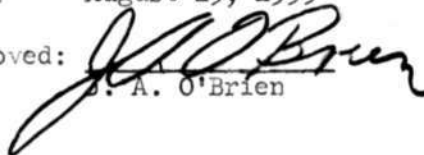Lexington 73, Massachusetts

SUBJECT: RESULTS OF THE SYSTEM TEST PERFORMED ON THE AN/FSQ-7 (XD-1) DURING JUNE 1955

To: N. H. Taylor

From: J. D. Crane

Date: August 25, 1955

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Abstract: A system test was performed on the central computer portion of the AN/FSQ-7 (XD-1) during the month of June. Four demonstration runs and a study of computer reliability showed that the central computer operated correctly about 90 to 95% of the assigned time with interruptions every one-half to three hours depending on the mode of computer operation.

Precision resistors were the only components which had excessive failure rates; extensive work is being done to correct this situation.

Some weaknesses in core memory circuits were corrected during the month of June; circuit margins were improved and increased reliability is expected.

The card machine did not appear to be as reliable as the electronic equipment.

Voltage margins are adequate; only one specific case requires improvement.

A few minor mechanical deficiencies (labels, markings, covers, etc.) were noted.

Performance of the central computer was satisfactory except for difficulties with core memory, card machines, and precision resistors.

1.0 Introduction

The first in a series of acceptance tests to be performed on the AN/FSQ-7 (XD-1) was conducted during the month of June 1955. This test consisted of four demonstration runs and a survey of central computer performance during June.

1.1 Demonstration Runs

Each of the four demonstration runs lasted about four hours; Air Force and MIT representatives attended all but one of these demonstrations. All computer operation was controlled by IBM engineers.

1.2 Performance Records During June 1955

Records of computer performance and margins were compiled for the month of June. Basic data required for this analysis was taken from log book entries and margin check reports issued by IBM. Log entries were placed on punched cards and data for the summaries were prepared by the IBM record section.

2.0 Equipment and Logical Functions Submitted for Acceptance

A list of equipment and instructions submitted for test has been compiled by Mr. H. L. Kurkjian of IBM and was included in a test proposal "System Test Plans for the Central Computer System", 10 May 1955, by Mr. Kurkjian. The test proposal discusses the system test program in detail. There are no exceptions to this proposal as it appears in its final form, so the results of the acceptance tests are based on only the equipment and instructions included in the proposal.

The following list of equipment is presented in this report to furnish the reader with an over-all view of the equipment being tested.

1. Left Arithmetic Frame
2. Right Arithmetic Frame
3. Instruction Control Frame
4. Selection Control Frame (with some exceptions)
5. Program Frame (with some exceptions)
6. Left memory Frames
7. Array Frames
8. Right Memory Frames
9. Maintenance Console
10. IBM 711 Card Reader (modified)
11. IBM 716 Line Printer (modified)
12. IBM 721 Card Punch (modified)
13. IBM 010 Card Punch

3.0 Results of Acceptance Test Demonstrations

Demonstration runs were performed on 9 June, 16 June, 22 June and 30 June 1955. A special effort was made to provide accurate records during these tests while equipment was being used under controlled conditions.

3.1 Logical Completeness

The computer was able to perform all of the specified logical functions. All of the required programs ran successfully.

3.2 Physical Completeness

All of the specified equipment was delivered and installed. It was noted, however, that some minor mechanical deficiencies or inadequacies existed (see Table I).

3.3 Reliability During Demonstrations Runs

A summary of the reliability during the four test runs is as follows:

Total Time	14.84 hours
Total Lost Time	1.34 hours
Number of Failures	43

$$\text{Percentage of Usable Assigned Time:} \quad 100 \times \left(\frac{14.84 \text{ hrs.}-1.34 \text{ hrs.}}{14.84 \text{ hrs.}}\right)=91\%$$

$$\text{Mean Good-Time Between Failures:} \quad \frac{13.5 \text{ hrs.}}{42 \text{ failures}} = .32 \text{ hrs.}$$

Time during which the computer was not operating satisfactorily was considered to be lost time. Printing or punching errors were discovered which did not cause lost computer time, but each occurrence was considered to be a failure. Repetitive failures were treated as individual failures for the computation of the mean good-time between failures. A list of the failures incurred is included in this report (see Table II).

About 40% of the failures were encountered in the printer and punch; 16% of the failures were core memory parity errors. Both core memories were being checked and modified during the month of June and the number of core memory parities decreased during this month. No parities were experienced in the 30 June 1955 demonstration.

A bad plug-in unit found during the fourth demonstration on 30 June caused 23% of the interrupting failures noted during demonstration runs.

4.0 XD-1 Performance During June 1955

The XD-1 logbook entries were kept by IBM engineers for the period including 13 June 1955 through 2 July 1955. These records were used as the source material for preparing this study of computer performance.

Reliability figures were recorded in such a manner as to indicate the performance of the equipment included in the system test and ignore the effects caused by installation of other equipment and failures in outside areas.

4.1 Equipment Included in Records

Only the failures which occurred in the equipment under test (see Section 2.0) were considered in the reliability calculations.

4.2 Limitations of the Record System

The most important factors influencing the accuracy of the computer reliability studies were completeness of log entries and the fact that much installation and testing was in process during the time the central computer was being observed.

4.2.1 Completeness of Log Entries

Records for 1 June through 13 June were not included in this summary because entries were not complete and accurate. After 13 June 1955, the records were much improved from the standpoint of completeness and accuracy. The most serious fault in the record system occurred when unexplained failures were explained and no complete method of correlating these facts was included in reports.

4.2.2 System Assignments During The System Test Period

A record of the percentage of time devoted to the various system assignments and reliability during each assignment is as follows:

Assignment	Percentage of Total System Time (%)	Percentage of Usable Assigned Time (%)	Mean Good-Time Between Failure (hrs)
Routine Maintenance & Mach. Improvement	31.10	85	3.0
Drum System Test	22.50	96	8.6
Tape System Test	19.80	99	17.7
Memory Evaluation	8.00	91	1.7
Marginal Checking	5.90	94	5.0
MIT (Group 61)	4.25	95	2.8
Manual Inputs System Test	3.70	98	6.6
System Tests	3.23	92	.3
Program Checking & Analysis	1.00	99	1.8
Others	.52	62	.6

During MIT (Group 61) operation and system tests the
records of performance are most easily interpreted; however,
these assignments consumed only 7.48% of the 361.35 hours
considered for this test. About 73% of the time was spent
on the first three assignment categories listed above.

4.3 Results of the Reliability Study

Results of this reliability study are expressed in terms of
the percentage of usable assigned time and the mean good-time be-
tween failures.

4.3.1 Percentage of Usable Assigned Time

The percentage of usable assigned time is indicative of the ability of the computer to perform satisfactorily the assignments listed in section 4.2.2. For the period of this test, the percentage of usable assigned time was found to be as follows:

Useful Assigned Time: 335.1 hrs.
Lost Assigned Time: 27.7 hrs.
Total Assigned Time: 362.8 hrs.

Percentage of Usable Assigned Time:

$$100 \times \frac{362.8 \text{ hrs.} - 27.7 \text{ hrs.}}{362.8 \text{ hrs.}} = 92.5\%$$

About 50% of the lost time was attributed to component failures (excluding tubes) and core memory parity alarms.

4.3.2 Mean Good-Time Between Failures

During the period considered in this test, 104 interrupting failures occurred. The mean good-time between failures was found to be:

Useful Assigned Time: 335.1 hrs.
Interrupting Failures: 104   failures

$$\frac{335.1 \text{ hrs.}}{104 \text{ failures}} = 3.1 \text{ hours between failures}$$

5.0 Distribution of Failures in XD-1

Failures were divided into two categories for presentation in this report -- explained failures and unexplained failures.

5.1 Explained Failures

A tabulation of explained failures is included in Table III. From this table, it is evident that tube failures, circuit component failures, and failures resulting from inability to maintain an adjustment are the major causes for interruption.

A description of the tubes whose failures were attributed to normal use is as follows:

Number of Tubes	Type of Tube	Fault (as indicated by technicians in plug-in unit repair)
1	2420	internal short
1	2420	cracked envelope
1	5727	low output
1	Z-2177	low output
3	5965	low output
2	2D21	unknown

A description of other component failures attributed to normal use are as follows:

Number of Components	Component Description
4	300K - ohm 1% resistors
9	510K - ohm 1% resistors
1	36K - ohm 1% resistor
2	neons (Flip-Flop indicators)
1	Type W diode
1	3:1 pulse transformer

All failures which resulted from failure to maintain adjustment occurred in the printer with the exception of one failure in core memory circuits.

5.2 Unexplained Failures

During the period under study, fifty-seven unexplained incidents occurred (see Table IV). Forty-four percent of the failures were core memory parity alarms. A few of the core memory parities were attributed to component failures in parity count circuits.

Complete information regarding subsequent repairs and adjustments which offered explanations for some of the unexplained failures was not available.

5.3 Failures Which Caused Lost Time

A tabulation of lost-time failures and the amount of time lost for each type of failure is presented in Table V.

6.0 Margins and Margin History

Margins on most of the circuits submitted for test were greater than $\pm$ 20 percent of the supply voltage or within the bounds determined by safety limits.

6.1 Margins Which Were Less Than $\pm$ 20 Percent of Supply Voltages

Circuits which did not meet the arbitrary $\pm$ 20 percent criteria were as follows:

1. The voltage margins of the c-FF's in the real-time clock frequency dividers are $+$ 17 volts and -52 volts on the -300 volt line. The positive margin is too low to be satisfactory.

2. The -300 volt line for the Memory Gate Generators in core memories I and II permits -20 volt excursions before failure. This is only 6.6% of the supply voltage, but this is considered to be satisfactory for the present status of memory.

6.2 Margins on Adder Gates and Parity Count Gates

During previous evaluations performed by MIT, margins which seemed low or caused reason for concern were noted. Series of gate tubes in the parity circuits and the adder circuits were watched closely because margins were $+$ 25 and -18 volts. These margins were $+$ 25 and -20 volts at the time of this system test. Results of efforts to improve these margins indicate that this is the maximum margin to be expected with the present circuits; nevertheless, a series of tests will be performed by IBM engineers to determine the effect of aging tubes in the adder and parity circuits.

7.0 Summary

Except for difficulties with card equipment and core memory, the central computer performed as well or better than we at Lincoln had expected at this stage of development. Indications are that we might expect the performance to be brought up to the high level that we are all aiming for after the system is finally assembled and allowed to operate without being subjected to frequent modifications.

7.1 Central Computer Reliability (Including all Equipment Under Test)

The actual reliability figures deduced from the test data are that the central computer can be depended upon to operate correctly about 90 - 95% of the time and that errors may be expected to occur about once every half hour to every three hours of operation depending upon the mode of operation. As the figures stand, they indicate extremely poor operation, especially when one considers that the lost time figures are made up for the most part by the time it took the program to start again. They do not consider the effect of an error on accumulated data in a long process as might happen in a real operation. It should be pointed out, however, that in almost all cases, where the computer would run through a program successfully, it would continue to do so for hours if people kept their "hands off". The error frequency should drop off very fast as the overall installation becomes more stable.

The details of this evaluation report point out deficiencies in record keeping. Actually record keeping has improved tremendously and is continuing to do so as men become more familiar with the system and the value of records. New improvements now incorporated in the data recording and processing schemes will increase the efficiency and accuracy of the record system. These records should be an aid in securing better performance.

7.1.1 Card Machines

The card machines and printer performed relatively poorly, but the tests they were given were more strenuous than the normal expected operating conditions. Indications are, however, that the mechanical equipment cannot be expected to equal the electronic equipment in performance. Considerable improvement has been made in the performance of these machines, but it is impossible to say at present whether or not all adjustments are stable or if some of the modifications to correct one trouble have introduced an unsuspected one.

The conclusions of a study of the card machine difficulties are that they are operating slightly less reliably than might be expected at present, but that their performance depends to a great extent upon the operators and maintenance men, and the combination should improve with time and experience. We should not expect to reduce the card machine errors to a relatively negligible amount and should plan our operations accordingly.

7.1.2 Core Memories I and II

During the month of June, corrective action was taken on design weaknesses noted in circuits used in core memories I and II. These modifications included circuit changes to the Sense Amplifier, Memory Clock, Memory Gate Generators, Core Memory Drivers, and Memory Address Register Cathode Followers.

The amount of system improvement resulting from circuit modifications has not been evaluated because the circuit changes have been installed so recently; however, memory margins have improved and an increase in reliability is expected from core memories.

7.1.3 Voltage Margins

With a few exceptions, the voltage margins are very good and appear to be stable. Margins on the cFF's in the real-time clock frequency divider need to be improved.

7.1.4 Components

The principle component failures are the 1% resistors and a very intensive program is underway to correct the situation. The other components including tubes and crystal diodes have been giving very little trouble.

7.1.5 Physical Deficiencies

This report also points out a few physical deficiencies in the equipment (cover labels, etc.) which should be corrected before final acceptance.

TABLE I

Minor Mechanical Deficiencies and Omissions Noted on XD-1

A. Ducts and Covers Not Installed

    1. Covers extending from the top of the modules to the expanded metal ceilings.

    2. Final air conditioning ducts and associated AC outlet fixtures.

    3. Z module end covers.

B. Markings Not Complete on All Frames and/or Plug-In Units

    1. Tube designations (some plug-in units and also memory driver panels).

    2. Circuit breaker labels on Z modules, front and back.

    3. Frame and module designations on modules -- including the memory stalls.

C. Miscellaneous

    1. Lamps indicating power on-off condition are difficult to replace.

    2. Many air flow indicator and power indicators are burned out (see 1, above).

    3. Air leaks are present in module framework.

    4. "Emergency Off" button is extremely sensitive.

    5. Temporary relays are used in d.c. power lines for core memory.

    6. Cyclic Program Control switches are difficult to turn.

TABLE II

Time Lost and Failures Noted During Test Activity Demonstrations

First Demonstration, 9 June 1955

Failure	No. of Occurences	Time Lost
Printer or Punch:		
1. Print "O" instead of "2"	2	--
2. Type wheel 15 in error	1	--
3. PER 73 failed (Card Punch)	1	3 min.
Core Memory Parity Errors:		
1. Unexplained (transients resulting from switching power was the suspected cause).	1	4 min.
2. Unexplained error (the word in memory had the correct parity).	1	1 min.
Miscellaneous:		
1. Failure to load program from card reader (unexplained).	1	3 min.
	7 failures	11 min.

Percentage of Usable Assigned Time $100 \times \dfrac{(3.64 \text{ hrs.}-.18 \text{ hrs.})}{3.64 \text{ hrs.}} = 95\%$

Mean Good-Time Between Failures $\dfrac{3.46 \text{ hrs.}}{7 \text{ failures}} = .49 \text{ hrs.}$

Second Demonstration, 22 June 1955

Failure	No. of Occurences	Time Lost
Printer or Punch:		
1. Words or portions of words omitted	3	--
2. PER 74 failed (punch)	1	--
3. Printed "¢" instead of "I"	2	--
4. Printed "-" instead of "R"	2	--
Core Memory Parity Errors:		
1. Unexplained errors	2	6 min.
2. Unexplained errors (the words in memory had the correct parity bits).	2	7 min.
Miscellaneous (unexplained):		
1. In-Out Interlock alarm	1	11 min.
2. "Master reset" and "reset flip-flop" buttons failed to operate correctly.	1	2 min.
	14 failures	26 min.

Percentage of Usable Assigned Time $100 \times \dfrac{(3.45 \text{ hrs.}- .43 \text{ hrs.})}{3.45 \text{ hrs.}} = 88\%$

Mean Good-Time Between Failures $\dfrac{3.02}{14} = .22 \text{ hrs.}$

TABLE II (Continued)

Third Demonstration, 16 June 1955

Failure	No. of Occurences	Time Lost
Printer:		
1. Print wheel 15 failed	3	--
2. A "0" printed in place of a "6".	1	--
Core Memory Parity:		
1. Unexplained parity alarm	1	2 min.
Miscellaneous:		
1. CPC operations inoperative (open wire)	1	
2. CPC delay switch inoperative (improper termination of pulse line).	1	21 min.
3. Bad neon on FF used in CPC counter.	1	
4. Master reset caused card reader to feed.	1	1 min.
	9 failures	24 min.

Percentage of Usable Assigned Time $100 \times \dfrac{(4 \text{ hrs.} - .4 \text{ hrs.})}{4 \text{ hrs.}} = 90\%$

Mean Good-Time Between Failures $\dfrac{3.6}{9 \text{ failures}} = .4 \text{ hrs.}$

Fourth Demonstration, 30 June 1955

Failure	No. of Occurences	Time Lost
Printer:		
1. Printed a "T" instead of a comma	1	--
Miscellaneous:		
1. Failure to load from card reader (unexplained at the time of the test, but a bad PU was found which was the cause of the trouble).	10	15 min.
2. Unexplained halt error.	1	5 min.
	12 failures	20 min.

Percentage of usable assigned time $100 \times \dfrac{(3.75 \text{ hrs.} - .33 \text{ hrs.})}{3.75 \text{ hrs.}} = 91\%$

Mean Good-Time Between Failures $\dfrac{3.42 \text{ hrs.}}{12 \text{ failures}} = .29 \text{ hrs.}$

TABLE III

Explained Failures in XD-1, 13 June 1955 through 2 July 1955

Failures Attributed To:

Failure Category	Normal Usage	Installation or Modification	Accidental Damage	Other Component Defects	External Cause or Cause Unknown
Broken connections, wires, plugs, etc.	9		2		2
Tubes	9	1	2		1
Circuit components	20	2		5	
Mechanical failures (gear motor, clutch, etc.).	1				
Out of adjustment	8				2
Miscellaneous	1				
No failure category included in reports	3	1			2

Three plug-in units were replaced during system operation for which there is no explanation regarding the faults found in these units at plug-in unit repair. The time required to replace these units was 2.59 hours.

TABLE IV

Unexplained Failures in XD-1, 13 June 1955 through 2 July 1955

Alarms

25 Core Memory Parity Alarms
 3 Halt Errors
 2 IO Interlock Alarm

Visual and Audible Failure Indications (excluding alarms)

3 Failures noted by a change in audio output.
1 Incident when "Load From Card Reader" failed to operate
     correctly.

Failures Noted in Printer, Punch and Reader

4 Printer
1 Punch
3 Reader

Other Failures

15 Unexplained failures with no initial indication of failure
       available (These failures occurred while the system
       was being used for memory evaluation, routine main-
       tenance and marginal checking).

TABLE V

All Failures or Incidents Which Caused Lost Time,
13 June 1955 through 2 July 1955

Failure or Failure Indication	No. of Occurrences	Time Lost (hours)	% of Total Time Lost (percent)
Circuit component (other than tubes)	6	7.37	26.6
Core memory parity alarms	25	6.69	24.2
Maintenance error (failure to install correct plug-in unit, etc.)	2	2.95	10.7
Plug-in units removed (the fault in the plug-in was not described).	3	2.59	9.3
Broken wires, plugs, etc.	6	2.07	7.5
Tubes	3	1.80	6.5
Unexplained failures (no initial indication of failure given).	15	1.16	4.2
Equipment failed to maintain adequate adjustment	2	1.12	4.0
Explained failures (a description of the part which failed was not available).	4	.99	3.6
Alarms (other than core memory parity alarms).	19	.93	3.4

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