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SUBJECT: JUNCTION-TRANSISTOR MAGNETIC CORE DRIVERS

TO: The Transistor Section - Distribution 2

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ABSTRACT: A transistorized core driver, employing one point-contact and one junction transistor, which can drive the equivalent of about 200 metallic magnetic memory cores in series is discussed in detail. A current output of 12 ma with a rise time of 0.3 μsec can be obtained from this circuit. The note begins with a discussion of the relative merits of point-contact and junction type transistors as core drivers. This is followed by an analysis of the grounded-emitter connection of the junction transistor. Next, the transistorized core driver circuit is presented and discussed in detail, including input and output characteristics, design criteria, and voltage margins. Finally the current and voltage outputs from the driver when it is driving the equivalent of a memory plane are shown. The note terminates with a paragraph on the future prospects for this type of driver.

1. A COMPARISON OF POINT-CONTACT AND JUNCTION TRANSISTORS AS CORE DRIVERS

The transistor core-driver for fast switching magnetic cores must possess sufficient power handling capacity, a fast rise time or high-frequency response, and a high output impedance.

Although the point-contact transistor has a higher frequency response than present junction transistors, its power handling capacity and output impedance level are much smaller.

Due to its extremely high output impedance the junction transistor is inherently a better current source than a point-contact transistor. The output impedance of a junction transistor is in the range of 500 KΩ to 1 MΩ while that of the point-contact transistor is only about 20 KΩ.

At the present time most transistor manufacturers are concentrating on the production of junction transistors with a higher frequency response. Other work is directed toward the development of power junction transistors. The ideal core driver for a coincident current memory requires a combination of the two characteristics.

1.1 POWER LIMITATIONS

Above a temperature of about 60 - 80° C. germanium will act as though it were intrinsic, i.e., the donor and acceptor type impurities which were added to control the conductivity of the germanium material, will no longer exert an appreciable effect. Thus the power-handling capacity of a transistor is governed by the temperature of the p-n junction. As the temperature depends largely upon the current density in the junction area, the larger the contact area the greater the power and current rating of the unit will be.

In the point-contact transistor the contact area is governed by the cat whisker electrodes which are very small. The power rating on this unit is therefore relatively low and it does not appear to be an easy matter to increase it.

The contact area in a junction transistor depends upon the area of the bulk of germanium which can always be increased. Therefore, the future in large power handling transistors lies with the junction transistor, and in fact, some transistors have already been developed which can handle several watts of power. However, due to the large junction areas in these units the collector capacitance has been greatly increased, and thus they have a very poor frequency response, i.e., f_{co} lies in the audio range.

A transistor found to be acceptable is a low-power commercially-built npn transistor with $f_{co} = 2$ mc, which has been modified to allow a larger collector power dissipation. It will be discussed later in the paper.

1.2 FREQUENCY RESPONSE

The higher frequency response of point-contact transistors as compared to junction transistors is mainly due to three effects. These are:

1) The mechanism through which the minority carriers flow from the emitter to the collector.

2) The spacing between the emitter and collector electrodes.

3) The collector capacitance.

In the point-contact transistor the distance that the minority carriers must traverse is very small since the two terminals are only about 0.002" apart. Furthermore, the carriers move mainly under the influence of an electric field at the points. This field produces a relatively fast movement of the carriers and a resultant high frequency response. The small collector capacitance of this unit also contributes to its good frequency response.

In the junction transistor the applied field has very little effect on the flow of carriers in the base region and so the flow is mainly due to a diffusion of the minority carriers in the germanium. This in itself would limit the frequency response of the unit, for the process of diffusion is a relatively slow one. Aside from the above consideration, the physical structure of the unit, i.e. the width of the base region, as well as its large collector capacitance are detrimental to a high frequency unit. If one is willing to accept small power dissipations the junction areas can be made smaller and an f_{co} in the order of two megacycles can be achieved.

2. THE GROUNDED-EMITTER CONNECTION OF THE JUNCTION TRANSISTOR

Since α_e for a junction transistor is less than unity, the first circuit which was evaluated was the grounded-emitter connection which affords a large current gain. The standard equivalent circuit for the grounded-emitter connection is shown in Fig. 1A. Another useful equivalent circuit for the grounded-emitter connection can be derived by the usual methods employed in network synthesis.

Any two terminal-pair network can be represented by the following equilibrium equations: (Fig. 1B)

$$V_1 = I_1 Z_{11} + I_2 Z_{12} \tag{1}$$

$$V_2 = I_1 Z_{21} + I_2 Z_{22} \tag{2}$$

By adding and subtracting $I_1 Z_{12}$ in equation 2) we obtain

$$V_2 - I_1 (Z_{21} - Z_{12}) = I_1 Z_{12} + I_2 Z_{22} \tag{3}$$

An equivalent circuit which can be represented by equations 1) and 3) is shown in Fig. 1C. In this diagram the $I_1 (Z_{21} - Z_{12})$ voltage source has been converted to a current source. From the usual grounded-emitter equivalent circuit, Figure 1A, the values of the open-circuit transfer impedances, which are required for the equivalent circuit of Fig. 1C, can be obtained as follows:

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2 = 0} = r_b + r_e \tag{4}$$

$$Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1 = 0} = r_e \tag{5}$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2 = 0} = r_e - \alpha_e r_c \tag{6}$$

$$Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1 = 0} = r_e + r_c (1 - \alpha_e) \tag{7}$$

When these values are substituted into the equivalent circuit of Fig. 1C and V_1, I_1, V_2, I_2 are replaced by V_b, I_b, V_c, I_c respectively, the circuit in Fig. 1D is obtained.

2.1 THE TRANSFER FUNCTION OF GROUNDED-EMITTER CIRCUIT

The usefulness of the circuit of Fig. 1D is readily demonstrated when the transfer function of the circuit is calculated. This equivalent circuit permits us to compute the transfer function I_c/I_b without regard to any internal current such as I_e. It should be noted here that the dependent current source is expressed in terms of the input current I_b not the emitter current.

If such factors as collector capacitance and transit time are to be included in the calculation, r_c becomes paralleled by the collector capacitance and

$$\alpha_e = \frac{\alpha_o}{1 + \tau s} = \frac{\alpha_o}{1 + j\frac{f}{f_o}} \tag{8}$$

where α_o is the current gain, in the grounded-base connection at low frequencies, and f_{co} is the cut-off frequency of the unit in the base connection.

If both effects are included the result will be so complicated algebraically that it will be of no practical use. For a more or less qualitative result the collector capacitance will be neglected. This assumption is valid for very low load impedances. In our case the result will be on the optimistic side. The exact calculation is given in the appendix. The result is

$$I_c(t) = +\frac{\alpha_o I_b}{(1-\alpha_o)}\left\{1 - \left[1 + \frac{r_e(1-\alpha_o)}{\alpha_o r_c}\right]e^{-\frac{(1-\alpha_o)}{\tau}t}\right\} \tag{9}$$

There are three things to note in this equation. First, there is a current gain of $\alpha_o/(1-\alpha_o)$ which can be very large if α_o is very close to unity. The time constant of the circuit has now become $\tau/(1-\alpha_o)$. The latter was to be expected for the gain-bandwidth product for the base connection must be the same for any other connection of the transistor. The third fact is that there is a small initial jump opposite to the direction in which I_c will finally flow. This is due to direct feed-through from the source since the dependent current generator has not yet had time to respond to the input signal. The waveform is given in Fig. 2.

If we assume that f_{co} = 2 mc in the grounded-base connection and α_o = 0.9, then for the grounded-emitter circuit f_{co} = 0.2 mc and the equivalent time constant is about 0.8×10^{-6} seconds. Then since the rise time is 2.2 time constants, the rise time in the grounded-emitter connection would be 1.7 μsec. This is a conservative estimate as mentioned previously, since the collector capacitance has been neglected.

The effect of the rise time of the driving current pulse on the output of the switching metallic cores[1] is shown in Fig. 3. From these pictures it is obvious that if we want a good ratio of "1" to "0" output at the sensing time, the rise time should be kept less than 1 μsec. The grounded-emitter circuit cannot satisfy this requirement when operated in the active region and must, therefore, be ruled out for the magnetic core driver. One can decrease the rise time by driving the collector into a saturated condition. This procedure actually involves taking a small part of a large exponential. It yields a decrease in effective rise time with a subsequent loss in gain. The rise time can be greatly reduced by this method but the resulting circuit will not be useable as a core driver. This is the case because the circuit will now act like a voltage source rather than a current source, since the current output is taken when the transistor is in the low impedance saturated state. This type of circuit may find applications in magnetic stepping registers or pulse circuits in general, where a gain in current is desired and the driver may approximate a voltage source without any disadvantages.

3. THE GROUNDED-BASE CONNECTION

Although the current gain in the grounded-base connection of a junction transistor is slightly less than unity, the frequency response is satisfactory for driving cores since rise times of the order of 0.2 μsec are obtainable from some commercial transistors. Unfortunately, these high-frequency transistors usually have power ratings of about 50 mw. In order to safely dissipate, say, 240 mw at the collector of the transistor, the unit must be cooled in some manner to keep the junction temperature down. One way to accomplish the cooling is to place the transistor in a glass enclosure and fill the space in the enclosure with silicon oil type DC550.[2] A transistor modified in the above manner was obtained from S. Schwartz. It is a Germanium Products n-p-n Junction transistor type 2520 K, with the following characteristics:

$$f_{co} = 2 \text{ mc}$$

$$r_{cr} = 1.09 \text{ m}\Omega$$

$$\alpha_o = 0.98$$

$$C_c = 13 \text{ } \mu\mu\text{f} \quad (Vc = 4.5v)$$

4. THE TRANSISTORIZED MAGNETIC CORE DRIVER CIRCUIT

The core driver which was developed on the basis of the above considerations consists of a voltage-source type input stage driving a

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[1] Magnetics Inc. Mo-Permalloy Core, 1/4 mil, 1/8" width, 1/8" diam, 5 wraps

[2] J. G. Mavroides and S. Schwartz - Lincoln Laboratory Technical Memorandum No. 38 - "Half Watt Power Transistors Obtained by Modifying Commercial Transistors." Sept. 16, 1953

current-source type output stage. The input stage is a single-transistor flip-flop which supplies a large current at a low impedance (it goes into the saturated region). The output stage converts the low impedance to a high impedance with only a slight loss of current. A circuit schematic diagram of the driver is given in Fig. 4A. The two pulse transformers shown are used to switch the circuit to the state specified in the diagram. When the point contact flip-flop is in the "on" (saturated) condition, diode d_1 and the emitter diode of the npn transistor are in the reverse direction. Thus there is no current supplied to the cores. If the first stage is driven "off" by applying a negative pulse at the emitter, both diodes switch to the forward conducting state. The collector voltage of the flip-flop is clamped to V_4 and the base voltage to V_2. Since the emitter of the npn transistor is in the forward direction at this time, it is in this state of the flip-flop that the driving current is sent through the core winding.

The clamping of the collector voltage to the value V_4 serves several purposes. The clamping action makes the current in the emitter of the second stage almost independent of the transistor in the first stage. The transistor in the first stage must just be capable of changing states. Also, since we would like the output current of the driver to be relatively large, this large current must be supplied by the flip-flop. This, in turn, means that large voltages must be employed. As the clamping of the collector voltage reduces the collector power dissipation in the "off" condition, it in effect permits us to use large voltages and yet not exceed the power ratings on the transistor.

4.1 DESIGN CRITERIA FOR FLIP-FLOP

The equivalent circuit of the driver is shown in Fig. 4B. In the design of the flip-flop stage of the core driver, there are three main points to be considered. These are:

1) In order to obtain a stable point in the "on" condition $\alpha_e \; I_{e\ \text{"on"}} > I_{c\ \text{"on"}}$

$$\text{or} \quad \alpha_e > \frac{I_{c\ \text{"on"}}}{I_{e\ \text{"on"}}} \tag{10}$$

The circuit must therefore be designed for a minimum α_e. This limit is chosen from practical considerations to be $\alpha_{e\ \text{"on"}} \geq 1.9$.

2) The amount of saturation should be not excessive. The saturation current is the net current flowing through the internal collector diode[3], when the transistor is in the saturated region. Thus:

$$\alpha_e \, I_{e\ \text{"on"}} - I_{c\ \text{"on"}} = I_{sat.} \tag{11}$$

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[3] The diode mentioned is the equivalent collector diode in the T-equivalent circuit for a transistor.

It has been shown experimentally that the "hole storage" time[4] increases with the magnitude of I_{sat} and with the length of time in saturation. Large hole storage effects necessitate using larger and/or wider triggering pulses to switch the flip-flop to the "off" state.

Furtherfore, since the rise time of the output current depends upon the length of time it takes the flip-flop to switch from the "on" to the "off" condition, a large amount of hole storage would be detrimental to a good rise time.

3) The desired current output must be specified. This current will be

$$I_o = \frac{V_3 - V_4}{R_2 + d_2 f} \qquad (12)$$

It should again be noted that the current is independent of the parameters of the transistor in the flip-flop.

4.2 THE V_e-I_e CHARACTERISTIC OF THE FLIP-FLOP

The V_e-I_e characteristic of the flip-flop shown in Fig. 5, can be determined by the ensuing procedure. A variable current source, I_e, is assumed to be applied at the emitter terminals. The break points in the V_e-I_e characteristic are then determined by the values of I_e at which the different diodes in the equivalent circuit are forced to change their state. In order to find these values of I_e, the circuit is cut across the diode or diode-and-battery combination of immediate interest. A Thevenin's equivalent circuit is then obtained for the remainder of the circuit looking from the cut terminals. When the resultant current is zero the diode is just about to switch; this condition therefore specifies a value of I_e.

The internal emitter resistance can be neglected when calculating the values of emitter current because it is in series with the current source I_e. However, it should be included when the value of V_e at a break point is sought.

It can be seen in Fig. 5 that the trigger voltages, based on the dc conditions, which are required to flip the circuit to the "on" position (~1.5 v) and to the "off" position (~8 v) are quite different. If a negative bias voltage is used in the emitter circuit, the emitter load line, (which is now the line V_e=0), will be effectively shifted downward in voltage. Thus the trigger requirements will be more nearly equal. The input requirements have not been stressed in the note because the problem of using the driver with a diode matrix has not been tackled yet. This will require bias batteries and perhaps a resistance in the

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[4] "Hole storage" is the effect which causes a delay when the transistor is pulsed so as to switch the unit from the saturated condition to the "off" condition.

emitter circuit, so that the trigger requirements and the "off" and "on" position points will be different.

It should also be noted that since the slope in the "on" condition depends mainly on R_1 and R_2 it cannot be changed inasmuch as other considerations specify the value of these parameters. This will be discussed later.

4.3 THE $V_c - I_c$ CHARACTERISTICS OF THE FLIP-FLOP

The collector characteristic is derived in the following manner. With a value of I_e specified from the $V_e - I_e$ characteristics, I_c and then V_c can be found by using Thevinen's equivalent circuit for the current sources.

From Fig. 6 and the equation for V_{c1}, it is obvious that the maximum power dissipation is determined largely by V_4, which should therefore be limited in magnitude to about 10 v.

The calculated voltages at the point where the transistor switches to the "on" state, (V_{c3}), and at the stable point in the "on" condition are not strictly correct. In order to make a good approximation to the actual voltages at these points r_b cannot be neglected, for if it is $V_{c3} = 0$. This we know is not true. In this region the usual equivalent circuit does not hold since the values of V_c obtained experimentally are about 1.5 volts lower than that calculated. One method used to overcome this difficulty is that of replacing the dependent current source and collector resistance by a constant voltage source.[5] The value of this voltage is naturally dependent upon the value of V_{c34}[6] for the transistor, but it will normally be about V =-1.5 volts. Experimentally, it can be seen that in the saturation region the value of r_b is much smaller than that in the active region. From the usual equivalent circuit it can be shown that the voltage $V_{c\ "on"}$ should be more positive than V_{c3}. The above facts, coupled with the fact that the actual measured voltage $V_{c\ "on"}$ varies with different transistors from 2 - 3.5 volts, make the following assumptions desirable:

1) The equivalent battery should be 1.5 v
2) $r_{b\ act} = 300\Omega$
3) $r_{b\ sat} = 100\Omega$

The maximum power dissipation is seen from Fig. 6 to be about 100 mw. As this occurs only for a short period of time, this power dissipation is not harmful to the transistor. The power dissipation in the "on" condition is also very important, since the flip-flop remains in this position except when an output pulse of current is desired. As explained previously, the calculated value of $V_{c\ "on"}$ is not too accurate.

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[5] This method was first used by Arthur W. Lo in "Transistor Trigger Circuits" Proc. IRE Nov. 52, p. 153.

[6] V_{c34} is the collector to base voltage with $I_e = 3$ ma and $I_c = -4$ ma.

Thus, the power dissipation in the "on" state varies with different transistors. When actual measurements were made on the circuit, the power dissipation at this point for several different transistors was found to be in the 30 - 50 mw range.

4.4 NUMERICAL VALUES FOR CIRCUIT PARAMETERS

The desired output current is about 12 ma. From collector power dissipation considerations, V_4 is chosen to be 10 v. V_1 and V_3 are conveniently chosen to be $V_1 = 40$ v and $V_3 = 50$ v. With larger voltages the power dissipation in the "on" condition will be excessive, since a larger value of $I_{c\ "on"}$ will be obtained. With these values and equation 12, section 4.1, the value of R_2 is calculated to be 3.2 K.

A value of $V_2 = 2$ v is chosen as a compromise between stability and input pulse height. A smaller value would mean the circuit might trigger with noise while a larger value would necessitate a large input trigger pulse.

The next value to be specified is that of R_1. Its magnitude is chosen as a compromise between stability and hole storage effects. As pointed out previously in equation 10), the requirement for a stable state in the "on" condition is

$$\alpha_e I_{e\ "on"} + I_{c\ "on"} > 0.$$

But, the larger the magnitude of the left-hand side of the inequality, the longer the hole storage time will be. The circuit was designed for a value of about $\alpha_e = 1.9$. This value seemed to be the best one experimentally. With this value of α_e the value of R_1 is found to be 5.5K.

4.5 TRANSISTOR SPECIFICATIONS FOR THE FLIP-FLOP STAGE OF THE DRIVER

The specifications for the point-contact transistor which is to be used in the flip-flop stage are:

1) $\alpha_e > 1.9$.

2) The value of V_{c34} should be limited to a maximum of about - 1.5 v since $|V_{c\ "on"}|$ increases as $|V_{c34}|$ increases. A larger $|V_{c34}|$ therefore means that there will be a larger collector dissipation in the "on" condition.

3) The storage coefficient[7] should be about 0.5 or less so that hole storage will not adversely effect the switching of the flip-flop.

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[7] Storage Coefficient $= \frac{\text{Turn-off-Time}}{(\alpha_e - 1)}$

4) The rise time of the transistor should be about 0.2 μsec if trigger pulses with small widths are desirable.

5. COLLECTOR OPERATING PATH FOR THE OUTPUT STAGE

The idealized collector operating path of the output stage is given in Fig. 7. The circuit normally sits at point A. When a current, with a trapazoidal waveshape, is applied to the emitter, i.e., when the flip-flop is pulsed to the "off" state, a large back voltage ($V_b = L_{eq}\frac{di}{dt}$) is developed across the cores. When the output current reaches its maximum value, $I_{co} = \alpha_e I_{e1}$, the voltage across the inductance jumps to zero and the equivalent impedance of the cores is just the d.c. resistance of the windings. The path followed is thus ABCD. At the end of the input pulse, i.e., when the flip-flop is triggered to the "on" condition, the emitter current decreases linearly to zero. The operating path is similar to the initial path but the back voltage is in the opposite direction. The operating path is now DEFA. Since $I_{c\text{"}o\text{"}}[V_{c2} + V_4]$ is set as close to the maximum power rating is as deemed safe, the return path leads to excessive power dissipations. This problem will be further discussed in section 7, when the equivalent circuit for the cores is considered.

5.1 THE OUTPUT IMPEDANCE OF THE DRIVER

The output impedance of the final driver stage is a good indication of the ability of the driver to act like a current source. The output impedance of the transistor (r_{co}) was measured and found to be about 1 mΩ. Figure 8 illustrates the ability of the driver to act as a current source. The load used here was a 330 ohm resistor, and the voltage across it was taken as a measure of the output current. The two waves shown in the picture were obtained at $V_{cc} = 25$ v and $V_{cc} = 4$ v. The change in current with the two values of V_{cc} was only 1 ma in a normal value of 12 ma. It should be noted here that a back voltage of 21 volts can be tolerated with only a 1 ma change in the output current.

5.2 SPECIFICATIONS FOR THE JUNCTION TRANSISTOR

As mentioned previously, in order to obtain a current output from the driver which has a fast enough rise time to be useful and which is at a high impedance level, the junction transistor must be operated in the grounded-base connection and in the active region. This, in turn, means that the transistor must be able to safely dissipate a large amount of power. The specifications for a junction transistor in this circuit are as follows:

1) $f_{co} > 1$ mc. This indicates that a rise time of 0.5 μsec is desired.

2) About 250 mw collector dissipation. This value will vary with the back voltage expected across the core. Since in section 5.1 it was shown that the back voltage can be a maximum of 21 v, and the current supplied is 12 ma, the power dissipation required is specified.

3) $\alpha_e > 0.9$. The value of α_e specifies the current loss in the output stage. Lower values of α_e can be used if the flip-flop stage is redesigned to give a little larger current output.

6. VOLTAGE MARGINS OF THE CORE DRIVER

The variation of transistor parameters in the flip-flop stage of the driver has very little effect on the output current as long as the circuit still changes state. This is due to the fact that the transistor is acting as a switch. The d-c voltages actually determine the current supplied to the second stage. These voltages must therefore be regulated.

The current output will not vary with the d-c voltage on the collector of the output stage because, as shown previously, the driver is a good current source.

With an input pulse of 12 v amplitude and about 0.25 μsec width, the following margins can be expected. (It must be noted that only one power junction transistor was available and only about 10 point-contact transistors were tried.)

$$V_1 = 40 \begin{smallmatrix} +6 \\ -5 \end{smallmatrix} \text{ volts}$$

$$V_2 = 2 \begin{smallmatrix} +4 \\ -1.5 \end{smallmatrix} \text{ volts}$$

$$V_3 = 50 \begin{smallmatrix} +2.5 \\ -2.5 \end{smallmatrix} \text{ volts}$$

$$V_4 = 10 \begin{smallmatrix} +2.5 \\ -2.5 \end{smallmatrix} \text{ volts}$$

When V_1 or V_2 exceeds the range of voltages shown, the circuit will not trigger. The nominal V_3 and V_4 voltages can be other than specified and the circuit will still operate. The range of voltages for V_3 and V_4 was determined by the stipulation that the current output not vary more than 1 ma from the nominal value of 12 ma.

7. THE EQUIVALENT CIRCUIT FOR THE CORES

The problem of deriving an equivalent circuit for the cores to be driven now presents itself. The output voltage from one core with a "non selection"[8] pulse of current through it is shown in Fig. 9. Since the driver can withstand a back voltage of about 21 v and the output voltage from one core is about 0.12 v, 180 non-selected cores in series can be driven. By using a current pulse with a longer rise time, the initial spike can be reduced to about 0.1 v and thus 200 cores can probably be driven.

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[8] A "non selection" pulse is the pulse obtained from only one driver in a coincident current memory system.

An equivalent circuit of the cores is shown in the dotted box in Fig. 10. The inductance L and resistor R_3 are used to give the initial spike and its decay time. Resistor R_2 is a resistor, which will have to be added to damp out the oscillations, while the diode and resistor R_1 are used to clamp the collector voltage to its nominal value of 25 v. Without this diode, the back voltage developed across the cores will make the collector voltage very large and thus the power dissipation will be exceeded. Resistor R_1 can be employed to make a compromise between the clamping action and the fall time of the current wave. With the diode included in the circuit, the operating path in the V_c - I_c characteristic of Fig. 7 is modified. It is now ABCDGA. The effect of including the diode in this circuit is shown in Fig. 11. It would be of very little practical value to determine specific values for these components since this is not an exact equivalent circuit of the cores. When the memory is built the final values can be determined.

8. REQUIRED POWER RATING OF THE TRANSISTOR WITH THE NUMBER OF CORES TO BE DRIVEN SPECIFIED

The power rating required of the junction transistor in the final core-driver stage can be approximated in the following manner:

1) From the value of coercive force (H_m) for the core, and its physical dimensions, the ampere-turns (NI) which must be supplied by each driver are specified. Each driver supplies half the ampere-turns required to bring the core to a magnetization, equal to H_m.

2) The current I_o is then specified. This, in turn, determines the turns N_o required on each winding.

3) The output voltage per core per turn, V_p, is determined experimentally with the above ampere turns applied.

4) The power rating of the transistor must be approximately

$$P = C N_o V_p I_o$$

where C = the number of cores to be driven in series.

9. FUTURE PROSPECTS

Through the use of complementary symmetry,[9] i.e., n-p-n and p-n-p junction transistors, it should be possible to design a driver which can "read" and "write" information on only one winding. This would save about one half of the windings on the core. The driver would consist of two of the above type drivers, one with a p-n-p output stage, the other

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[9] "Symmetrical Properties of Transistors and Their Applications", by G. C. Sziklai Proc.IRE June 1953 p. 717-24.

with an n-p-n stage (as discussed in this note). Since the cores are in the collector circuit of both drivers, each driver will act like a current source when driving the cores. A circuit schematic of the proposed driver is shown in Fig. 12. When the flip-flop voltages are larger in magnitude than the corresponding battery in the output stage of the drivers, a pulse of current is sent through the cores in the direction indicated in the diagram.

Signed Stanley Oken
Stanley Oken

Approved Donald J. Eckl
Donald J. Eckl

SO/er

Drawings

A-58306	Fig.	1A, 1B
A-58307	"	1C, 1D
A-58308	"	2
A-58312	"	3
A-58309	"	4A, 4B
C-58316	"	5
C-58358	"	6
A-58310	"	7
A-58313	"	8
A-58315	"	9, 10
A-58314	"	11
A-58311	"	12

APPENDIX I

CALCULATION OF COLLECTOR CURRENT RESPONSE FOR GROUNDED-EMITTER JUNCTION TRANSISTOR

The grounded-emitter equivalent circuit is shown in Fig. 1D. Assume that a load R_L and a voltage source V_{cc} are connected to the collector in order to make an operable circuit.

Let the driving pulse be a current step I_b at the base. Since we are interested only in the variational output current, V_{cc} is shorted out. Then, taking a Thevinen's equivalent circuit for the network to the left of terminals A - B, and for the dependent current source and collector resistance, we obtain the transient solution as:

$$I_c(s) = \frac{I_b(s)(\alpha_e r_c - r_e)}{[r_e + R_L + r_c(1 - \alpha_e)]} \tag{1}$$

with the substitutions:[10]

a) $I_b(s) = L[I_b(t)] = \frac{I_b}{s}$

b) $\alpha_e = \frac{\alpha_o}{1 + \tau s}$

equation (1) becomes:

$$I_c(s) = \frac{\frac{I_b}{(r_e + r_c + R_L)\tau}\left[(\alpha_o r_c - r_e) - r_e \tau s\right]}{s\left[s + \frac{r_e + R_L + r_c(1 - \alpha_o)}{(r_e + R_L + r_c)\tau}\right]} \tag{2}$$

This transform can be simplified by the method of partial fractions to:

$$I_c(s) = + \frac{I_b}{(r_e + r_c + R_L)\tau}\left[\frac{K_o}{s} + \frac{K_1}{s + B}\right] \tag{3}$$

where $B = \frac{r_e + R_L + r_c(1 - \alpha_o)}{(r_e + r_c + R_L)\tau}$

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[10] L = Laplace transform

$$K_o = \frac{\left[\alpha_o r_c - r_e\right]\left[r_e + r_c + R_L\right]\tau}{\left[r_e + R_L + r_c(1 - \alpha_o)\right]}$$

$$K_1 = \frac{\left[(\alpha_o r_c - r_e) + r_e\tau\right]\left[\frac{r_e + R_L + r_c(1 - \alpha_o)}{(r_e + r_c + R_L)\tau}\right]}{\left[\frac{r_e + R_L + r_c(1 - \alpha_o)}{(r_e + r_c + R_L)\tau}\right]}$$

Substituting in the values of K_o and K_1 into equation (3) and assuming $r_c \gg r_e + R_L$ (this is valid in the active region), we obtain as a final result:

$$I_c(s) = \frac{I_b \alpha_o}{(1 - \alpha_o)}\left\{1 - \left[1 + \frac{r_e(1 - \alpha_o)}{\alpha_o r_c}\right]e^{-\frac{(1 - \alpha_o)}{\tau}t}\right\}$$

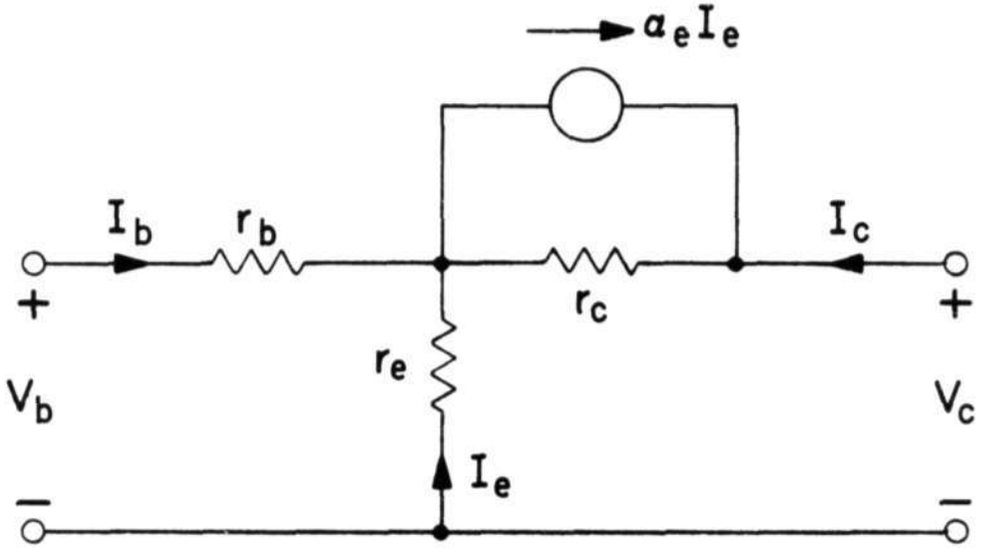


FIG. 1A
STANDARD EQUIVALENT CIRCUIT
FOR A TRANSISTOR IN THE
GROUNDED-EMITTER CONNECTION

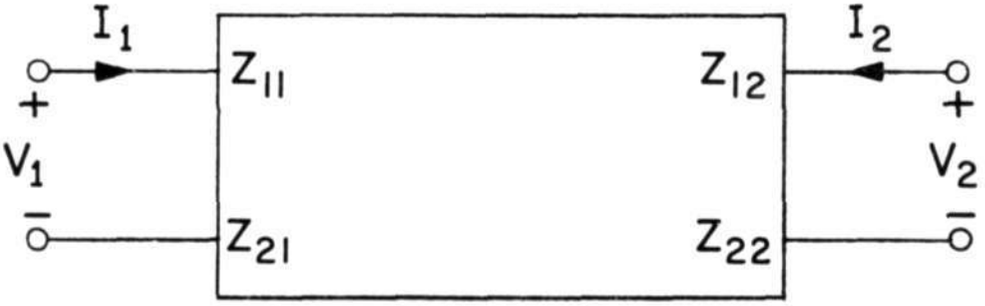


FIG. 1B
A GENERAL REPRESENTATION OF A
TWO TERMINAL PAIR NETWORK

A-58106

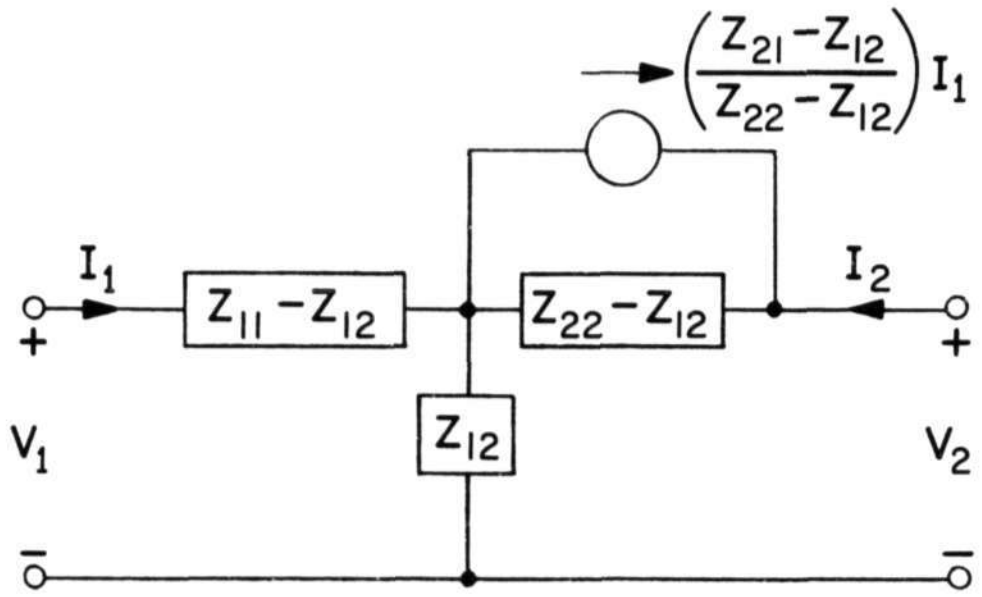


FIG. 1C
AN EQUIVALENT CIRCUIT
USEFUL FOR TRANSISTORS

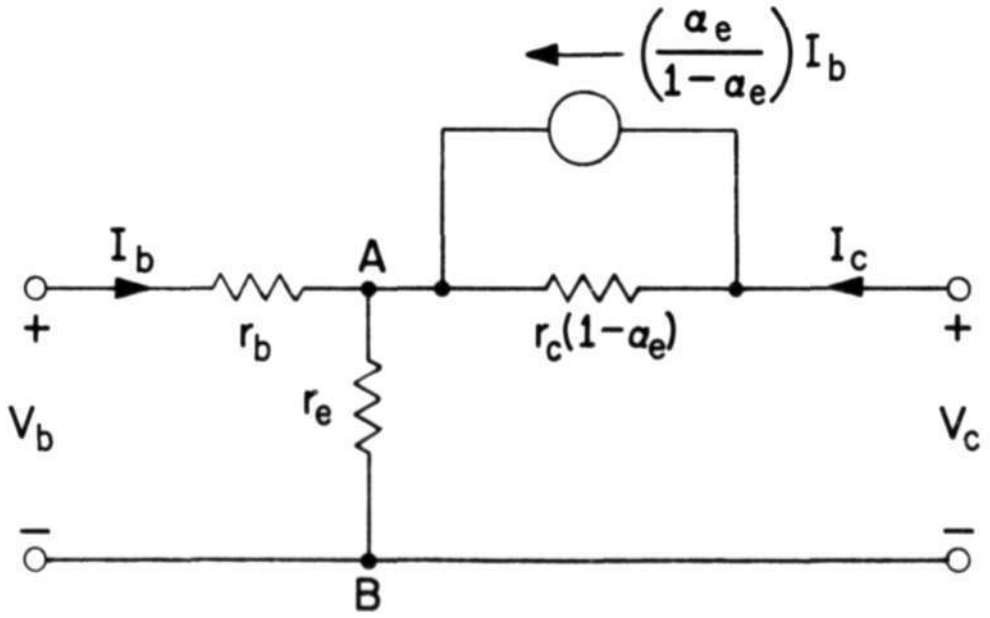


FIG. 1D
ANOTHER GROUNDED-EMITTER
EQUIVALENT CIRCUIT

A-58307

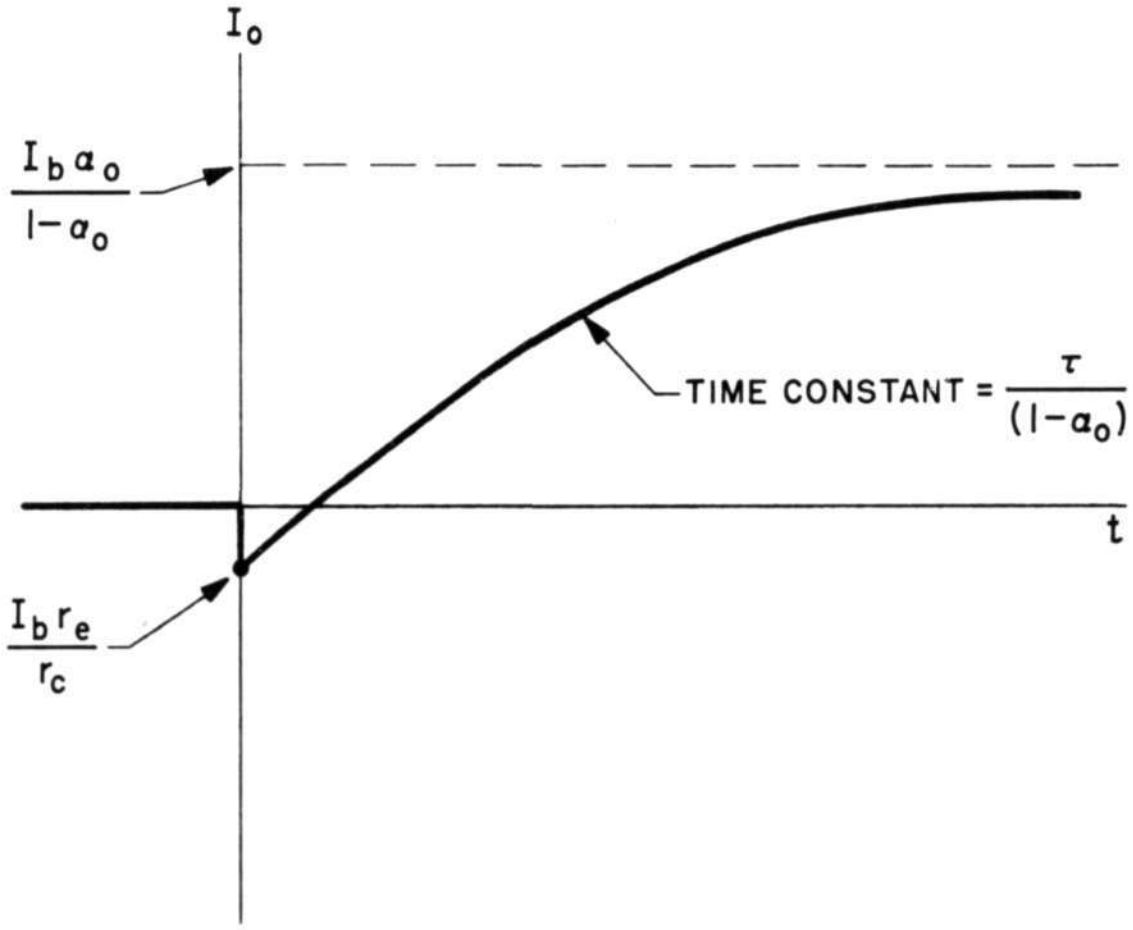
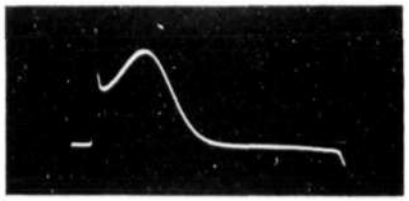


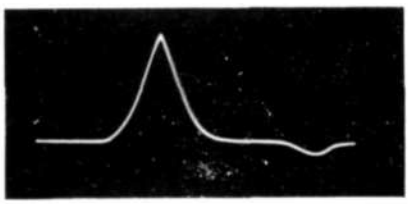
FIG. 2
THE OUTPUT CURRENT FROM
GROUNDED-EMITTER CONNECTION

A-58308

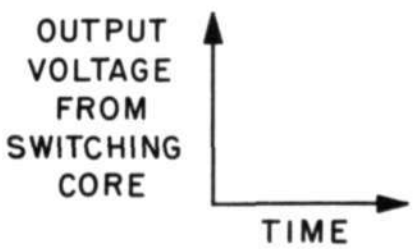


RISE TIME = 0.18 μsec
OF
DRIVING PULSE

RISE TIME = 1.0 μsec
OF
DRIVING PULSE



RISE TIME = 1.6 μsec
OF
DRIVING PULSE



TEN TURN SENSING WINDING
0.2 AMPERE TURNS

SCALES:
TIME: 1.0 μsec / cm
VOLT: 0.17 V / cm

FIG. 3
THE EFFECT OF RISE TIME OF CURRENT PULSE
ON OUTPUT FROM MAGNETIC CORES

A-58312

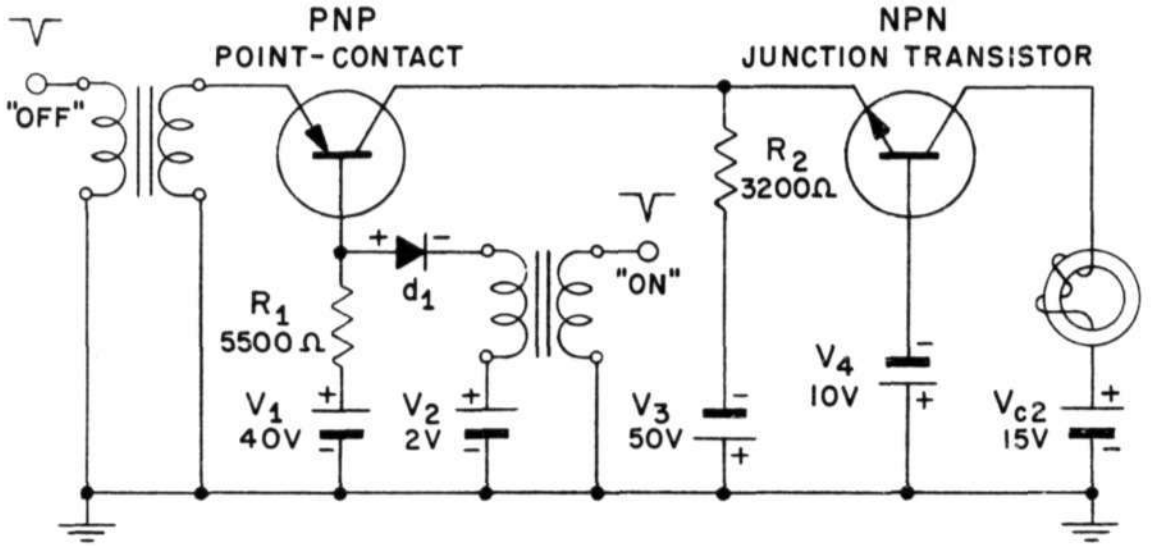


FIG. 4A
SCHEMATIC DIAGRAM OF CORE DRIVER

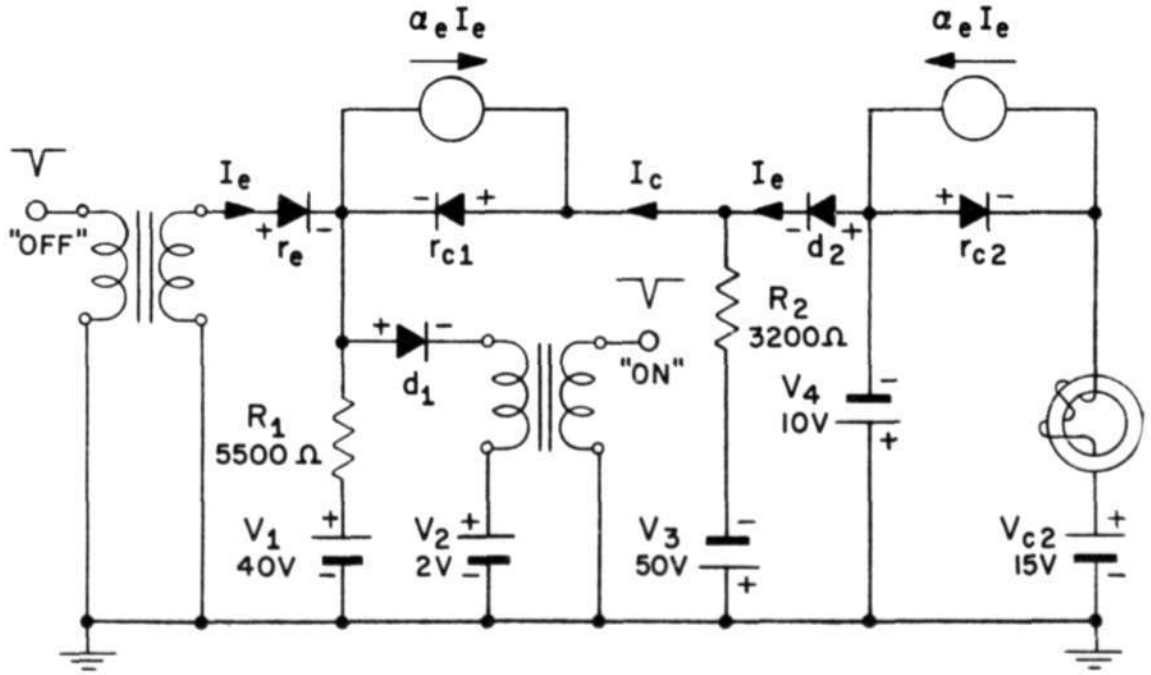
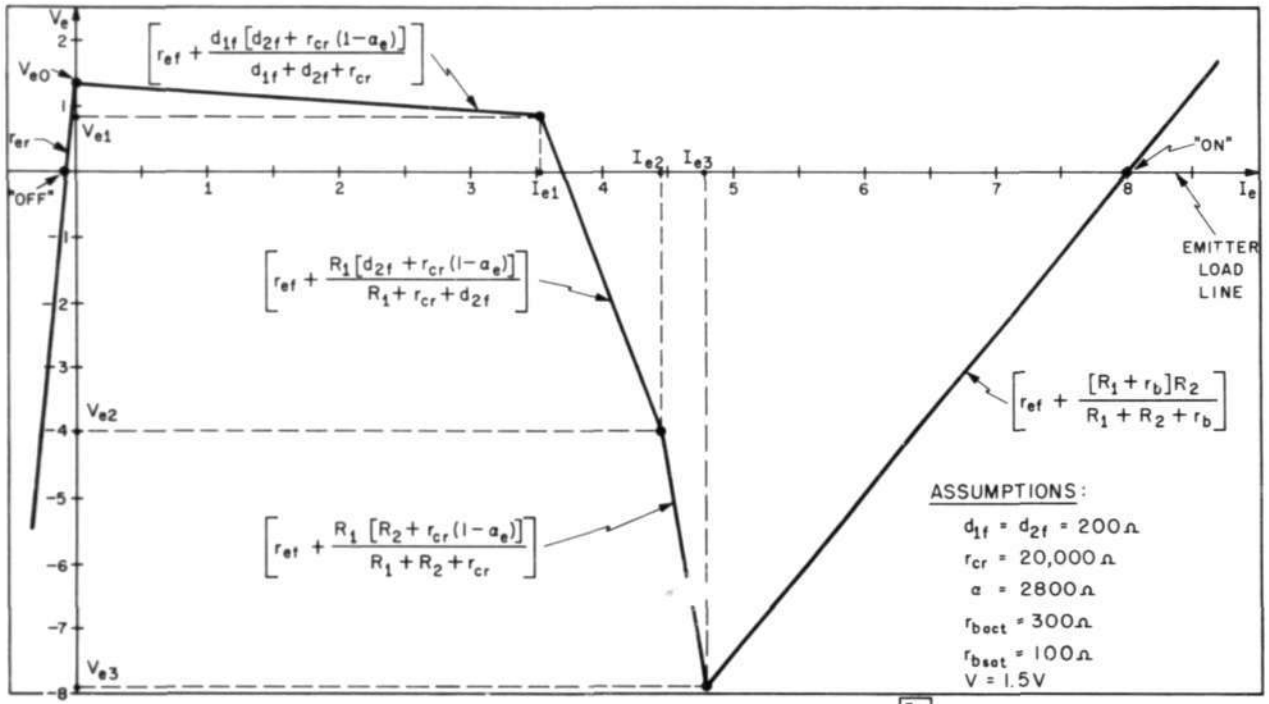


FIG. 4B
EQUIVALENT CIRCUIT OF CORE DRIVER

A-58309

C-58316



V_e

$$V_{e0} = \frac{V_2(r_{cr}+d_{2f}) - V_4 d_{1f}}{d_{1f}+d_{2f}+r_{cr}} = 1.4\ V$$

$$V_{e1} = I_{e1}\left[r_{ef} + \frac{d_{1f}[d_{2f}+r_{cr}(1-a_e)]}{d_{1f}+d_{2f}+r_{cr}}\right] + V_{e0} = 0.8\ V$$

$$V_{e2} = I_{e2}\left[r_{ef} + \frac{R_1[R_2+r_{cr}(1-a_e)]}{R_1+R_2+r_{cr}}\right] + \left[\frac{V_1[R_2+r_{cr}] - V_3R_1}{R_1+R_2+r_{cr}}\right] = -4V$$

$$V_{e3} = I_{e3}\left[r_{ef} + \frac{R_1R_2}{R_1+R_2}\right] + \frac{V_1R_2}{R_1+R_2} - \frac{V_3R_1}{R_1+R_2} = -7.9V$$

$$V_{e"ON"} = 0V$$

I_e

$$I_{e0} = 0\ ma$$

$$I_{e1} = \frac{\left[\frac{V_1}{R_1} - \frac{V_4}{d_{2f}+r_{cr}} - \frac{V_2[R_1+r_{cr}+d_{2f}]}{R_1[r_{cr}+d_{2f}]}\right]}{\left[\frac{r_{cr}[a_e-1]-d_{2f}}{r_{cr}+d_{2f}}\right]} = 3.6\ ma$$

$$I_{e2} = \frac{\left[\frac{V_3}{R_2} - \frac{[R_1+r_{cr}+R_2]V_4}{R_2[R_1+r_{cr}]} - \frac{V_1}{R_1+r_{cr}}\right]}{\left[\frac{R_1+a_e r_{cr}}{R_1+r_{cr}}\right]} = 4.4\ ma$$

$$I_{e3} = \frac{V_1+V_3}{[R_2a_e + R_1[a_e-1]]} = 4.8\ ma$$

$$I_{e"ON"} = \frac{[V_3+V][R_1+r_b] - V_1R_2}{r_{ef}[R_1+R_2+r_b] + [R_1+r_b]R_2} = 8.1\ ma$$

FIG. 5

EMITTER "N" CURVE FOR FLIP-FLOP

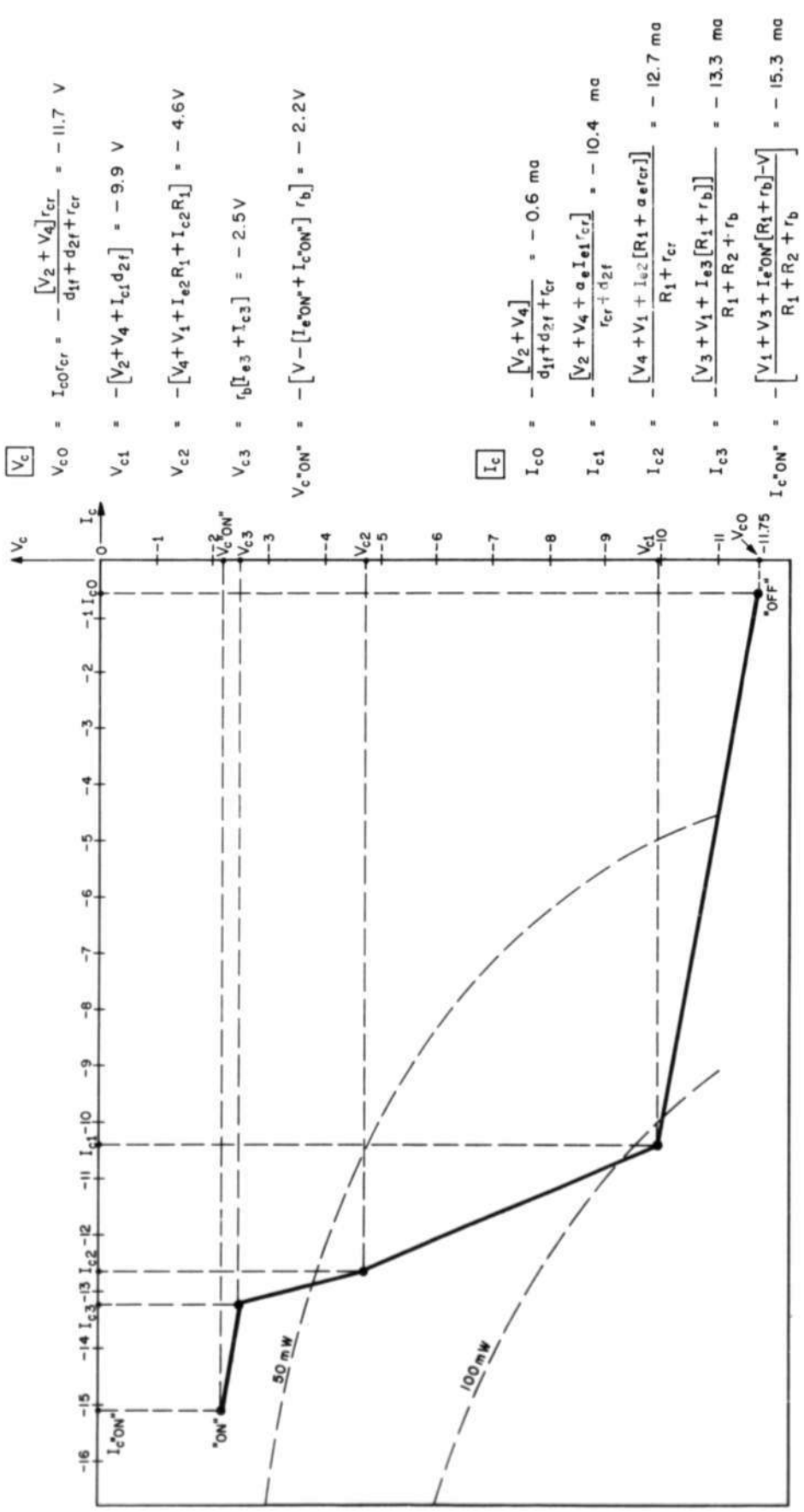
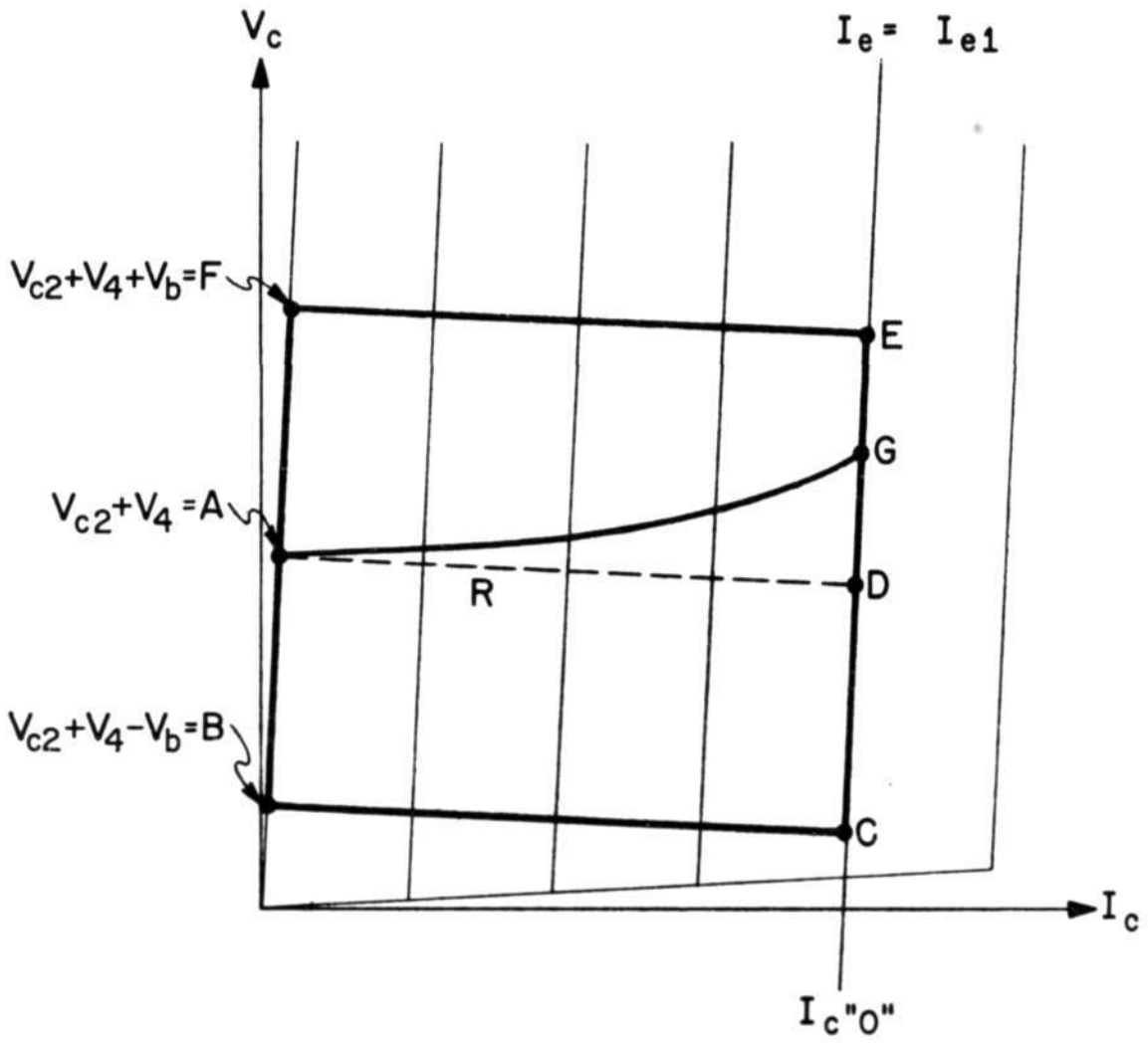


FIG. 6
$V_c - I_c$ CHARACTERISTIC FOR FLIP-FLOP

C-58358



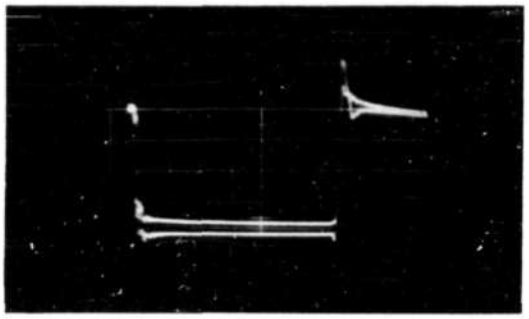
V_b = BACK VOLTAGE ACROSS THE CORES

R = RESISTANCE OF WIRE.

FIG. 7

THE IDEAL $V_c - I_c$ OPERATING CHARACTERISTIC FOR THE OUTPUT STAGE OF CORE DRIVER

A-58310



SCALES:

TIME = 1.0 usec / cm

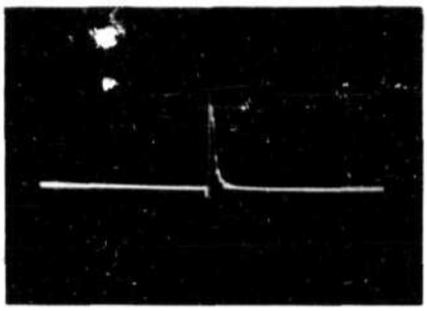
CURRENT = 3.0 ma / cm

LARGER CURVE V_{cc} = 25 VOLTS

SMALLER CURVE V_{cc} = 4 VOLTS

FIG. 8
CHANGE IN CURRENT OUTPUT WITH THE COLLECTOR VOLTAGE OF THE OUTPUT STAGE

A-58313



SCALES:

TIME = 1.0 μsec / cm

VOLTS = 0.05 V / cm

SENSING WINDING = 8 TURNS

FIG. 9

OUTPUT FROM CORE WITH "I_m" / 2 CURRENT INPUT

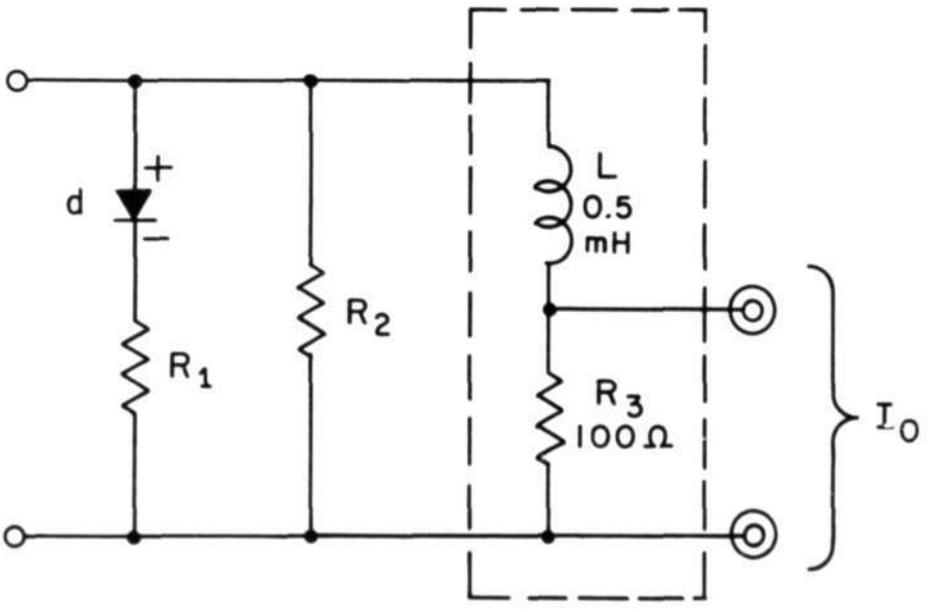
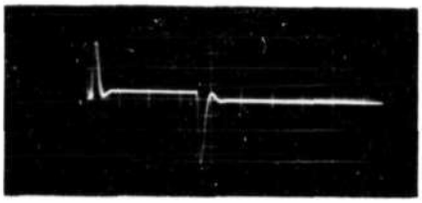
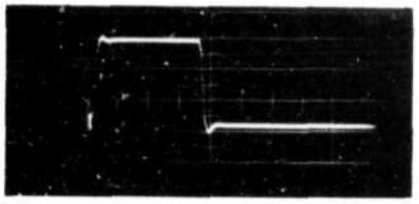
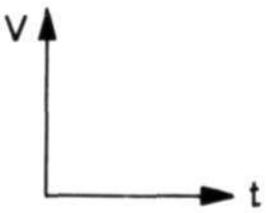


FIG. 10

AN EQUIVALENT CIRCUIT FOR THE CORES

A-58315

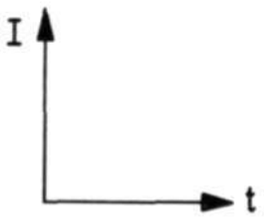
VOLTAGE OUTPUT	PARAMETERS	CURRENT OUTPUT
	DIODE = OUT R_1 = OUT R_2 = 2600 Ω	
	DIODE = IN R_1 = OUT R_2 = 2600 Ω	



SCALES :

VOLTS = 8 V / cm

TIME = 2.0 μsec / cm



SCALES :

CURRENT = 4.4 ma / cm

TIME = 2.0 μsec / cm

FIG. 11
OUTPUT FROM DRIVER WITH EQUIVALENT
"MEMORY PLANE" LOAD

A-58314

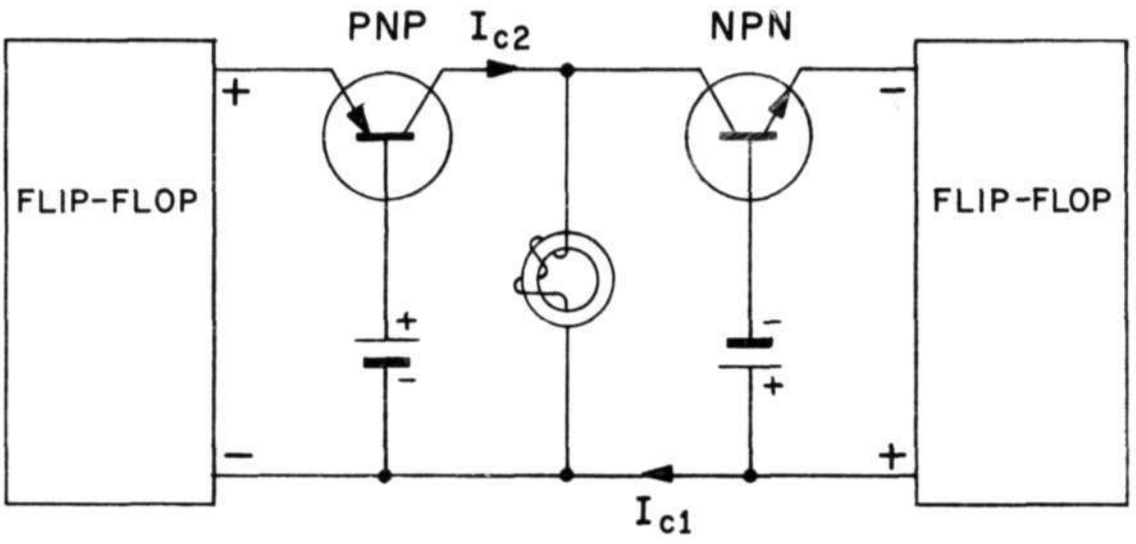


FIG. 12
A SCHEMATIC DIAGRAM OF THE
PROPOSED READ-WRITE DRIVER

A-58311

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