Division 6 — Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: BIWEEKLY PROGRESS REPORT FOR AN/FSQ-7 (XD-1), Sept. 14, 1953

To: AN/FSQ-7 Planning Group

From: A. P. Kromer, P. J. Gray

Equipment Power Supplies

Specifications are now being written for the D.C. supplies for AN/FSQ-7. A performance test has been run on a 150 V, 25 A Inet supply using a magnetic amplifier in the output stage. Performance was good, although the unit needed special attention and adjustment each time it was started. IBM will investigate this further.

It appears that the 0.2 farad capacitance in the filter section can be reduced by a factor of 4 or 5, without impairing performance, if a choke is used. This will be investigated in about 2 months when the unit is delivered here.

Cooling Equipment

A meeting was held at MIT this week with Francis Associates, at which preliminary specifications for the FSQ-7 cooling equipment were discussed. A meeting will be held in two weeks in Poughkeepsie at which time the consultants will give a preliminary description of equipment size, etc. The shortage of space in Building A is presenting a serious problem, as the cooling equipment will be considerably larger than the space presently allocated.

Arithmetic Element & Control

The arithmetic element model is now operative and work is in progress on determining its margins.

Report IM-46, which is a proposal for marginal checking of the central machine, was accepted except that the system will be initially automatic as well as manual.

A new pluggable unit design is underway at IBM. Trial layouts for etched wiring cards for all circuits in the arithmetic element are progressing well. Final layouts must await the completion and acceptance of a pluggable unit design.

Control switch block diagrams are being revised to insure that there are no more than three levels of cathode followers between flip-flops and c.p.o. units.

Internal Memory

The tests of the 64 x 64 plane were completed, using the 32 x 32 memory stall which has since been installed in WWI as a second bank of core memory. The test results were so promising that XD-1 design is proceeding on the basis of only one sense winding (and one sense amplifier) per memory plane.

Design work is essentially complete on MTC Memory, Model II. Drafting, procurement, and construction are beginning.

A large number of basic design decisions were made at a two-day meeting with IBM (at MIT) and the work should move forward rapidly from now on.

Memory Cores

Cores of the type to be used in the FSQ-7 are now operating in the second bank of magnetic core storage of WWI. General Ceramics has delivered enough of these cores so that we expect that we will have enough good cores to construct a 64 x 64 x 17 memory for MTC. Selection of these cores should be complete by the end of September.

Since approximately September 1, General Ceramics has been making cores for AN/FSQ-7 (XD-1) and expects to have 20,000 to 50,000 good cores by September 15, and be on schedule by October 15.

Neither MIT nor IBM is ready to perform 100% testing of XD-1 cores as they are shipped from General Ceramics. Our careful evaluation of General Ceramics production will be maintained at both MIT and IBM.

Radar Inputs

The magnetic core counter, magnetic delay register, and biased diode readout register are all operating at IBM.

The limits of the basic stepping register in these circuits are being evaluated here.

Difficulties encountered with the phone line demodulators point toward removal of these units from the mapper consoles to a central location for monitoring purposes. This change will require changes in the block diagram of the phone line input equipment which will be worked out in Poughkeepsie next week.

Input Buffer Drum

There is justification for the continuation of development of a low-speed flip-flop due to the fact that it reduces the number of cathode followers required. However, disagreement exists over the type of low-speed flip-flop to be used. This controversy should be resolved in another week.

The block diagram for the input buffer drum is complete, but block schematics cannot be completed until the following basic circuits are designed and approved: read amplifier, write amplifier, low-speed flip-flop.

A program has been initiated for tying in our efforts with those of Division 2 with regard to the connection of phone lines to the input equipment.

Central Display Generator & Selector; Display Console

A schedule for the display work has been agreed upon with IBM, and the various smaller tasks have been divided between MIT and IBM in order to avoid duplication of effort.

The character generator designed by W. Triest has been selected as the one to compete with the Charactron tube for use in FSQ-7.

Two Charactron guns have been received and are currently being mounted in 16" tubes.

It has been decided that there will be only two intensification levels in the display system. Track data will be interleaved and there will probably be 12 or 13 history points in each track.

Output Buffer Drum

A program of study on the output system has started at MIT. Included in this study group are R. Cypser, R. Jeffrey, I. Aronson, R. Hopkins and J. Jacobs. The purpose of the group is to: 1) Study the weapons which will be controlled by AN/FSQ-7; 2) Establish working relationships with the various groups having responsibility for ground-to-ground and ground-to-air communication and the groups who have the responsibility for the operation of the AN/FSQ-7 equipment; 3) Propose a design for the output equipment by February 1, 1954.

Signed: A. P. Kromer

Signed: P. J. Gray

Approved: N. H. Taylor

APK:PJG/mmt