

Memorandum M-2467

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Division 6 - Lincoln Laboratory  
Massachusetts Institute of Technology  
Cambridge 39, Massachusetts

SUBJECT: JOINT MIT-IBM MEETING ON MEMORY-CORE MEASUREMENT, October 13, 1953

To: Jay W. Forrester

From: David R. Brown

Date: October 20, 1953

Abstract: MIT and IBM will share the core-testing program to obtain 150,000 good cores by January 1, 1954. MIT will perform two thirds of the testing, and IBM (High Street) one third. Cores must be tested at a rate of 15,000 tests per day beginning November 2. IBM will perform all plane testing.

The specifications for General Ceramics cores are changed to accept  $V_1$  from 0.090 volt to 0.120 volt. Accepted cores will be divided into two groups for plane assembly.

Separate specifications will be written for cores to be supplied by RCA Victor.

A meeting at IBM, High Street, was held on October 13, 1953, attended by C. Balliet, R. Blessing, J. Crowe, N. Edwards, A. Heckel, R. Henn, S. Houck, J. Johnson, V. May, W. Strom, R. West, and W. Wittenberg of IBM and D. Brown, J. McCusker and W. Papian of MIT.

The agenda for the all-day meeting included: (1) a review of the previous meeting, (2) establishment of the time schedule and assignment of responsibilities for the core-testing program, (3) specifications and methods of test, and (4) coordination of measurement techniques.

The minutes of the previous meeting held on September 24, 1953, and reported in Memorandum M-2449 were reviewed. The last sentence in the fourth paragraph on page 1 which read, "Two MIT Mod. V core drivers were exchanged for two Codeco Mod. VI core drivers." should be changed to read, "Three MIT Mod. V core drivers were exchanged for one Codeco Mod. V core driver and two Codeco Mod. VI core drivers." The membership of the committee should not be as rigid as that proposed in paragraph 9 on page 2. The same groups should be represented, but the representatives of those groups will be different persons from time to time depending upon the current situation.

The principal business of the meeting was the establishment of the time schedule for testing cores for the XD-1 high-speed memory and assignment of responsibilities for carrying out the tests.

One most essential part of the core-testing program is that which will provide 150,000 tested cores by January 1, 1954, for the construction of a single high-speed magnetic-core memory. If the specifications now being used for testing cores for the second MTC memory are retained and lots of cores continue to have the same yield, approximately five tests are required for each good core obtained. The number of tests performed on each good core is less than five but the figure of five tests per core is properly weighted to take into account the yield obtained. A total of 750,000 tests must be performed between now and January 1. Assuming 50 working days between now and January 1, this is 15,000 tests per day or 3,000 good cores per day. In addition to this number of tests per day, lot evaluation and plane tests must be carried out.

The following equipment would have to be in operation before November 1 in order to carry out this part of the core-testing program: three semiautomatic core testers for 100-percent tests, one semiautomatic core tester for sample tests, one special setup for delta measurements, and one plane tester. The total manpower to be assigned directly to the job should include three engineers and eight to ten laboratory assistants. The space needed would be less than 1,000 square feet.

At the present time, MIT has one semiautomatic core tester and one fully automatic core tester in operation which have been performing 15,000 tests per day providing an average of 3,000 good cores per day. In addition, MIT has a special setup in operation for the evaluation of delta voltages, and a plane tester, which is proving to be inadequate. To carry out the entire part of the core-testing program being discussed, MIT would require one additional semiautomatic core tester for sample tests.

At the present time, IBM (High Street) has one semiautomatic core tester in operation and expects to have a second semiautomatic core tester in operation in the near future. Two additional semiautomatic core testers would be required, a special setup for delta measurements, a plane tester, and additional space. The required number of laboratory assistants could be readily obtained, but the assignment of engineering manpower might prove to be difficult.

At IBM ( Plant 2) one manual core tester is in operation. This setup is required for sample measurements on cores submitted by other suppliers and is not available for this part of the core-testing program.

IBM (High Street) will plan to do plane testing.

IBM (High Street) and MIT will share the core-testing program. Each will do lot evaluation and 100-percent testing. MIT will perform 10,000 tests per day to yield 2,000 good cores per day and IBM will perform 5,000 tests per day to yield 1,000 good cores per day. IBM (High Street) will have in operation by November 2 the facilities necessary for 5,000 tests per day. These facilities will include one semiautomatic core tester for 100-percent tests, one semiautomatic core tester for lot evaluation, and one special manual setup for delta measurements. J. Crowe will list the equipment and manpower in addition to what he now has so that these items can be obtained without delay. A plane tester will be put into operation at High Street during the first week in November.

During the meeting repeated emphasis was placed on the fact that the subject under discussion represented only a portion of the core-testing program. It omits liaison and coordination, test equipment development, and special measurements. More important, it provides for only 150,000 good cores by January 1, these core being obtained from General Ceramics production. This quantity will be sufficient for only one memory, whereas XD-1 and XD-2 together will require a total of four memories. In addition, it makes no provision for testing cores from other suppliers, eventhough RCA is now commencing production.

At the present time, the memory-core specifications are contained in four documents: (1) "Specifications for a Ferrite Memory Core," Engineering Note E-563, June 30, 1953; (2) "Sample Testing Procedure," July 15, 1953; (3) "Revision #1," July 17, 1953; and (4) "Interpretation of Memory-Core Specifications," Memorandum M-2420, September 22, 1953. These contain the specifications for cores from General Ceramics. Note that Memorandum M-2420 changes the test temperature from 21 C to 24 C plus or minus 1 C.

The specification on fracture strength in paragraph 3.2 of Engineering Note E-563 is changed from 500 grams to 400 grams.

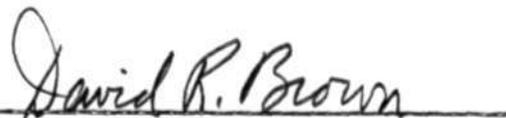
The specification on the pulse response,  $V_1$ , in paragraph 4.2 of Engineering Note E-563 is changed from a minimum of  $0.1095$  volt and a maximum of 0.115 volt to a minimum of 0.090 volt and a maximum of 0.120 volt. The change in the specification for the pulse response,  $V_1$ , will permit a greater yield from General Ceramics production. For assembly into memory planes, the cores accepted from General Ceramics will be split into two groups, one having limits on  $V_1$  of 0.090 volt to 0.105 volt and the other having limits 0.105 volt to 0.120 volt. Cores from only one group will be used in any given memory plane.

RCA Victor has produced sample lots of memory cores which are quite acceptable from the point of view of performance. Their cores, however, are not exactly like General Ceramics cores and do not meet the specifications. A new set of specifications will be necessary for cores from RCA Victor. This means that cores from General Ceramics cannot be mixed with cores from RCA Victor in the same memory bank. RCA Victor should be asked to prepare a 10,000-core lot for selection of cores to build a 64-by-64 memory plane. Measurements on this memory plane will permit a more critical evaluation of RCA Victor memory cores.

R. West is to undertake another round robin to coordinate measurement techniques at the different core-testing sites during the last part of October. Sufficient time should be allowed at each site to remove all disagreements and clarify any questions. One man from IBM and one man from MIT will work 100-percent of the time on the coordination of measurement techniques until satisfactory agreement is found. The coordination of measurement techniques, however, is only a portion of the liaison program.

DRB/jk

Signed



David R. Brown

cc: Group 63 Staff  
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 W. N. Papian, IBM (via Kromer)