Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: IBM - MIT MEMORY CONFERENCE OF 22 SEPTEMBER 1953

To: N. H. Taylor

From: W. N. Papian

Date: 25 September 1953

Joint IBM-MIT meetings were held at Project High on the 22nd of September to discuss the XD-1-2 internal memory.

The people involved included:

IBM	MIT
F. Durgin	W. Canty
N. Edwards	E. Guditz
R. Henn	C. Laspina
W. Ratledge	J. Mitchell
W. Strohm	W. Papian
W. Wittenberg	D. Shansky

A. The two unsettled questions which were carried over from Memorandum M-2405 (on the September 9th conference) were settled as follows:

1. The increase in tube count necessary to drive the electrically quartered crystal matrix is too large and its advantages are too small; electrical quartering will not be done. However, partly because air-conditioning duct-work has to run vertically through the center of the memory stall, each crystal matrix will be physically quartered, and each quarter assembled on a subpanel mounted on back of a selection-plane driver panel.

2. The X and Y crystal matrices will be physically mixed. The resultant increase in matrix-drivers tube count was shown to be negligible and no resulting maintenance disadvantages can be demonstrated once it is agreed that, as A.1 above states, each crystal matrix quarter is to be built right on a selection-plane driver quarter.

B. Other items which were discussed follow:

1. Circuit schematics for the Digit-Plane Driver and Sense Amplifier/Discriminator are to be ready for release from the memory sections on October 1. The -30 and +90 supply voltages to the S.A.D will be marginal checkable; the gain control range will be reduced in order to reduce effects of potentiometer value drift. IBM will commence packaging these units into standard plugin chassis as soon as possible.

2. There will be as many read and write gate-generator power amplifiers as are needed to give a short enough rise time out of the selection-plane-driver pulse transformers (approximately 1/2 μsec). Experimental work to determine this will be performed at MIT and IBM aimed at fixing the number by October 1.

3. A "Proper" Block Schematic is in IBM's drafting room. Memory control and timing will conform to IBM report H-40. The maximum overall "jitter" expected from the delay-line memory control may be as much as 1/4 microsecond; the delay in machine timing during memory access must safely overlap this period.

4. Stall layout is coming along nicely and is in line with the latest thinking about air-conditioning. Both IBM and MIT are in touch with Francis Associates, and there appear to be no insurmountable difficulties in the way of keeping the cores in the stack at the desired 75 ± 3 degrees Fahrenheit while the rest of the stall contains slightly pressurized cold air.

C. Further detailed questions will be settled by the teams working on the circuitry and layout of the XD-1-2 memories. Smaller, but more frequent visits will take place during the next few weeks.

Signed: W. N. Papian

WNP/rb

cc: D. R. Brown
N. Edwards (IBM
J. McCusker
W. Wittenberg (IBM
Group 62 Section Chiefs & Memory Section
N. Daggett