Division 6 - Lincoln Laboratory
Massachusetts Institute of Technology
Cambridge 39, Massachusetts

SUBJECT: IBM - MIT MEMORY CONFERENCE OF SEPTEMBER 9, 1953

To: N. H. Taylor

From: W. N. Papian

Date: September 11, 1953

Joint IBM-MIT meetings were held at MIT on the 8th and 9th of September to discuss the XD-1 internal memory.

The people involved included:

IBM	MIT
F. Durgin	W. Canty
N. Edwards	E. Gates
R. Henn	E. Guditz
H. Ratledge	J. Mitchell
W. Strohm	W. Papian
C. Taft	D. Shansky
R. West	
W. Wittenberg	

The meetings were also attended at times by W. Ayer, J. Bassett, R. Best, N. Daggett, and B. Remis.

A. The following is a list of items on which a common point of view was reached.

1. There will be only one memory plane of 4096 cores on a unit frame.

2. All planes will be identical.

3. Coordinate wire spacing in the planes is to be 0.1 inch center to center.

4. Frame dimensions are to be as small as possible consistent with A3, with structural strength, and with lug spacing problems. The frame is likely to be a slightly smaller version of the MTC II aluminum casting.

5. Plane and strips are to be "MTC style" using the new CTC lug; coordinate wires are to come thru a center line of holes in the thin phenolic strip, then connect to the two rows of staggered

lugs. Plane-to-plane connections will be soldered short busses as in MTC.

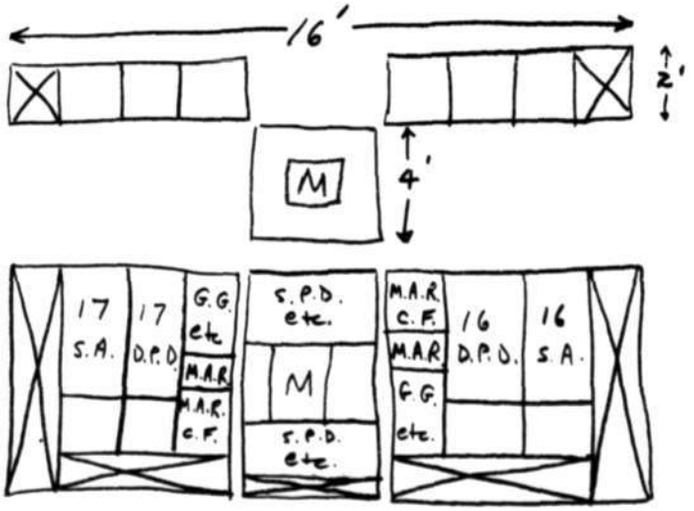
6. Henn and Guditz will decide on plane's wire sizes; coordinate lines will be 32, 33, or 34, digit and sense lines probably 34, all quadruple formex.

7. MTC plane wiring sequence will probably be used (digit and sense windings to go in last) but wiring-aid jigs may be used.

8. MTC sense-winding configuration will be used but enough spare lugs will be available so that the winding may be split if that turns out to be necessary.

9. The memory array, or stack, will be quasi-pluggable; that is, it should not be necessary to use a soldering iron or screwdriver on the electrical connections in order to remove it. Digit-plane connections from memory stall to module will be by shielded single-wire, such as coax, with BNC type of connection at the array end and standard module connection at the other end. Sense-winding connections will be roughly the same except that shielded twisted pair is needed.

10. The memory layout and floor plan will be split in half along the same general lines as the rest of the internal machine. The following plan and layout look good.



The rather large amount of floor space is required because of the small amount of usable video-equipment space available in the standard module.

11. Memory control will be designed using basic circuits.

12. A tentative block sketch and timing diagram were approved. IBM will have a proper Block Schematic (including timing diagram) drawn up and issued as soon as possible.

13. The sense amplifier and digit-plane driver basic circuits will be essentially those of the existing MTC II prototypes. Packaging will be in the XD-1 standard plug-in unit.

14. Selection-plane transformer-primary current regulation will be no worse than 2% for 120% to 60% driver tube variation. Currents will be adjustable manually as in MTC II and, for marginal checking, by variation of the negative supply voltage to the cathode resistors, if possible.

B. Unsettled questions hinge around the breakup and layout of the address-selection system and other equipment in the memory stall.

1. IBM proposes breaking up each crystal matrix into quarters, driving each quarter separately and mounting each quarter (with its cathode followers) on the selection-plane driver panel. This looks fairly attractive from the trouble-shooting point of view and will probably be accepted provided it does not raise the tube count seriously.

2. IBM also proposes mixing the x and y matrices physically in such a manner as to make the connections and terminations on the memory stack more symmetrical and, thus, reduce the density of the terminating components. MIT thinks this unattractive from the trouble-shooting point of view and because it requires larger leads from MAR cathode followers to the matrices. However, if proposal B1 above is accepted, these objections will be seriously diminished.

Both of these problems are being studied at IBM and MIT. The next joint meeting is scheduled for the week of September 21 at which time the decisions will be made.

Signed: William N. Papian
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WNP/rb

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