

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: PROJECT GRIND MEETING OF JUNE 24, 1953 (First Day)

To: AN/FSQ-7 Planning Group

From: A. P. Kromer, R. P. Mayer

Date: June 29, 1953

Abstract: At this meeting slowed down video inputs, video mappers, and slowed down video input registers were discussed. A general description for the input registers was agreed upon.

Members Present:

M.M. Astrahan	IBM		A.P. Kromer	MIT	
R.L. Best	MIT		W. McMillan	IBM	
E.W. Bivans	MIT		R.P. Mayer	MIT	
J.M. Coombs	IBM		J.A. O'Brien	MIT	
R.P. Crago	IBM		K.H. Olsen	MIT	
D.J. Crawford	IBM		M.J. Raffensperger	IBM	
S.H. Dodd	MIT		E.S. Rich	MIT	
N.P. Edwards	IBM		H.K. Rising	MIT	
R.R. Everett	MIT		H.D. Ross	IBM	
J.F. Jacobs	MIT		H.K. Smead	MIT	
H.J. Kirshner	MIT		N.H. Taylor	MIT	

The object of the minutes of the Project Grind meetings is to put on record some of the decisions made and some of the reasons for these decisions. Any problems will be brought into the open so that decisions can be made as soon as possible. It was also agreed that everyone should get even tentative plans for various parts of the system so long as everyone knows that they are tentative. If there are any errors or ommissions, they should be called to the attention of A. P. Kromer or R. P. Mayer.

I. Slowed Down Video

The discussion on the slowed down video system was somewhat short largely because some of the people responsible for this work are on vacation. It was generally agreed that only one type of demodulator will be used and that IBM will assign a man to maintain contact with the work of Group 24 on

the demodulator. Group 24 will be developing the electronics of the demodulator. Breadboard work including margins using computer tube types will be completed by September 1, 1953. IBM will (they) do the mechanical design, etc., and produce the equipment. The logic required for interconnecting three standard demodulators for the large radar will be arranged by the computer group (MIT-IBM).

II. Video Mappers

It was generally agreed that parallax between photo tube and the human eye is a big problem. IBM will work on half-mirror techniques and so forth but allowing the operator to look on either side of the photo tube when actually placing the "map" may be a satisfactory alternative to start.

It is probably desirable to show what has been mapped out. It was agreed that a method of doubling the intensity of spots which are actually seen by the photo tube should be investigated, (perhaps tried out in the Cape Cod System). The photo tube will not be sensed during the reintensification time.

The sweep for the mapper will be obtained from a rotating yoke and a linear range sweep. The major requirement on this sweep arrangement is that it be repeatible. This sweep arrangement also provides a time base system for the rejection of spurious r and θ pulses going to the counters. The rotating yoke will be synchronized with the θ pulses. Slip rings were suggested for this but a photo tube system is also being designed. Either slip rings or photo tube signals will be mixed with the θ signals to control magnetic brake. IBM will make further investigations of various techniques used in video mappers, consulting with Ed Rich, Cape Cod and Group 24.

Perhaps it will be desirable to omit a system for synchronizing the north markers. It may be much more practical to use a high inertia azimuth sync system perhaps using a synchronous motor and not a magnetic brake. A manual control of the approximate speed would be used for roughly synchronizing the mapper with the antenna. The reason for the high inertia system is that it is important to have the mapper follow the antenna so that a high volume of clutter is removed even though spurious r and θ pulses make the computer see targets in the wrong places.

There was some discussion concerning whether the SDV demodulator and a power supply should be placed in the mapper console but no conclusions were reached. It was generally agreed that the counters should not be in the mapper because they are not necessary for manual monitoring of the line and because all of the counters should be in a single rack so that the problem of reading them to a common drum register could be simpler. These problems are part of the packaging problem that shall be discussed at another meeting.

III. SDV Input Registers

The Cape Cod SDV system is somewhat different from that which will be used with XD1. It was agreed that the design for XD1 should be based on the storage tube SDV system even though some Cape Cod equipment might be used initially.

It was agreed that the computer program should take care of adding any fixed errors to the counters so that the counters can be kept simple.

The long-range radar will not use 3 counters stored in 3 places on the drum but will use 1 counter stored in 1 place on the drum. This simplifies the equipment somewhat and reduces the probability of storage on the drum by an insignificant amount (the probability of storage when the drum is half full is 99%).

The counter scheme described below was accepted for use in AN/FSQ-7 because it uses fewer cathodes and because the magnetic cores (metallic ribbon) as used in such a system have been tested sufficiently so that it appears they will work reliably (1100 cores are required for the system at one AN/FSQ-7 Central. 29 cathodes and 99 diodes per phone line are required with this system while an alternative vacuum tube system requires 46 cathodes and 126 diodes per phone line). The counter scheme works as follows:

> A core stepping register is used for each counter and a "1" is added to this counter when necessary by stepping the register through a serial adder circuit which uses no vacuum tubes but only cores (for simplicity in other parts of the circuit the complement of the required number is used and "1" is subtracted at each count). The core stepping register uses a delay line transfer circuit from core to core and requires one core per digit of the register. All steps of the counter system are synchronized with the drum because this requires only one synchronizer, which is used to synchronize the range signal coming from the SDV demodulator. This synchronizer also controls the number of pulses going to the stepping registers and an auxiliary stepping register is used to indicate when the proper number of pulses have occurred. If a target is indicated by the demodulator the counter is stepped into a readout core stepping register while it is stepped through the adder circuit. This means that the readout core register will contain the number which was held in the counter before the "1" was added in. The readout register is not disturbed until the next target appears even though the counter stepping register will have "1" added to it whenever a range mark occurs. A "drum demand" pulse reads the readout core register by pulsing it sharply into the "set" condition which results in strong readout pulses going to an open-line bus system running to the drum input register (a vacuum tube register). The "drum demand" pulse senses all counters "simultaneously" in a circuit which is similar to a high speed carry line. Thus, the first set of counters which is ready is read to the drum and other counters which are ready must wait for other "drum demand" pulses. The probability of storing the last set of counters in this circuit is about 99% when the drum is half full.

Dave Brown and other people connected with memory cores are to be consulted to see if there are any cores that they know about which are particularly suited to this application.

The cores should be wound with #39 wire or larger. Some attempt has been made by IBM to pot the cores but a few problems remain to be solved before this can be done without adverse effect on core performance.

IBM Report IM23 discusses basic stepping registers and includes information on the way diodes are used. More discussion is needed on the diodes but some people feel that they are used in a satisfactory way.

The margins on these circuits appear to be quite good. Perhaps the margins should be increased by running the system at 65KC instead of at 100KC because this will only slightly decrease the probability of storing information on the drum.

The pulse-lengths for pulses in this part of the system have not been decided. It was generally agreed, however, that the entire system should have as few different pulse lengths as possible. The high speed part of the machine will in general use 1/10 microsecond pulses.

Signed A.P. Kromer
A.P. Kromer

R.P. Mayer
R.P. Mayer

RPM/APK:jrt