Jack I. Raffel
August 31, 1953

ELECTRICAL ENGINEERING DEPARTMENT
MASTER'S THESIS PROPOSAL

TITLE: A Large Planar Switch For Register Selection In A Magnetic-core Memory.

STATEMENT OF THE PROBLEM

The purpose of this thesis is to evaluate a proposed selection scheme for a magnetic-core memory and to compare it with that presently used at the MIT Digital Computer Laboratory.

HISTORY OF THE PROBLEM

The three-dimensional magnetic-core memory was first proposed by J. W. Forrester.[1] The fabrication and successful operation of a 1024-register memory of 17-digit word length in the Memory Test Computer has demonstrated that this is a compact, reliable, rapid-access device for the large-scale storage of information.

The ability of a magnetic core to store information depends upon its having two stable remanent-flux states of opposite polarity. These two flux states can be arbitrarily identified as ONE and ZERO. The memory cycle consists of reading out of a single register the information it holds and then writing information into the register. The present scheme used at the Digital Computer Laboratory at MIT uses a three-dimensional selection system in which mutually perpendicular X, Y, and Z plane windings thread the matrix.[2]

Figure 1 shows a hysteresis loop for a memory core. Excitation of $\frac{Im}{2}$ on an X plane and a Y plane selects a single register at the intersection of these planes by providing it with Im, or current sufficient to switch the core. Inhibiting on a Z plane winding with $\frac{-Im}{2}$ then provides for digit selection.

Each digit plane has its own sense winding in addition to a Z winding. The readout of information is accomplished by picking up and amplifying the induced voltage due to the change of flux of a core switching. Discrimination between a ZERO and a ONE depends upon the large difference in induced voltage between a core driven from the bottom to the top of its loop and one that is merely driven out further into saturation.

The readout problem is complicated by the fact that there are a number of unwanted voltages induced on the sense winding in addition to the selected core output. These are of two main types: 1) register-select noise which may

come from half-selected cores in the X and the Y planes corresponding to the address of the selected core and 2) both capacitive and inductive coupling directly from the driving lines.

The problem of selection in a magnetic-core memory has been studied extensively[3,4] and many systems proposed which lead to higher selection ratios but which, in general, require more associated equipment than is used at present.

PROPOSED SYSTEM

In the present system, register selection takes place within the memory. The system to be investigated in this thesis would have register selection performed completely external to the memory. This was actually the first considered by Forrester[1], but requires an input for each register. If these were supplied directly from vacuum tubes their number would become prohibitive. An alternative would be to use a switching device with as many outputs as registers. The outputs from this switch must be capable of driving memory cores. Figure 2 shows a sketch of the proposed scheme.

A magnetic-matrix switch[5] is one possibility except that the large size needed would make it impractical. The switch plane can consist of a matrix of square-loop cores with a common bias winding supplying -B amp-turns.[6] This holds all the cores initially in the lower flux state represented on the hysteresis loop of Figure 3 as point a. A single core can be selected by driving with D/2 amp-turns on an X and the same on a Y line, provided D/2-B does not drive past the knee of the curve and D-B is capable of switching the core completely. Each secondary from the switch can now be used to drive a register of memory cores.

Writing is accomplished by driving the entire register with enough current to switch the core (Im), and inhibiting on the digit plane winding with a half-select pulse $\frac{(Im)}{2}$. This prevents the writing of ONES in those digits in which ZEROS are to be stored, but does not destroy information in the rest of the plane. (On the readout there are no restrictions on amplitude of the driving pulse.)

The possible advantages of this type of scheme are:

1. Reduction of register-select noise.
2. Simpler memory construction.
3. Faster and larger readout signals.

4. Possibility of favorable transformation of impedance seen by vacuum-tube drivers.

5. Reduction in number of drivers from 4n to 2n +1 for an n x n memory.

PROCEDURE

The thesis investigation will be divided into the following parts:

a) Design and Construction of Planar Switch

A single switch core will be tested, while driving memory cores to determine driving current requirements, core loss, and output current wave form. An attempt will be made to analyze the outputs from half-selected cores in the switch and to minimize their effect on the overall system. Among factors to be determined are: number of primary and secondary turns, core material and dimensions, wiring geometry, primary excitation, and secondary impedance.

b) Switch Driving Memory

Significant portions of a memory of fairly large size (16 x 16 x 32) driven by a switch will be built and the necessary logic assembled to test the memory under simulated operating conditions. Data will be taken for various modes of operation.

c) Evaluation of System

The system will be evaluated by comparing results with those obtained with the present memory system. This comparison will consider operating margins, tube count, complexity of construction and cycle-time.

EQUIPMENT NEEDS

All necessary equipment is available at the MIT Digital Computer Laboratory. Standard pulse equipment will be used and laboratory facilities will be available for the construction of any special units that may be needed during the course of this thesis.

Both switch cores and memory cores will be supplied by Group 63 of Division VI, Project Lincoln.

ESTIMATED DIVISION OF TIME

1.	Preparation of Proposal.	50 hours
2.	Further Study of Literature.	25 hours
3.	Experimental Work and Analysis	150 hours
4.	Correlation of Results and Formulation of Conclusions	100 hours
5.	Preparation of Thesis Report	75 hours
6.	Total.	400 hours

SIGNED: Jack Raffel
Jack I. Raffel

DATE: August 31, 1953

JIR:tl

SUPERVISION AGREEMENT

The problem described herein seems adequate for a Master's thesis. The undersigned agrees to supervise the research and evaluate the thesis.

SIGNED: David R. Brown
David R. Brown
DDL Staff Member

BIBLIOGRAPHY

1. Forrester, J. W., "Digital Information Storage in Three Dimensions Using Magnetic Cores", Project Whirlwind Report R-187 (May 16, 1950), MIT Servomechanisms Laboratory.

2. Papian, William N., "A Coincident-Current Magnetic Memory Unit", Project Whirlwind Report R-192 (August 31, 1950), MIT Servomechanisms Laboratory.

3. Everett, R. R., "Selection Systems for Magnetic Core Storage", Engineering Note E-413 (August, 1951), MIT Servomechanisms Laboratory.

4. Haynes, M. K., "Multidimensional Magnetic Memory Selection Systems", Code 03.013.403 (August 19, 1952), International Business Machines Corporation, Poughkeepsie, New York.

5. Olsen, Kenneth H., "A Magnetic Matrix Switch and Its Incorporation Into A Coincident-Current Memory", Project Whirlwind Report R-211 (June 6, 1952), MIT Digital Computer Laboratory.

6. Olsen, Kenneth H., "A Linear Selection Magnetic Memory Using An Anti-Coincident Current Switch", Project Whirlwind Memorandum M-2110 (May 8, 1953), MIT Digital Computer Laboratory.

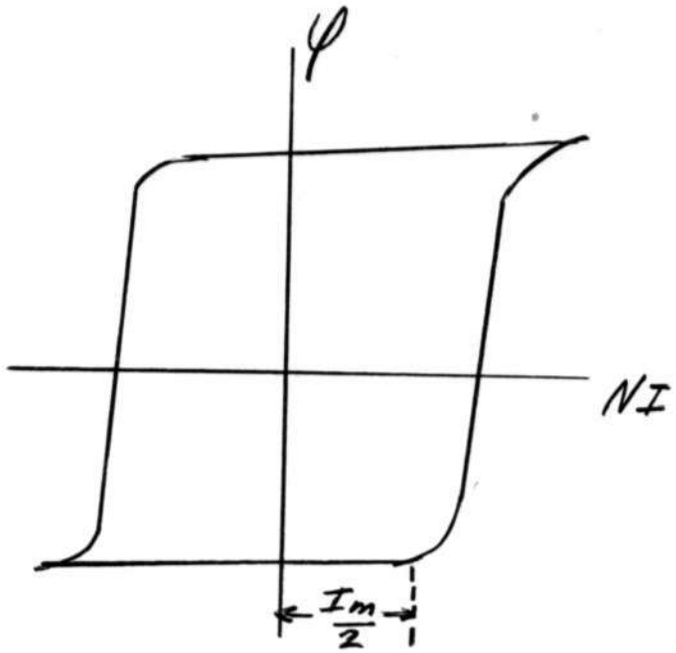

FIG. 1

HYSTERESIS LOOP OF MEMORY CORE

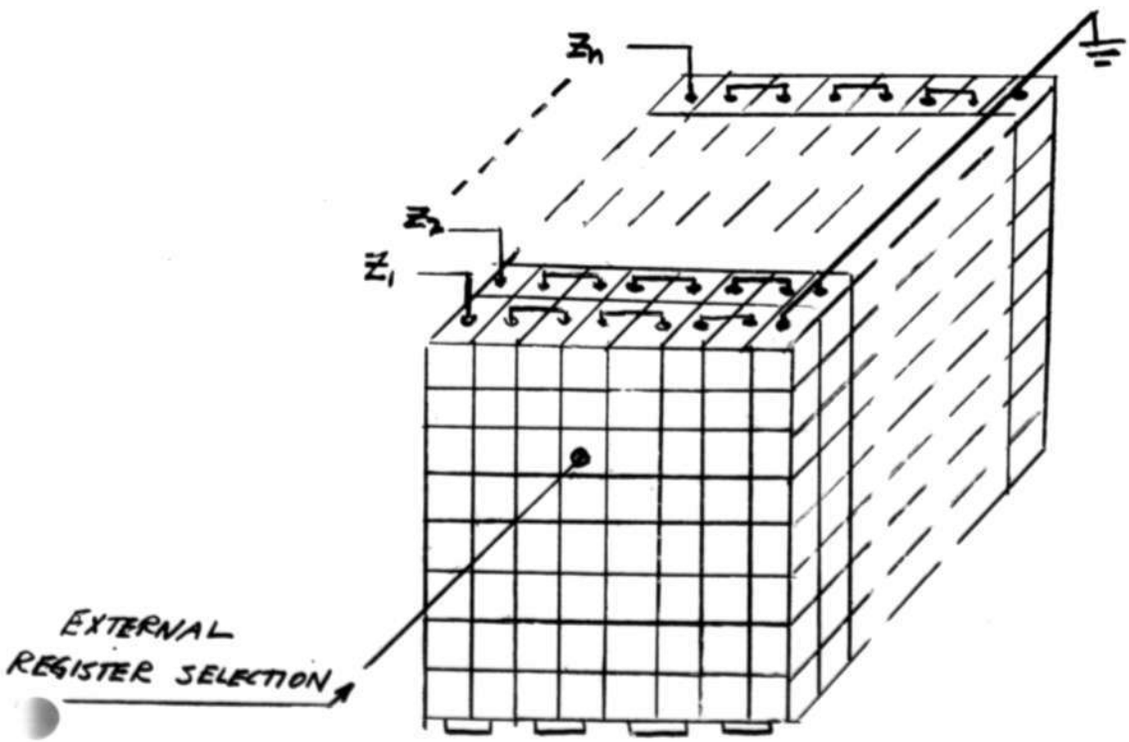

FIG 2

SCHEMATIC OF PROPOSED SELECTION SYSTEM

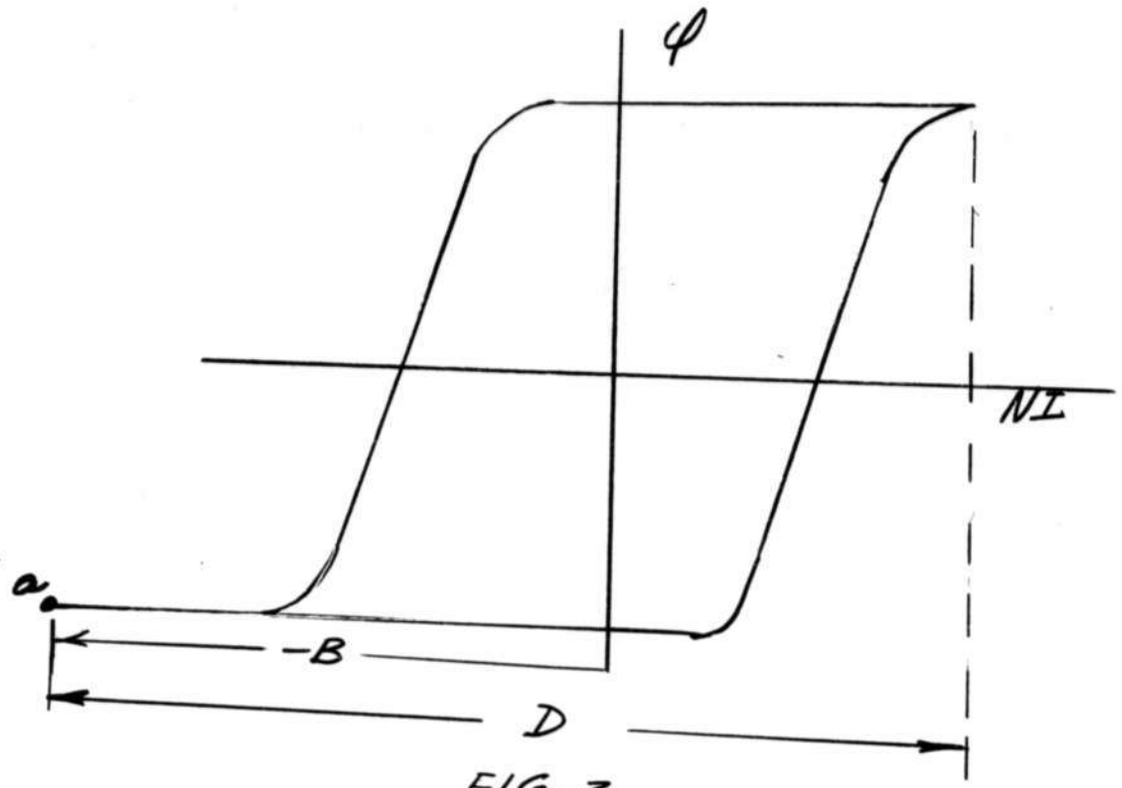

FIG. 3

OPERATING HYSTERISIS LOOP OF SWITCH CORE