Digital Computer Laboratory
Massachusetts Institute of Technology
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Subject: WWII Memory Address Selection System, PB No. 61

To: N. H. Taylor

From: N. Edwards and W. N. Papian

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This note is meant to satisfy item 1 (General Description of Function Needed) of the WWII Time Schedule for this subject.

The Memory Address Selection System takes the 24 outputs from the Memory Address Register (12 flip-flops) and, at a time determined by the computer, either reads from or writes into the selected memory register. The attached block diagram illustrates this function, yet is sufficiently general that it allows for the important decisions to be made, such as: will the decoders be diode or core matrices? will the drivers be vacuum tubes? with or without transformers? or will an "Olsen switch" do both the decoding and the driving?

The two units labelled Memory Address Decoder and Selection Plane Drivers are required to convert from the flip-flop base 2 to the Selection Plane base 64. Upon receipt of the Read gate from the Gate Generator, they must deliver to both the selected X plane and Y plane a rectangular current pulse (probably 1/2 ampere high and of 1 1/2 μsecond duration) of Read polarity. This is to be followed by the opposite, Write, polarity.

Cross reference on related work is made to PB Nos. 18, 62, 63, 64, and 65.

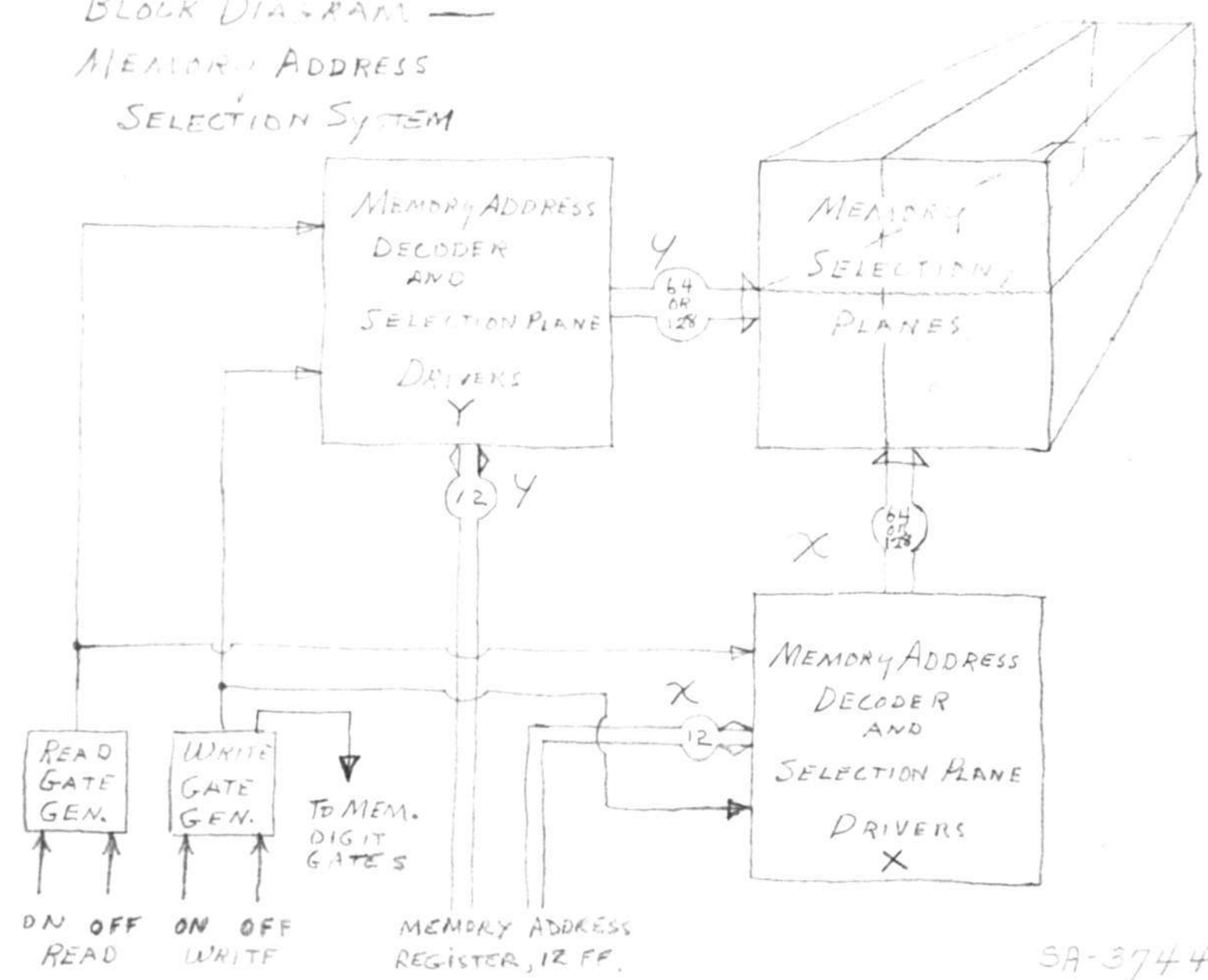
Signed NE
N. Edwards

Signed WNP
W. Papian

Approved
N. Taylor

WNP:NE/bs
Drawing attached: SA-37440

BLOCK DIAGRAM —
MEMORY ADDRESS
SELECTION SYSTEM



SA-37440

4/7/53 NE, WMP