Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II BLOCK DIAGRAMS MEETING OF APRIL 8, 1952

To: Whirlwind II Planning Group

From: W. A. Hosier

Abstract: This note abstracts the discussion of the meeting attended by the following persons, for the benefit of any who may wish to trace the course of thought on the subject.

G. R. Briggs	W. A. Hosier	N. H. Taylor
D. R. Brown	J. Jacobs	R. P. Mayer
D. A. Buck	R. C. Jeffrey	
R. R. Everett	W. Ogden	
J. W. Forrester	I. Reed	

In view of pressure from Air Defense agencies to have a prototype WWII computer operating by about the end of 1954, and of an estimated year's time necessary to assemble and test it after completion of detailed plans, it seems that some fundamental preliminary decisions need to be made on the logical plan of the machine by, say, July 1 of this year. To this end, we require

(a) as complete a survey as possible of the logical designs open to us, and of components whose performance is now known or at least predictable; and

(b) if possible an acceptable quantitative means of evaluating and comparing proposed designs - some sort of "figure of merit", as it were, to aid us in coming to a decision.

Meetings will be held twice weekly during this and the succeeding months to try to achieve such goals.

Besides the group's experience with WWI, other computer designs are familiar to individuals in it:

W. Ogden:	ERA 1101
I. Reed:	CADAC
D. Brown:	CALDIC
H. Grosch:	IBM 604

Certain more or less obvious general attributes of machines were pointed out - i.e., speed, traffic-handling capacity, reliability, and cost, together with some rough relationships among them.

More specific questions were also raised:

1. Shall effort be made to incorporate the non-destructive read-out from magnetic storage (originally proposed in D. Buck's report E-454 and discussed in M-1436) - and if so, into what parts of the system?

Among the considerations bearing on this are:

(a) How much time does it really save over rewriting? D. Buck mentioned that he has observed read-outs of this type requiring only 5% of the core's switching time, and thinks this is a reasonable figure to use in general - but the realizable gain in speed will of course depend on other things such as delays in the circuits energized by read-out pulses, and the proportion of operating time taken up by read-out operations. Reference was made to a report (M-1325) by D. R. Israel on what would be gained in WWI if storage access were instantaneous.

(b) What does the increased complexity of non-destructive read-out cost, both in dollars and in reliability?

(c) Are there logical systems, such as the use of two parallel banks of storage, which would compensate for time lost in the customary destructive read-out? Would the double storage scheme put too great demands on the programmer?

2. Is the magnetic stepping-register a device to be preferred for control purposes over other schemes such as the time-pulse distributor and control matrix? The assumption that such a register could be made large enough to handle driving power for most operational channels without amplification brings up another basic question:

3. Should the general policy be to replace several small circuit elements (principally vacuum tubes) with one large one wherever possible? N. Taylor said that information available from WWI does not altogether indicate that the answer to this question is an unqualified "yes" - citing the fact that WWI has had trouble with gassy 829's, and commenting that one important factor may be current density at the surface of cathodes. He suggested that no tubes be used with envelopes smaller than 5/8", and preferably nothing under 7/8". J. Forrester commented that intermittent defects such as short circuits and open welds were less likely with large tubes.

In connection with the matter of components capable of handling large amounts of power, Mr. Forrester quoted Vice-President Metcalf of General Electric as saying that General Electric is developing germanium diodes capable of handling currents of the order of 500 amperes.

4. Is it desirable to employ a common bus of the sort used in WWI?

N. Taylor pointed out that electronic registers with single-source inputs and single-destination outputs are relatively simple compared to registers with sufficient gate tubes necessary to permit their use in a bus system.

Dave Brown described briefly the computer which he had helped design for the University of California, which, he pointed out, used the same basic logic as Whirlwind I, simplified as much as possible in the interests of economy. This machine is a serial decimal machine with no bus, each decimal digit being represented in simple binary form. One feature of the machine to which he thought it worthwhile to call attention is its program timing: a cycle of only 4 clock pulses as compared to WWI's 8. R. Everett pointed out that the 8 time pulses in WWI were decided on principally to allow checking. The University of California computer as described by Brown employed a program counter; I. Reed suggested that this could be dispensed with if one were to employ time sharing of some of the other registers and a storage register.

The remainder of the meeting was spent in an analysis of the single-register computer as described by R. Everett in his report (M-1319) - in particular, of the difficulty of executing the order ts in such a machine. It was generally agreed that whatever technique one employs to get around this difficulty, it amounts to adding another register; hence a 2-register machine would seem to be minimum.

R. Everett pointed out that "multiply" is the critical operation in a machine with a limited number of registers, since it requires retention of the largest number of intermediate results.

Mr. Reed mentioned the "tabula rasa" proposal advanced by designers of CADAC which involved breaking orders down into components of the most rudimentary sort and combining these rudimentary orders by sub-programs more or less permanently stored in the memory - a proposal analagous to R. Mayer's idea of putting the control matrix into the memory (see M-1397).

As a course of action to be pursued between this meeting and the following one on Thursday, April 10, it was suggested that R. Mayer and R. Jeffrey review the analysis they have done of the 1 and 2 register computer, going through some of the more important orders for the purpose of determining how long and involved is the process of executing these orders in machines of this type. Mr. Forrester stressed the importance of actually getting a tentative block diagram on paper so that concrete proposals could be dissected and modified or rejected in the course of future meetings.

SIGNED W. A. Hosier
W. A. Hosier

A. H. Taylor

WAH/cp