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Digital Computer Laboratory
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Cambridge, Massachusetts

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SUBJECT: WHIRLWIND II MEETING OF JUNE 13, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and R. P. Mayer

Date: August 8, 1952

Members

- | | | | |
|----------|-------------|-------------|---------------|
| Present: | I. Aronson | A. Heineck | R. Pacl |
| | R. Best | W. Hosier | W. Papian |
| | G. Briggs | J. Jacobs | H. Rising |
| | D. Brown | R. Jeffrey | G. Sandy |
| | R. Callahan | A. Katz | R. Sims |
| | S. Dodd | W. Klein | N. Taylor |
| | D. Eckl | W. Linvill | R. von Buelow |
| | R. Everett | R. Mayer | B. Widrowitz |
| | R. Gerhardt | J. McCusker | R. Wieser |
| | A. Guditz | W. Ogden | J. Woolf |
| | | K. Olsen | |

Readers should remember that some details may have changed between June 13th and August 8th.

The first half of the meeting consisted of a report by D. Eckl on transistor circuits. A transistor adder was being built and worked on; the circuit was not yet finished, but each of four digits was completed to the extent shown in Figure 1. The lower flip-flop represents the A-register, and the upper flip-flop represents the partial-sum register. The carry register was not yet built. Electronic details of the flip-flop and gate circuits are shown in Figures 2 and 3, respectively. Notice that the flip-flop circuit contains six diodes and two transistors. It may be possible to eliminate four of

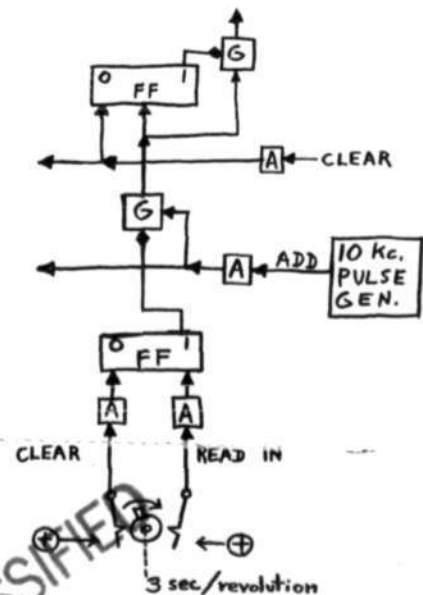


Fig. 1.

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these crystals if faster and more uniform transistors become available. Notice that the gate circuit input is forced negative as soon as the transistor fires. This makes it difficult to couple together several gate circuits on the output of the driving pulse source. This difficulty can be avoided by using the transformer and crystal circuit shown.

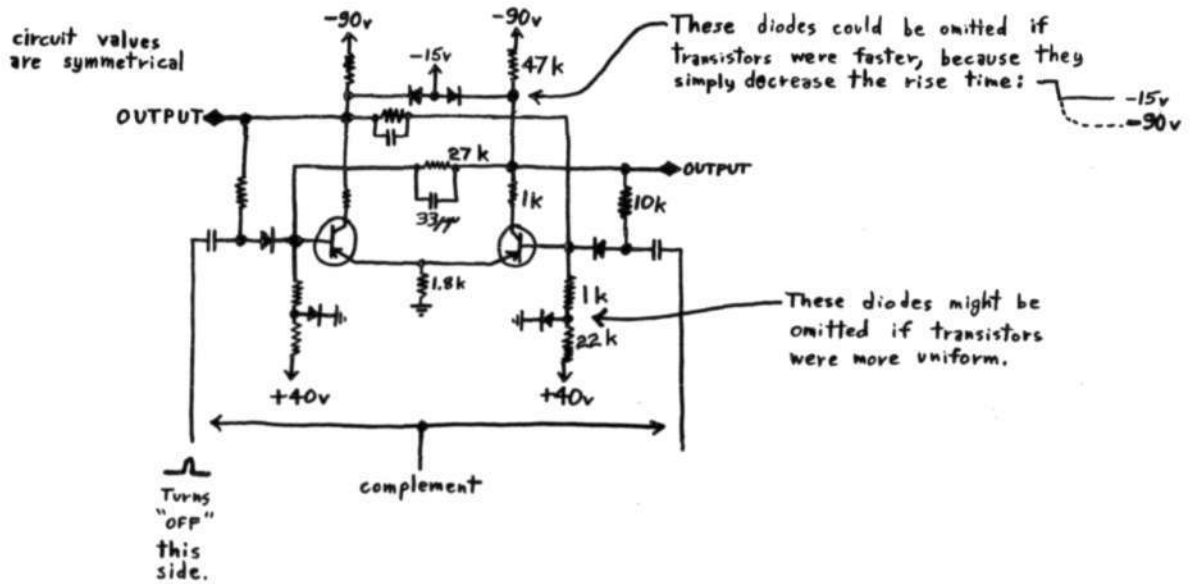


FIGURE 2. FF CIRCUIT

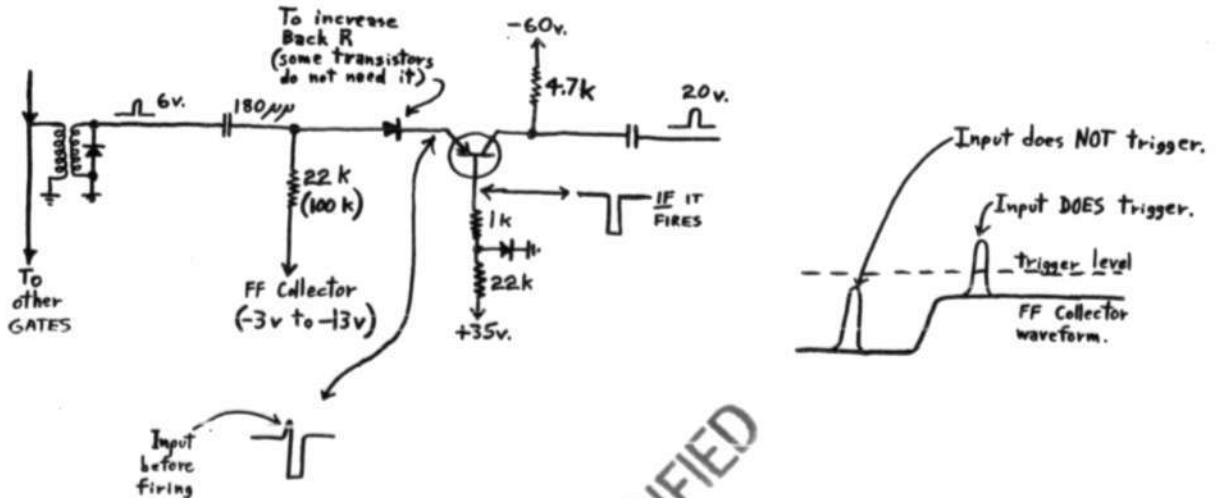


FIGURE 3 GATE CIRCUIT

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The main problem so far seems to be to get transistors and to get them uniform enough to work in standardized circuits. A recent shipment of RCA transistors contained eight out of twelve transistors which would work in standardized circuits.

Some of the characteristics claimed for Bell Labs' transistors are as follows:

Within 20% of specifications.
Extrapolated life greater than 70,000 hours.
Operation at vibrations greater than 100 G.
Shock of 20,000 G without damage.
1 to 3 watts instantaneous output pulse from a 1693 transistor operated class C.

Results of our own tests indicate the following:

Flip-flops have been running at speeds ranging from 800 KC to 1.5 mc (Bell 1734). (The Bell 1734 has a rise time and fall time of 0.2 microseconds each, so that it probably can be made to run faster.)

DC input power of 300 mw for flip-flops and 350 mw for gates.

The gate has an unloaded rejection ratio of 40 to 1 and an output amplitude of 20 volts.

The flip-flop output waveform has a 10-volt swing, but this is deliberately made small in order to shorten the rise time. The flip-flop is deliberately made slightly sticky in order to avoid temperature problems. It was pointed out that noise pulses might be smaller if signal pulses were smaller.

The transistor group is also working on a dynamic flip-flop. The block schematic is shown in Figure 4.

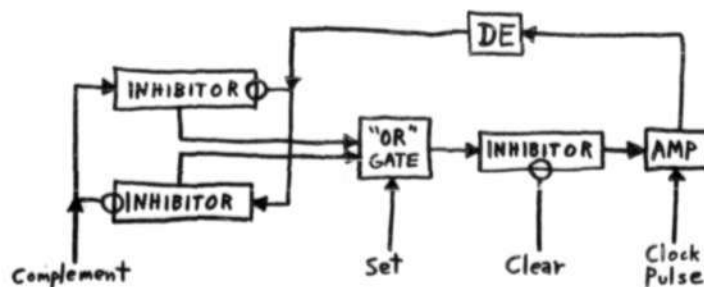


FIGURE 4. DYNAMIC FF

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The second half of the meeting on June 13th consisted of a report by W. Papian on the progress of the magnetic memory section. He first summarized the items of interest which had come up since the previous time he talked:

- (1) z axis installation and operation in the ceramic array.
- (2) Data on driving more cores in arrays.
- (3) Checking and alarm circuits.
- (4) Signal-to-noise ratios.

The z axis had been connected and was then undergoing tests which indicated that it is quite satisfactory. For a preliminary discussion of the z axis, see the notes of the April 25th meeting (M-1495). Briefly, the z axis refers to the operation of a digit plane driver for inhibiting the writing of a "1" whenever a "0" is desired. The access-time (including read and rewrite) is expected to be 4 microseconds for this type of operation, but the experiments allowed 5 to 6 microseconds for this.

Some experiments had been performed concerning the requirements for driving an array of cores. According to these experiments, the back voltage from a single core has a peak amplitude of 0.1 volts. One might speculate, then, that 2,000 cores would produce a back voltage of 200 volts (there are 2,048 cores in the 64-register by 32-digit plane of a 64 x 64 x 32 memory). In order to drive against this 200 volts, a 715 tube could be used with a 500-volt power supply. It was found that the back voltage from 256 cores had a peak amplitude of only 8 volts (0.03 volts per core) and that 512 cores produce a back voltage of 18 volts peak. The equivalent circuit of the 256-core array has a 2-microhenry inductance and a 1-ohm resistance. An equivalent circuit for a 4,000-core array was tested and indicated a back voltage of 60 volts (the waveshape, however, was different from the previous tests). No data had been collected on the delay-line effect, because the special probe for such tests was still under development.

A checking and alarm circuit has been designed and connected for use in checking the ferrite array. If a checkerboard pattern is stored in the array, then the flip-flop which controls the digits written into the array will be complemented between each write back into storage, so that a simple control flip-flop, which is automatically complemented, will contain the same information as the control flip-flop if the array is still operating properly. A simple circuit checks to make sure that they do agree, and if not, a bell rings, and the indexing of the selecting switch stops so that the faulty core is continuously displayed. This circuit allows marginal checking to be performed easily, and such a check showed 5 cores out of the 256 to be bad. One of these seemed to be very bad, and it was removed and given to the testing group, who confirmed this fact.

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The problem of signal-to-noise ratios is rather complicated. It concerns the different outputs on the sensing winding, which can be summarized as follows:

- (1) The desired signal from the selected core;
- (2) The signal from two "extra" cores;
- (3) $\sum \Delta_{ns}$ signal, to be described;
- (4) Signals due to different core characteristics;
- (5) Signals due to the difference between disturbed or undisturbed digits;
- (6) Special noise (outside noise);
- (7) Cross-talk (unbalanced air flux along the edges of the array).

The size of the array should have no serious effect on items 1, 2, and 6. Item 7 can be balanced out by running the sensing line around the edge of the array in the proper way. Items 3, 4, and 5 probably grow with the size of the array, probably in proportion to the square root of the number of registers.

Noises 2, 3, 4, and 5 come from non-selected cores. These non-selected signals are supposed to be canceled out by the geometry of the sensing winding, but this cancellation is never perfect for various reasons.

The $\sum \Delta_{ns}$ signal is of special interest. Figure 5 shows a hysteresis loop. The circled areas indicate that the slope of the line immediately to the right of the 0-current axis has a different slope depending on whether the core is storing a "0" or a "1". So $\Delta \phi_0$ for a non-selected core, is dependent on whether that core contains a "0" or a "1". Cancellation, therefore, cannot be exact if the two cores which are supposed to cancel do not both contain "0's" or both contain "1's". The resultant non-selected signal will be the difference between $\Delta \phi_0$ and $\Delta \phi_1$, which we can designate as Δ_{ns} . It is conceivable that a disturbed "0" occupies a portion of the hysteresis loop which happens to be parallel with that of a disturbed "1", but this possibility will have to be investigated

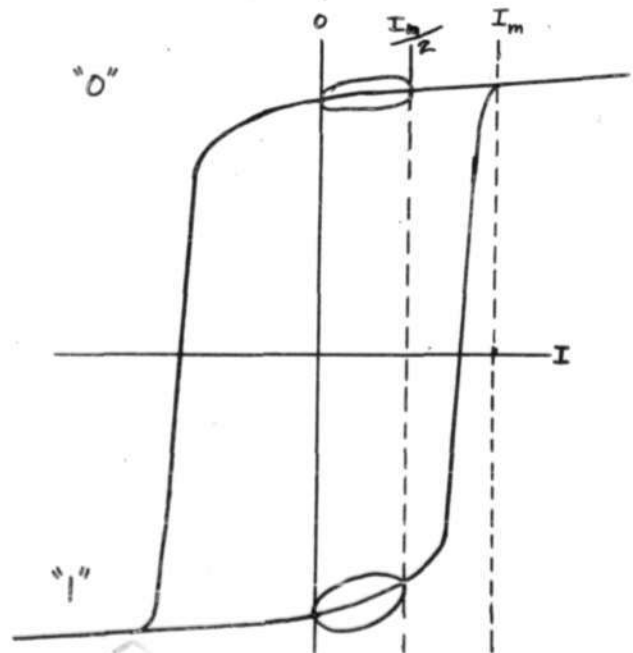


FIG. 5

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further, since the data on the present arrays are probably nullified by the fact that the cores themselves are not uniform. The existence of this problem indicates an explicit characteristic which we should specify to manufacturers.

If a larger array makes it more difficult for the undesirable signals to be canceled out, the array can be split into four or more sections, and the signals from each section can then be mixed together, or, if necessary, the signals from the selected section can be gated into the output circuit.

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