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Memorandum M-1518

Digital Computer Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: WHIRLWIND II MEETING OF MAY 23, 1952

To: Whirlwind II Planning Group

From: N. H. Taylor and R. P. Mayer

Date: June 10, 1952

Members Present:

I. Aronson	A. Heineck	R. Nelson
P. Baltzer	W. Hosier	K. Olsen
R. Best	J. Jacobs	W. Papian
G. Briggs	R. Jeffrey	H. Rising
D. Brown	A. Katz	C. Schultz
R. Callahan	W. Klein	R. Sims
D. Eckl	W. Linvill	N. Taylor
J. Forrester	R. Mayer	R. von Buelow
R. Gerhardt	J. McCusker	B. Widrowitz
A. Guditz	J. Mitchell	J. Woolf

It was pointed out that all WWII meetings will be held in the Whittemore building from now on, as shown on the schedule that is being distributed.

If there are any people who would like to consider using tubes above their rated dissipation, they should look at the picture of an automobile tire which was demolished while being used above rated dissipation. This picture is available on the bulletin board of Building 2, Whittemore Building.

R. Nelson described the one-week training course which is now being started. Advanced courses will be given later by different groups of people in the project. The one-week course will be repeated each week for a number of weeks. Anyone who wants to take all or part of this course should see either his immediate supervisor or N. Taylor. People are welcome to sit in a second time on any lectures which they feel they did not understand. No formal registration is required for these repeated lectures, and no prejudice will be held against people who repeat.

After the above miscellaneous news items were completed, the new organization for the WWII effort was described. Four engineering sections are being set up for designing the memory (headed by W. Papian), the control (no head yet), the arithmetic element (headed by J. Jacobs), and the terminal equipment (head not yet chosen). In addition, a research-and-development section (head not yet chosen) will continue to work on general problems associated with all phases of WWII. The control section will include the systems section and will be responsible for tying all of the sections together. The logical design section will be split up, with one member assigned to each of the four engineering sections.

The rest of the meeting was spent in discussing WWIA. Most of this discussion involved the purposes of WWIA and methods of building it.

The functions of WWIA will be to indicate what circuits are likely to give trouble, to provide life tests, to determine the reliability of various components, to find out whether tubes or transistors should be used, etc. To a large extent, these purposes can be fulfilled by exhaustive tests on small sections of the total system. However, isolated tests in racks are not sufficient because new problems of reliability and stability will probably be introduced when the equipment is assembled into a system. It is possible to interconnect equipment as it becomes available and perform a running life test on the growing assembly. However, it is difficult to evaluate the history of components in such a varying system. Instead, we should build a functioning machine, set it off in a corner, let it run, and see what happens. Only in this way can we feel a little more confident that all of the pieces will fit and work together as a system without the necessity of locating and correcting major difficulties which could arise only in an interconnected system.

The three major problems in designing a memory are:

1) Driving the cores, which involves both the length of the register and the number of registers involved;

2) Deterioration under use (reliability);

3) Output signals versus noise and interaction.

As far as the driving problem is concerned, we should use tube drivers because they: will give us experience with the memory system; will indicate whether core drivers will be practical to use; will give us information which will allow us to design core drivers. The deterioration problem can be investigated by the use of a small array, but this is already under investigation. We will not get very many useful answers to the third problem by using small arrays unless there is a gap of about a year before larger arrays are available.

If the model is to be small enough so that it doesn't become the final computer, it will not provide solutions to the driving and signal problems which will arise in building long register lengths and a large number of registers. It would seem desirable, therefore, to work simultaneously on a large memory for exhaustive tests and on a small memory for the functioning prototype. The small memory could be designed so that it would check both the problem of long register length and that of a 64 x 64 selection scheme without the necessity for building a 64 x 64 x 32-bit memory.

We are going to have to solve the problem of the large 64 x 64 array eventually anyway, so that perhaps we should start this investigation now. We can decide later to build an 8 x 8 memory if it looks as though building the 64 x 64 will be too difficult. For a functioning computer, small sections of the 64 x 64 array might be used.

For running components in an interconnected system to test only the memory, only a few digit columns and a few pieces of control equipment are needed (using a simple cp technique). For testing other electronic components, a larger memory may be required. It should be pointed out that we are testing only electronic techniques and not logical design nor a complete system when we are using a simple prototype computer.

A date should be set for reviewing the objectives of this WWIA effort.

Rollin P. Mayer
Rollin P. Mayer

Norman H. Taylor

RPM:NHT/bs