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SUBJECT: BINARY COUNTING WITH MAGNETIC CORES

To: N. H. Taylor

From: D. A. Buck

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Abstract: Magnetic materials suitable for multi-dimensional memories have recently become candidates for circuit elements in other parts of a digital computer. Their possible uses in binary counters and as pulse-operated gates are being considered.

A. INTRODUCTION

In a binary adder any one of the stages, except possibly the first and the last, must be prepared to interpret a combination of ONE's and ZERO's on three inputs and supply a ONE or ZERO to each of two outputs. Two of the inputs are the digits to be added and the third is the carry from the preceding stage; the outputs are the sum digit and the carry to the following stage. The relationship between the input combination of ONE's and ZERO's and the output combination of ONE's and ZERO's is the well known binary addition table. If a stage receives a carry from the preceding stage and at the same time transmits a carry to the following stage, it is said to "propagate" the carry, and the carry is thought of as passing through the stage. If a stage has no carry as an input but does have a carry as an output, it is said to "originate" a carry, and conversely, if a stage has a carry input but no carry output, it is then said to "block" the carry. These definitions will be used in the following discussion.

B. COUNTERS

Counting is a special case of addition in which one of the addends is always unity. In counting however, unlike in addition, only the least significant stage can originate a carry. All other stages either propagate or block a carry. The carry can be thought of as originating in the least significant stage and propagating up through the stages until it is blocked; having been blocked it cannot start again.

The carry can propagate through any number of stages in the counter from none to the maximum number. The carry propagates through no stages on alternate counts when unity is added to an even number and merely changes the least significant digit from ZERO to ONE, and the carry propagates through the maximum number of stages when the counter exceeds its modulus, or "overflows". The latter case in many ways subjects a given counter design to its most difficult operating conditions. The carry, as it propagates up the entire length of the counter, must maintain its amplitude and waveshape to an extent that will allow it to accomplish its addition function at each stage. In this case, also, the greatest amount of time is required for the carry to come to a stop so that the counter can be read. Since no knowledge of the count is assumed at the time of reading, the maximum carry propagation time must be allowed after each and every count.

The problem of making the carry propagate rapidly has been temporarily deemphasized here in view of the more fundamental problem of maintaining the amplitude and waveshape of the carry as it propagates. At present, it seems desirable that for all except very short counters the carry be amplified in some manner as it goes from stage to stage, and since it is hoped that the obvious expedient of putting a vacuum-tube amplifier between stages can somehow be avoided, a small-scale investigation of possible techniques of getting the carry up through the stages was undertaken. The progress to date will be briefly reported.

Counters are often divided into two categories: those in which the carry is regenerated by each stage as it flips over from ONE to ZERO, and those in which the carry propagates through gates which are controlled by the various stages. Logically the two are identical, especially when the regeneration by each stage of a counter of the first type is thought of as a gating action. The distinction, however, exists, and the counters in the first category are called "progressive-carry" counters while those in the second category are called "gated-carry" counters.

1. Progressive-carry Counters

In progressive-carry counters the carry, as it enters a stage, causes the stage to trigger, that is, to change to ONE if it contains ZERO or to ZERO if it contains ONE. In the latter case, in which the stage changes from ONE to ZERO, the carry is re-shaped and delivered to the following stage. This process continues up through the stages until the carry comes to a stage which already contains ZERO. This stage is changed from ZERO to ONE and the carry stops. The power gain of each stage is utilized in the re-shaping process so that the carry propagates without attenuation.

To date, magnetic-core counters in the progressive-carry category are restricted to those which use a high-frequency magnetic amplifier type of flip-flop. One stage of a counter representative of this class is shown in Figure 1. Developed by Computer Research Corporation, it was

preceded by a similar development by Engineering Research Associates. Robert Pfaff, a S.M. thesis student with the group, is at present investigating the possible use of a counter of this type in an application associated with the M.I.T. Servo Laboratory Milling Machine Project.

2. Gated-carry Counters

Gated-carry counters (Fig. 2) are those in which each stage of the counter operates a gate which controls the carry. Figure 2a illustrates one stage of a gated-carry counter in which, after a short delay, the flip-flop is triggered by the carry entering the stage. If the stage contains ONE, the carry has time before the flip-flop triggers to pass through a gate which is held open by the ONE-side of the flip-flop. If the stage, on the other hand, contains ZERO, the flip-flop is triggered, but by the time the gate on the ONE-side opens, the carry pulse, which is shorter than the delay, disappears and is not propagated to the following stage. Figure 2b illustrates one stage of a similar gated-carry counter in which the flip-flop need not be capable of triggering. Two gates instead of one, however, are required.

A scheme has been worked out (Fig. 3) to use pulse-operated magnetic cores in this latter configuration. This is actually a four-core stepping register arranged so that the output feeds back into the input. The logical operation will be described here, but the circuit design considerations will be covered in the section on pulse-operated magnetic gates. Magnetic cores numbered 1 and 3 are the flip-flop and cores 2 and 4 are the gates of the gated-carry counter. Among the four cores of a stage, there is but a single ONE and three ZERO's. The single ONE will always lie, when the counter is at rest, in either core number 1 or core number 3, the two cores of the flip-flop. If the ONE lies in core number 1, the flip-flop contains ZERO and if it lies in core number 3, the flip-flop contains ONE. The carry input pulse is made into two power pulses which are displaced in time one from the other by the delay. The first of these, power pulse I, drives the information from the odd-numbered cores into the even-numbered cores (flip-flop into gates), while the second, power pulse II, drives the information from the even-numbered cores into the odd-numbered cores (gates into flip-flop). The single ONE, then, will circulate around the loop of four cores once for every two carry input pulses. Each time it rounds the bend at core number 3, a carry is sent to the following stage. A carry can also be taken from core number 4 which will be delayed from the carry from core 3 so that the delay can be eliminated in all but the first stage, only amplification being needed in succeeding stages. The vacuum tube amplifiers shown could probably be eliminated for a very short counter, as already mentioned. A four-core stepping register of this design (minus carry output leads) was constructed by the group. Using ferrite cores, it was able to count at a rate exceeding 100 KC.

C. PULSE-OPERATED MAGNETIC GATE-AMPLIFIERS

At this point we depart from counters temporarily to investigate the possible use of pulse-operated magnetic cores to replace the vacuum-tubes as carry amplifiers and gates.

1. A Simple Coincidence Gate

One scheme which suggests itself is to apply a power pulse and a pulse to be amplified simultaneously through windings N_2 and N_1, of Fig. 4a, in such a way that the power pulse alone is not enough to switch the core but the combination of the two pulses will switch the core. As the core switches, the instantaneous power delivered by the power pulse is the product of the instantaneous voltage and the instantaneous current in winding N_2. Symbolically, $p_2 = e_2 i_2 = N_2 i_2 \frac{d\phi}{dt}$. Similarly, $p_1 = e_1 i_1 = N_1 i_1 \frac{d\phi}{dt}$ and the output power $p_3 = e_3 i_3 = N_3 i_3 \frac{d\phi}{dt}$. Since, during switching, the $\frac{d\phi}{dt}$ is common to all windings, the power going into each of the two driven windings is proportional to the ampere-turns of that winding, and since the power going into these driven windings must go somewhere, it goes into the load, supplying the output power. The requirement governing the ampere turns in the two driven windings is that their sum slightly exceed the knee of the hysteresis loop. The ratio of power-pulse ampere-turns, $N_2 i_2$, to the pulse-to-be-amplified ampere-turns, $N_1 i_1$, might be made arbitrarily large and therefore it would appear that the power gain is limited only by the degree to which the amplitude of the power pulse can be controlled.

When the hysteresis loss of the core is considered, however, the inability of the scheme to provide power gain is clearly seen. The hysteresis loss in the core, $\int H dB$, is the area of the hysteresis loop. As this gate operates, moving from one residual point on the hysteresis loop to the other, one half of the hysteresis loop area must be dissipated in the core. The power-pulse ampere-turns, $N_2 i_2$, can be thought of (Fig. 4b) as supplying a fraction of the hysteresis loss which is arbitrarily close to, but never greater than, unity. If the power pulse were to supply more than just the hysteresis loss, the core would switch on this pulse alone, thereby destroying the gating action of the core. The pulse to be amplified, then, supplies the rest of the hysteresis loss plus the power delivered to the load. Clearly, as in the case of a conventional transformer, there can be no power gain.

2. The Harvard Gate-Amplifier

A pulse-operated magnetic gate which <u>does</u> have a power gain (Fig. 4c) has been developed by the Harvard Computation Laboratory. In this scheme, the power pulse and the pulse to be amplified are <u>not</u> applied simultaneously, and they are each large enough to switch the core. The pulse to be amplified is first applied, switching the core from ZERO on

the top of the hysteresis loop, the core's rest state, to ONE on the bottom. When the pulse to be amplified is removed, the core is left at ONE on the bottom of the loop, where it will remain until the power pulse is applied. The power pulse, applied so as to produce flux in the opposite direction, switches the core back to ZERO, and the gate is once again in its rest position. The presence of the rectifier in the load circuit effectively removes the load when the pulse to be amplified switches the core but reconnects the load as the power pulse switches the core in the opposite direction. This allows the power pulse to supply power to the load as well as one-half of the B-H loop area, while the pulse to be amplified merely supplies the other half of the B-H loop area. If the pulse to be amplified is defined as the input to this core and the pulse delivered to the load is defined as the output, it can then be said that the core gives a power gain. Gating action is achieved by virtue of the fact that if a power pulse comes along without having been preceded by a pulse to be amplified, the core, which is already on the top of its hysteresis loop, will move from ZERO to "a" and back causing a negligible change in induction and therefore no pulse in the load. If it is assumed that at the time of a power pulse one does not know in which state the core lies, then there will or will not be a pulse in the load depending upon whether or not a pulse to be amplified came along. The pulse to be amplified, then, can be thought of as a gating pulse.

This gate, beside providing amplification, has the most desirable feature that neither the pulse to be amplified nor the power pulse need be measured pulses. They are only required to exceed a minimum value, above which they can have any value whatever.

An interesting feature of this gate is that only one pulse can pass for each gating pulse, a feature which might be used to advantage in an application such as a push-button pulse synchronizer in which an asynchronous pulse is used as the gating pulse and the first clock pulse to come along after the gating pulse is used as the power pulse. All subsequent clock pulses would merely drive the core from ZERO to "a" and back, the gate being "off". In this application, the gating pulse would have to be larger in ampere-turns than the power pulse so that it could overwhelm the power pulse in the event they coincided with one another in time.

This is the gate used in the magnetic stepping register and in the gated-carry counter already described. It has the obvious disadvantage that a time delay is required between input and output. If, in the gated-carry counter already described, this gate were used to replace the tubes used to amplify the carry between stages, a succession of these delays would be required in order that a carry propagate the entire length of the counter.

3. A Current-Biased Gate Amplifier

Still another magnetic-core gate has been developed which is turned off by a current through one of its windings (Fig. 5), in a way analagous to that in which a vacuum-tube is biased off by a negative voltage. A large m.m.f. due to the control current, i_2, will hold the core in a region where there is a negligible induction change for a given change in power-pulse m.m.f. In this region, the power pulses are effectively disconnected from the load since coupling is by changes in induction. Furthermore, there will be little voltage across the control winding, N_1, and the power winding, N_2, so that a negligible amount of power will be supplied by these circuits when the gate is "off". Removal of the control current, i_1, allows the core to move to its residual induction point on the bottom of the hysteresis loop and the gate is then said to be "on". If, when the gate is "on", a positive pulse followed by a negative pulse occurs in the power winding, N_2, the core will go around its hysteresis loop and the resulting induction change will deliver a positive and negative pulse to the load. The control circuit, delivering zero current, will absorb no power. Subsequent pairs of positive and negative pulses in the power winding, N_2, will deliver pulses to the load. These pairs can, in fact, be sine waves, if it is desired merely to couple power to the load, as would be the case if the load were a panel lamp in an indicator circuit. A variation is to have a single positive pulse which will act as in the gate previously described coupling a single pulse to the load and then no more until the gate is turned "off" and then "on" again.

This gate has been extended to a scheme in which a core can be biased off by any number of control windings, each of which acting alone is enough to hold the gate "off". K. Olsen has applied this to a multi-position switch in which the control windings on a number of cores are connected as a matrix so that all of the cores except one are biased off. This gating scheme is the basis for a "carry-matrix" type of gated-carry counter yet to be described.

L. A CARRY-MATRIX COUNTER

Taking advantage of the fact that the carry progresses through the stages of a counter, triggering each of them, until it comes to a stage containing ZERO which it triggers and then stops, we can use the gate just described to control the carry. Consider a matrix of magnetic cores (Fig. 6) in which there is one core whose responsibility it is to propagate the carry to each stage. These cores are connected as gates in such a way that a ZERO in any stage of the counter will bias off all of the gates leading to higher stages. This scheme involves the use of flip-flops which can be triggered. An extension of this (Fig. 7) uses two cores instead of one to propagate the carry to each stage. The

stage itself biases one of the two cores off. The output of one of the cores sets the flip-flop to ONE while the output of the other sets the flip-flop to ZERO. The whole thing is so arranged that if the flip-flop is ZERO it gets set to ONE or if it is ONE it gets set to ZERO, and therefore need not be capable of triggering.

This concludes the discussion of counters. It was felt that the informal appendix at this point is a useful way to introduce some of the design problems and techniques.

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APPROVED WNP
W. N. Papian

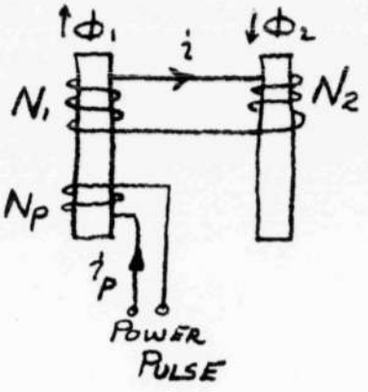
LAB/cp

Appendix I, Pages 8-10 (Drawings SA-50622-3-4)
Appendix II, Page 11 (Drawing SA-50625)
Drawings Attached:

Fig. 1 - Drawing No. SA-50617, Page 12
Fig. 2 - Drawing No. SA-50618, Page 13
Fig. 3 - Drawing No. SA-50619, Page 14
Fig. 4 - Drawing No. SA-50620, Page 15
Fig. 5 - Drawing No. SA-50621, Page 16
Fig. 6 - Drawing No. SA-50532 Page 17
Fig. 7 - Drawing No. SA-50561, Page 18

APPENDIX I

MAGNETIC CORE COUPLING



CONSIDER TWO IDENTICAL CORES SO ARRANGED THAT ONE DRIVES THE OTHER. ASSUME NO LEAKAGE FLUX. LET $\frac{\mu A}{\ell} = 1$ SO THAT $\phi = NI$

$$\phi_1 = N_p i_p - N_1 i$$

$$\phi_2 = N_2 i$$

SUBSTITUTING,

$$\phi_1 = N_p i_p - \frac{N_1}{N_2}\phi_2 \qquad (1)$$

WRITING A VOLTAGE-LOOP EQUATION,

$$N_1 \frac{d\phi_1}{dt} = N_2 \frac{d\phi_2}{dt}$$

ASSUME ϕ_1 AND ϕ_2 START FROM ZERO AT $t=0$. AT ANY TIME, T,

$$\int_0^T N_1 \frac{d\phi_1}{dt}\,dt = \int_0^T N_2 \frac{d\phi_2}{dt}\,dt$$

$$N_1 \phi_1 = N_2 \phi_2 \qquad (2)$$

SUBSTITUTING (2) INTO (1),

$$\phi_1 = N_p i_p - \frac{N_1^2}{N_2^2}\phi_1$$

$$\frac{N_2}{N_1}\phi_2 = N_p i_p - \frac{N_1}{N_2}\phi_2$$

THEREFORE,

$$N_p i_p = \phi_1\left(1 + \frac{N_1^2}{N_2^2}\right) = \phi_2\left(\frac{N_1^2 + N_2^2}{N_1 N_2}\right) \qquad (3)$$

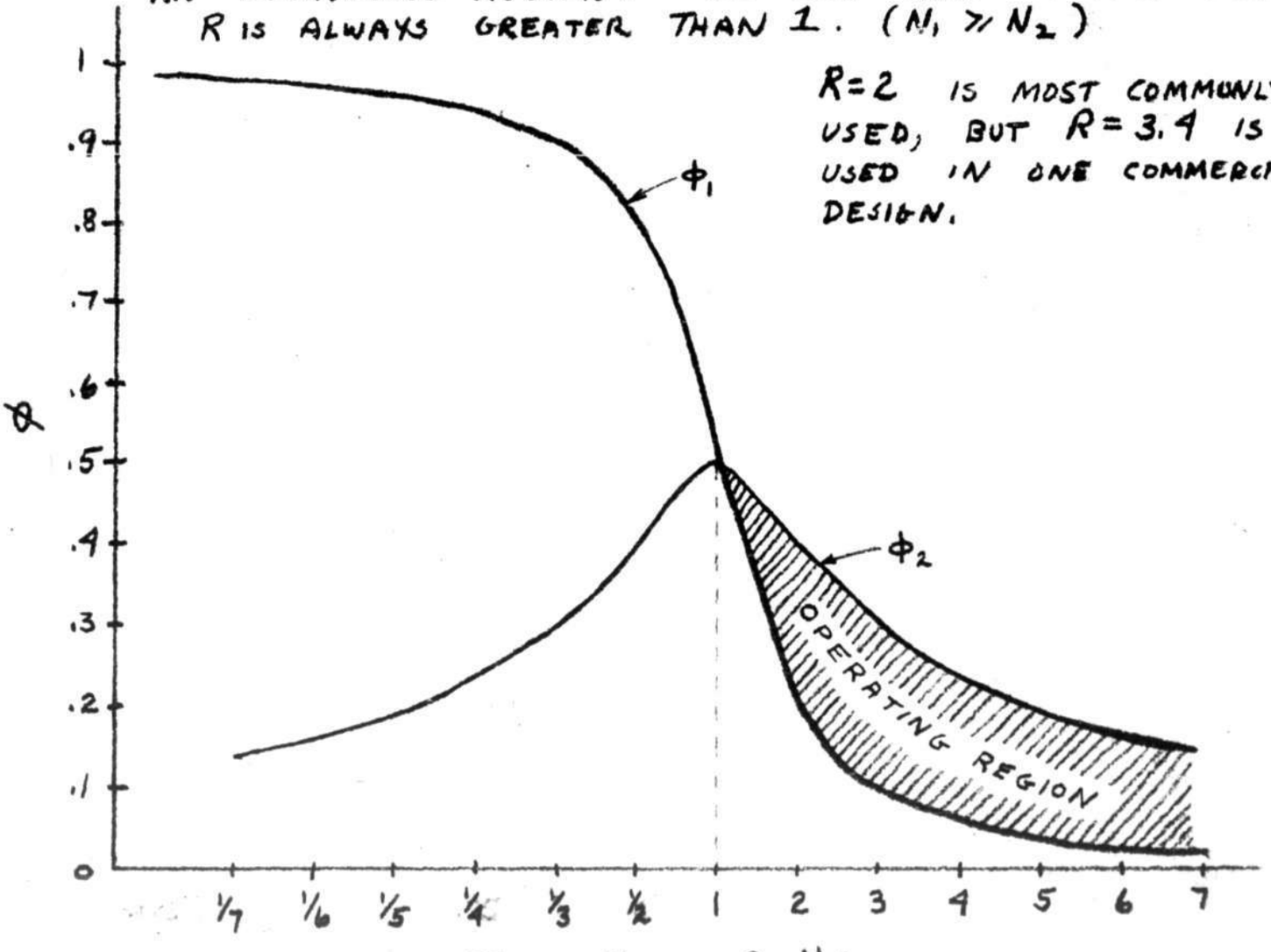
DEFINE TURNS RATIO $R \equiv N_1/N_2$

THEN

$$N_p i_p = \phi_1\left(1 + R^2\right) = \phi_2\left(R + \frac{1}{R}\right) \qquad (4)$$

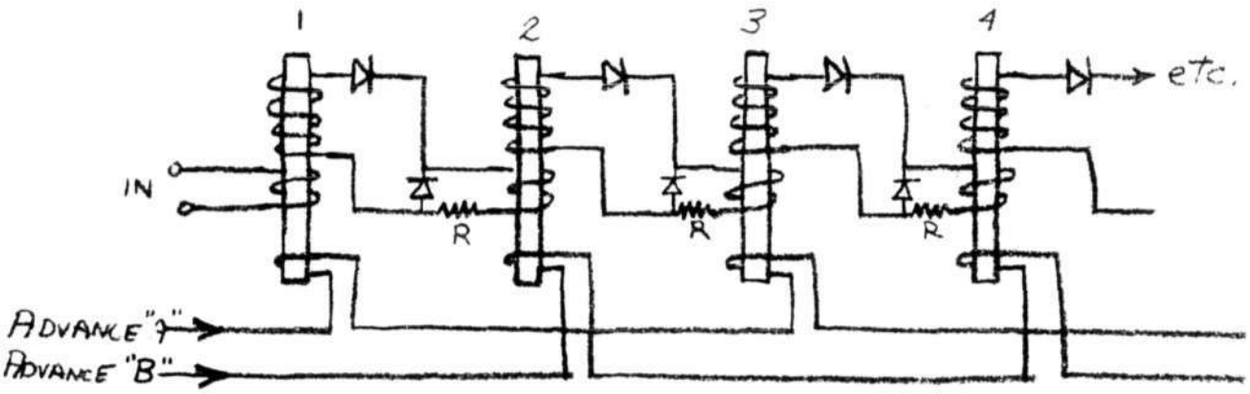
SM-50622

FOR A GIVEN $N_p i_p$, WE CAN PLOT VALUES OF ϕ_1 AND ϕ_2. BECAUSE ϕ_1 AND ϕ_2 ARE LIMITED BY SATURATION, ϕ_2 MUST EXCEED ϕ_1 IN THE REGION IN WHICH BOTH CORES ARE SWITCHING SO THAT CORE 2 WILL SWITCH BEFORE CORE 1. OTHERWISE CORE 2 WOULD NOT SWITCH COMPLETELY. WE CAN THUS DEFINE AN "OPERATING REGION". WE SEE THAT IN THIS REGION R IS ALWAYS GREATER THAN 1. ($N_1 \geq N_2$)



$R = 2$ IS MOST COMMONLY USED, BUT $R = 3.4$ IS USED IN ONE COMMERCIAL DESIGN.

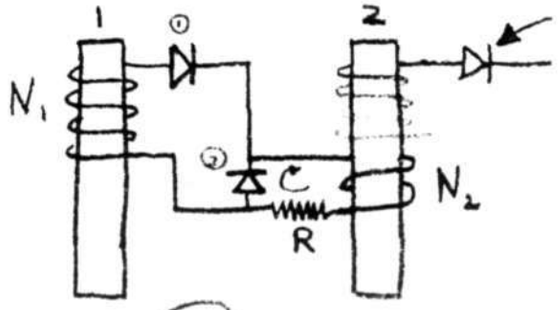
S.-50623



TYPICAL STEPPING REGISTER

ADVANCE "A" STEPS INFORMATION FROM ODD CORES TO EVEN CORES.
ADVANCE "B" STEPS INFORMATION FROM EVEN CORES TO ODD CORES.

COUPLING DETAILS

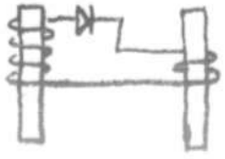


PRIME PURPOSE OF SERIES DIODE IS TO UNLOAD CORE 2 WHEN READING FROM CORE 1 TO CORE 2.

	N_1	N_2
HARVARD (ALDEN)	150	75
BURROUGHS	80	40
TRANSDUCER (CIRCUIT BELOW)	33	9

R IS USUALLY ≈ 15 Ω

CURRENT FLOWS AROUND COUPLING LOOP IN SAME DIRECTION DURING ADVANCE "A" AS ADVANCE "B". DIODE ② IN CONJUNCTION WITH THE RESISTOR PREVENTS BACKWARD FLOW OF CURRENT. ALSO HELPING PREVENT BACKWARD FLOW ARE CORE 1 B-H LOOP SHAPE AND DIODE ① NON-LINEAR FORWARD CHARACTERISTICS, PLUS TURNS RATIO. IN FACT, THESE LATTER THREE ARE ENOUGH TO DO THE JOB ALONE. ONE COMMERCIAL DESIGN:



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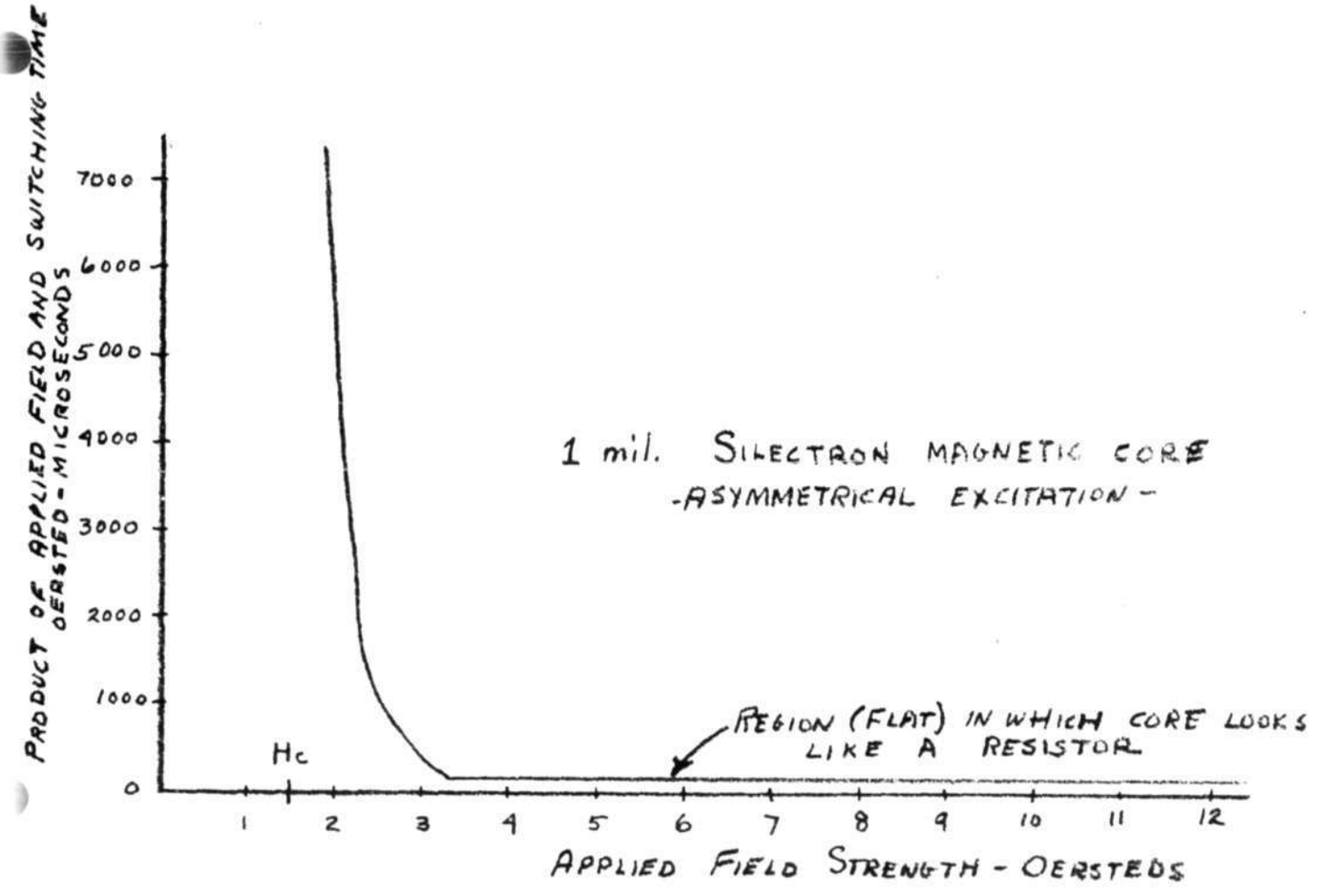
C

APPENDIX II



SANDS, OF BURROUGHS, HAS OBSERVED THAT FOR MOST METALLIC CORES THERE IS A RANGE IN THE APPLIED-FIELD VERSUS SWITCHING-TIME CURVE OVER WHICH THE PRODUCT OF THE TWO IS CONSTANT. DOUBLING THE DRIVING CURRENT THROUGH ITS WINDING PRODUCES TWICE THE APPLIED FIELD STRENGTH. THIS IN TURN CUTS THE SWITCHING TIME IN HALF DOUBLING $\frac{d\phi}{dt}$ AND THEREFORE DOUBLING THE VOLTAGE ACROSS THE WINDING, EXACTLY AS IF THE WINDING WERE A RESISTOR. SANDS GIVES:

$$R = \frac{\overbrace{1.26 \times 10^{-8}}^{\text{UNITS}} \; N^2 \; (B_r + B_m) \; A}{H \cdot t \cdot L}$$

N: TURNS; $(B_r + B_m)$: B-H LOOP HEIGHT (GAUSS); A: AREA - SQ. CM.

H: APPLIED FIELD OERSTEDS; t: TIME IN SECONDS; L: MEAN LENGTH MAGNETIC PATH CM.

SC-506625

TYPICAL R's:

ORTHONIK 1.1 mil. 1.85×10^{-2} OHMS/TURN^2

Mo-PERMALLOY .26 mil. 5.51×10^{-2} OHMS/TURN^2

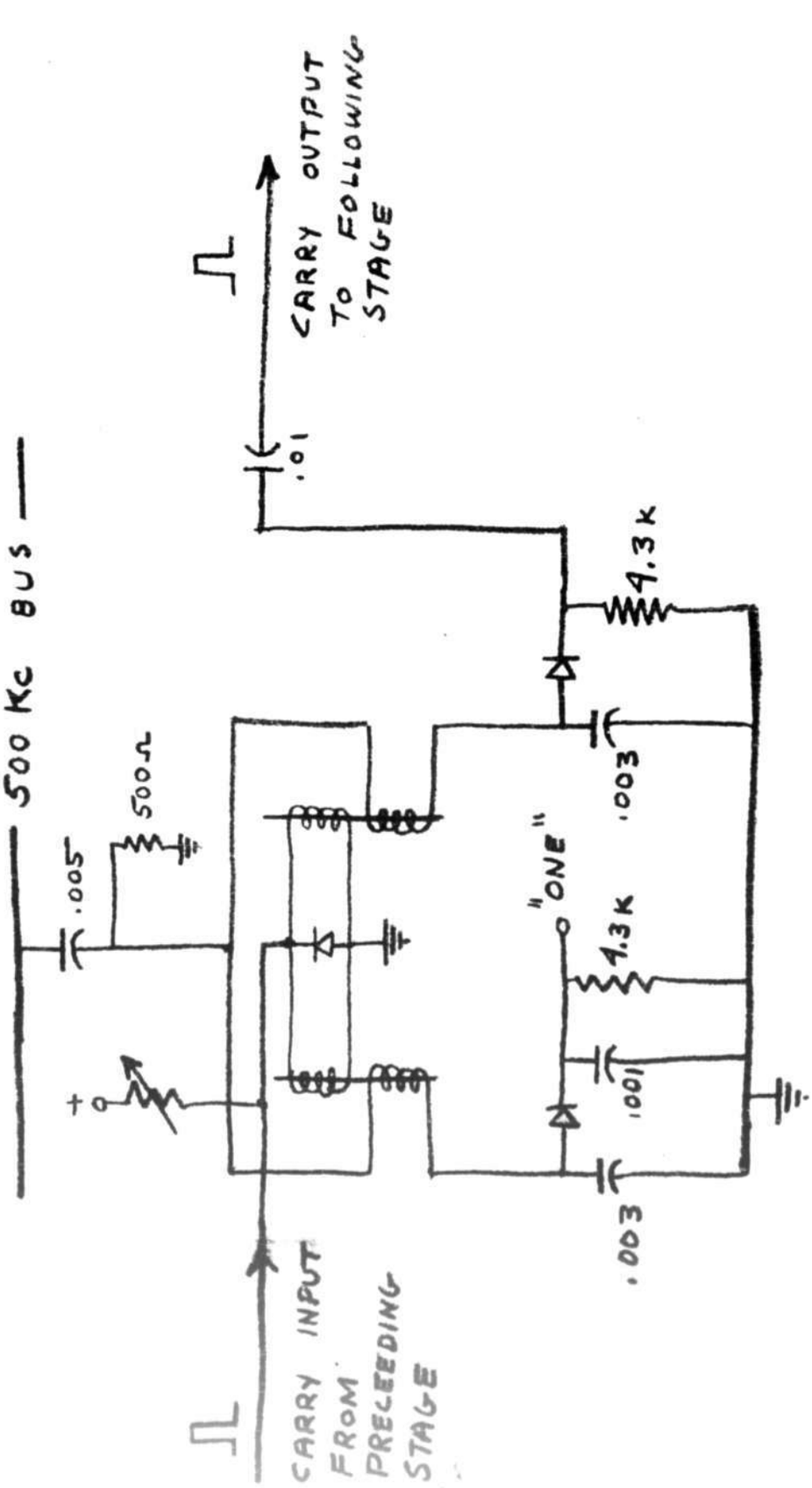
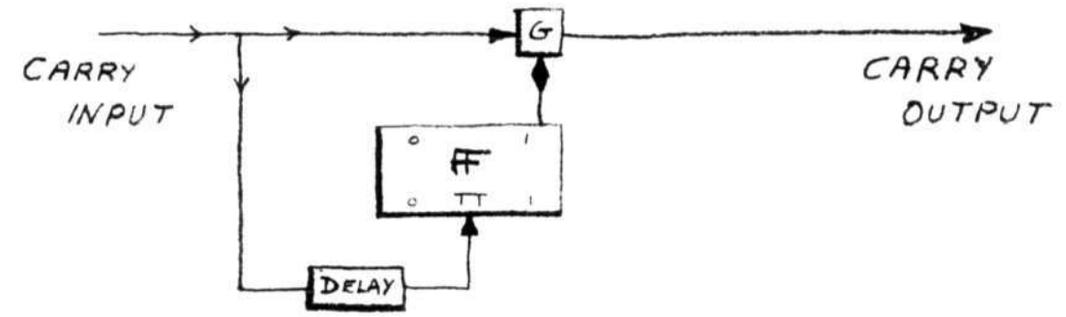
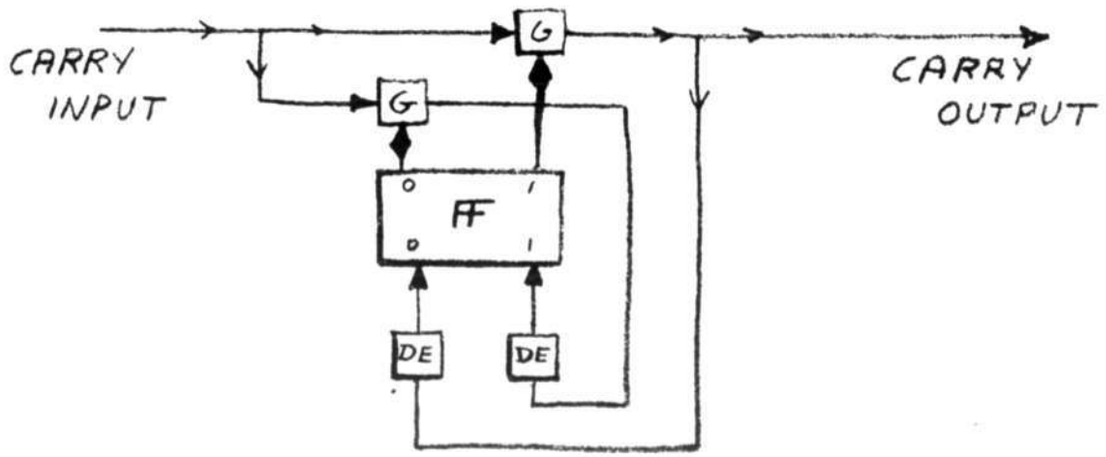


FIG. 1. COMPUTER RESEARCH CORP. COUNTER (ONE STAGE)

SF 50617



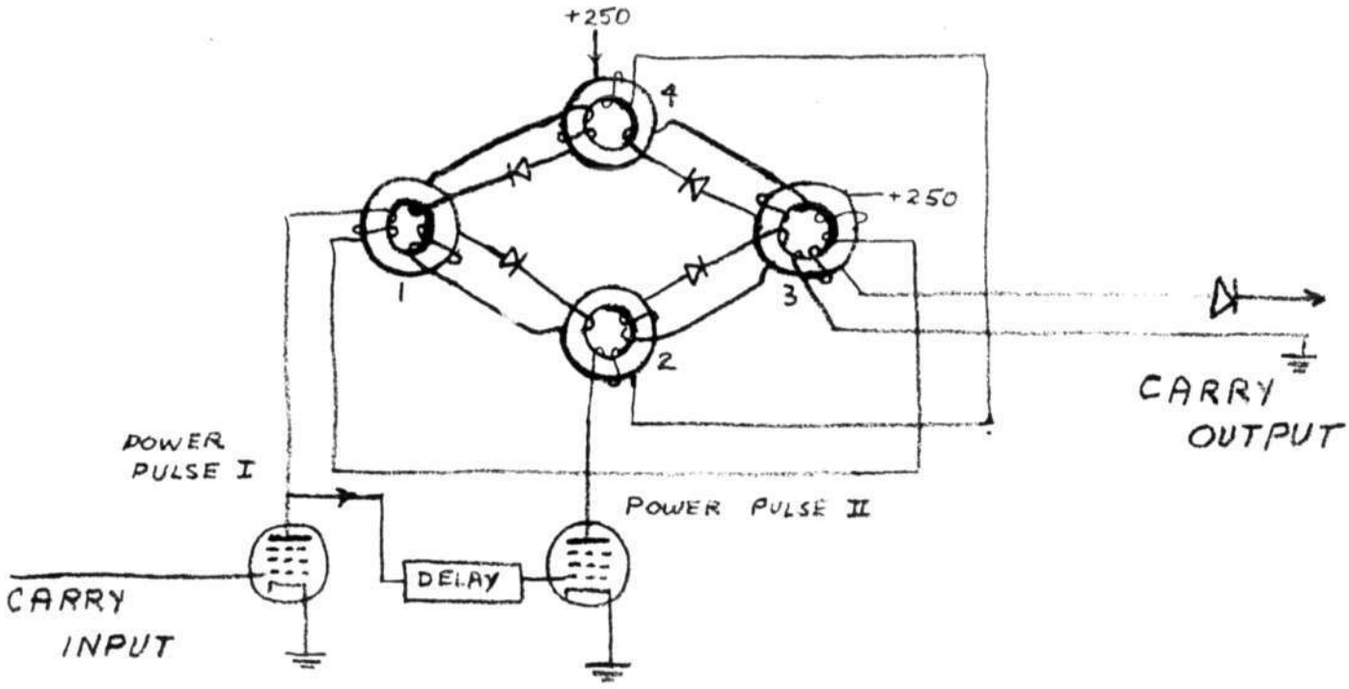
(a)

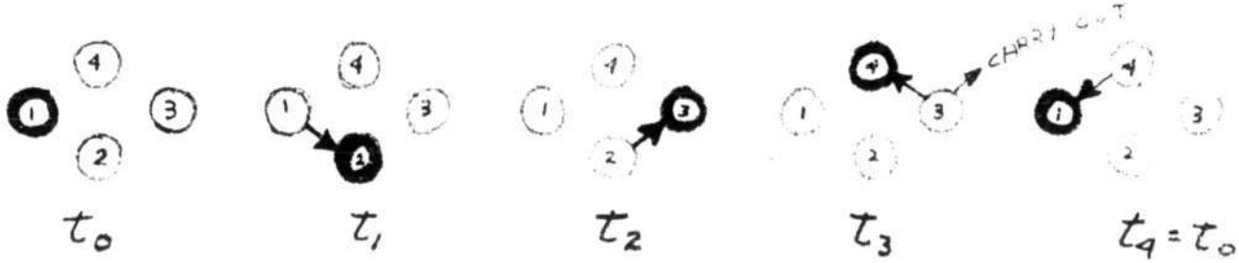


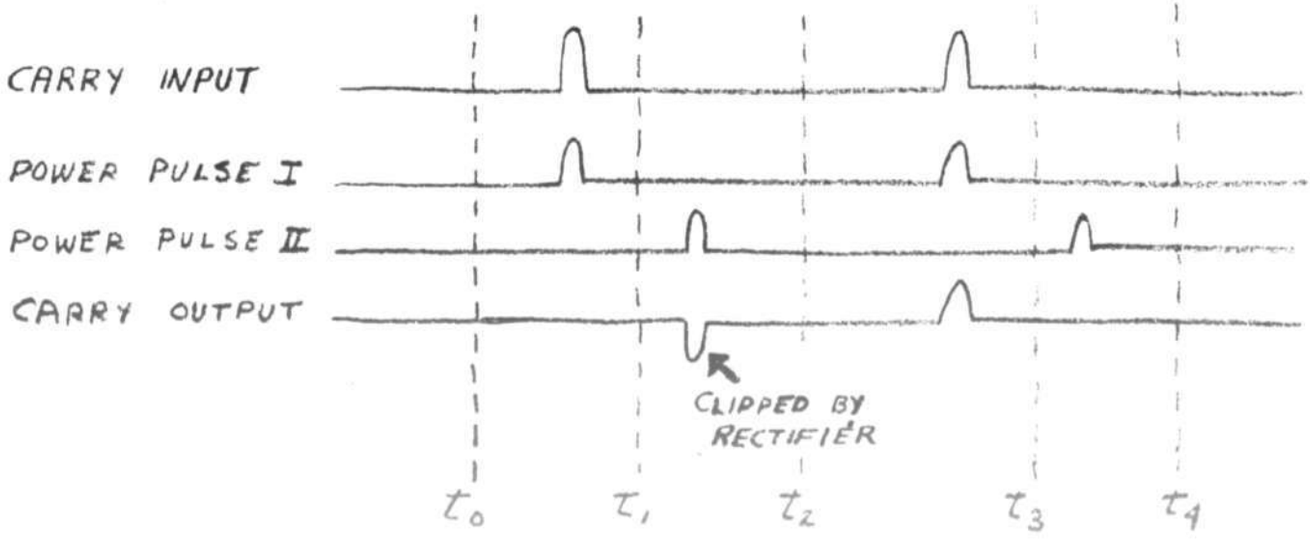
(b)

FIG. 2 GATED CARRY COUNTERS

SA-50618







SA-50619

FIG. 3 MAGNETIC GATED-CARRY COUNTER

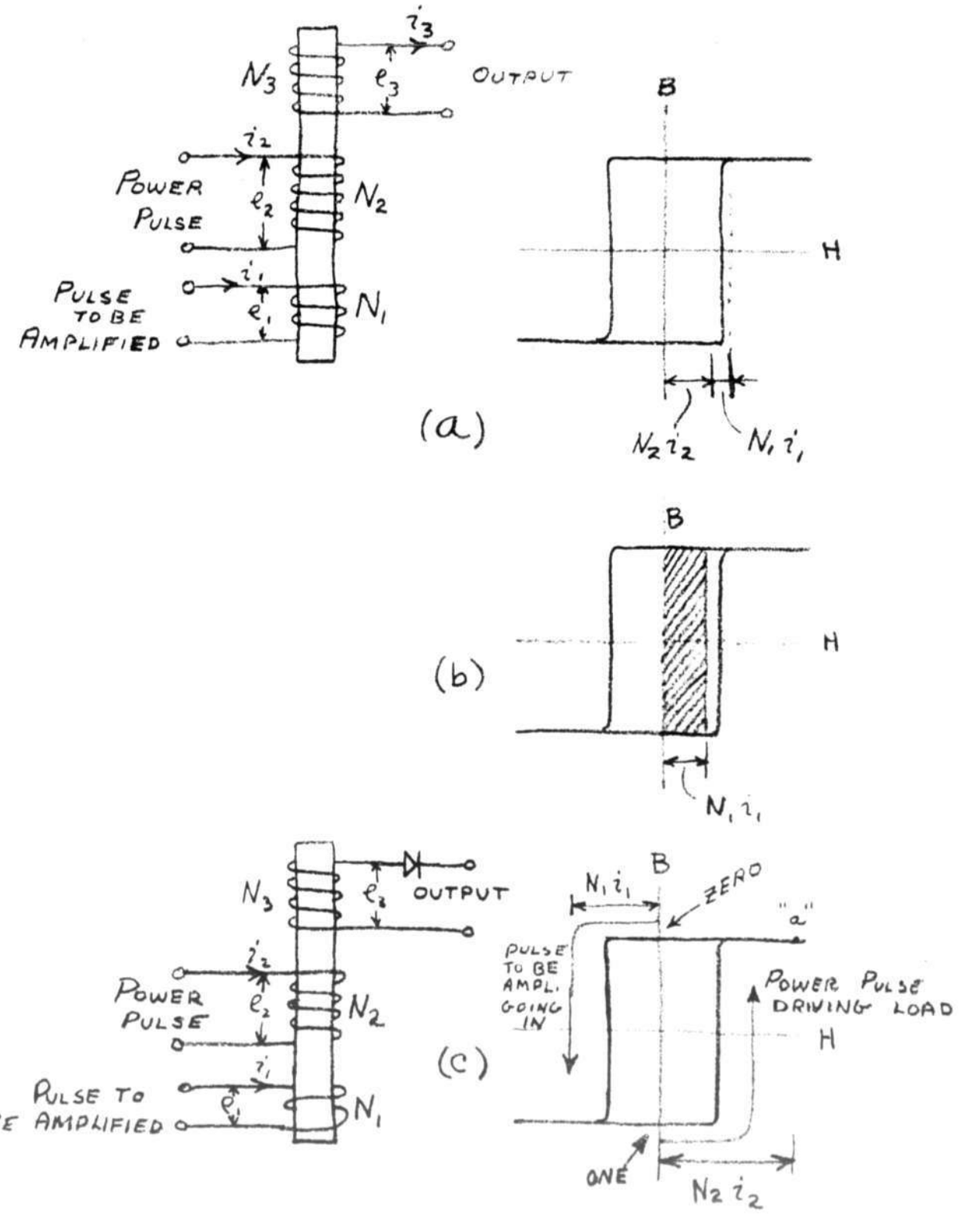


FIG. 4 PULSE-OPERATED CORES

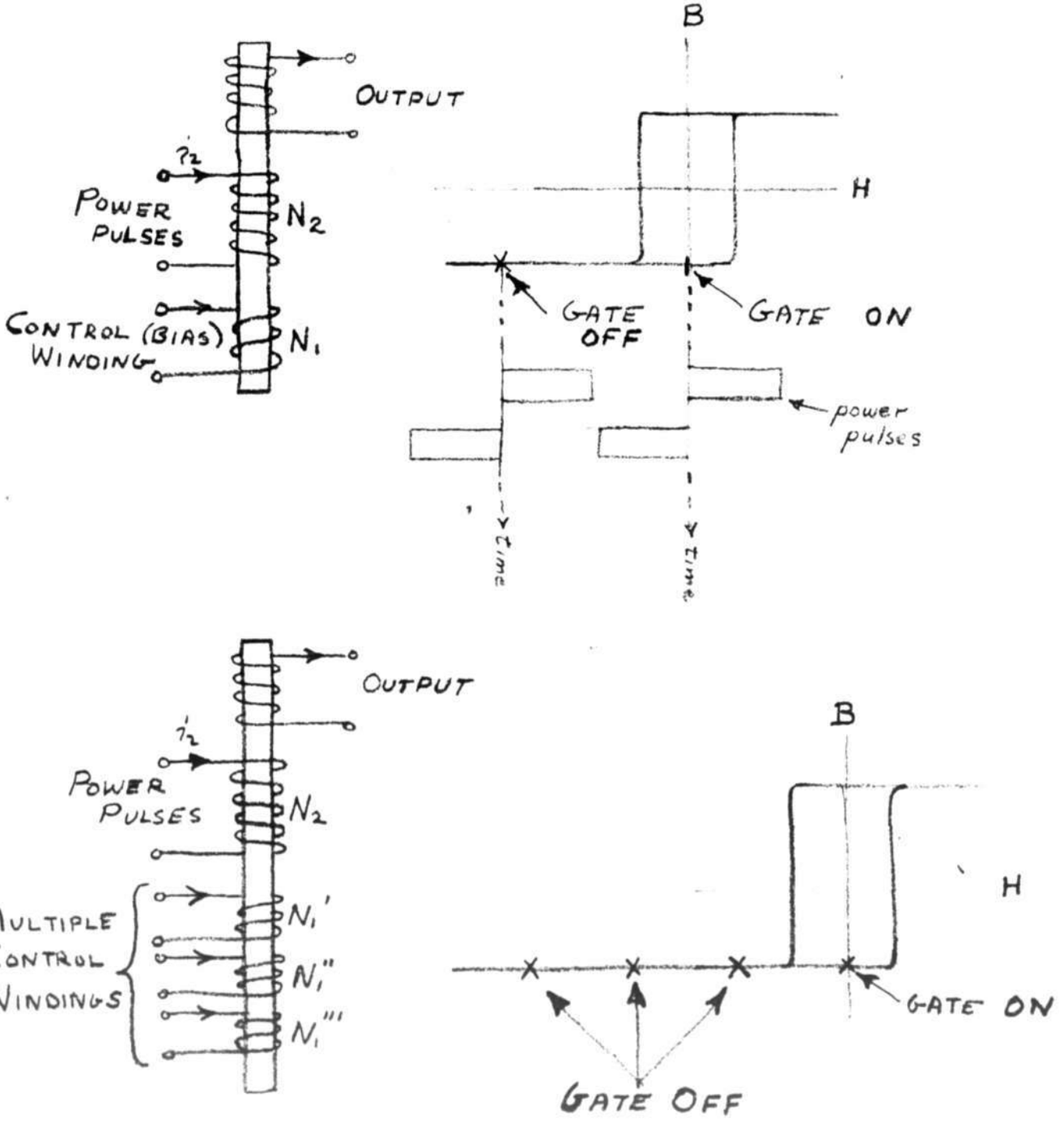
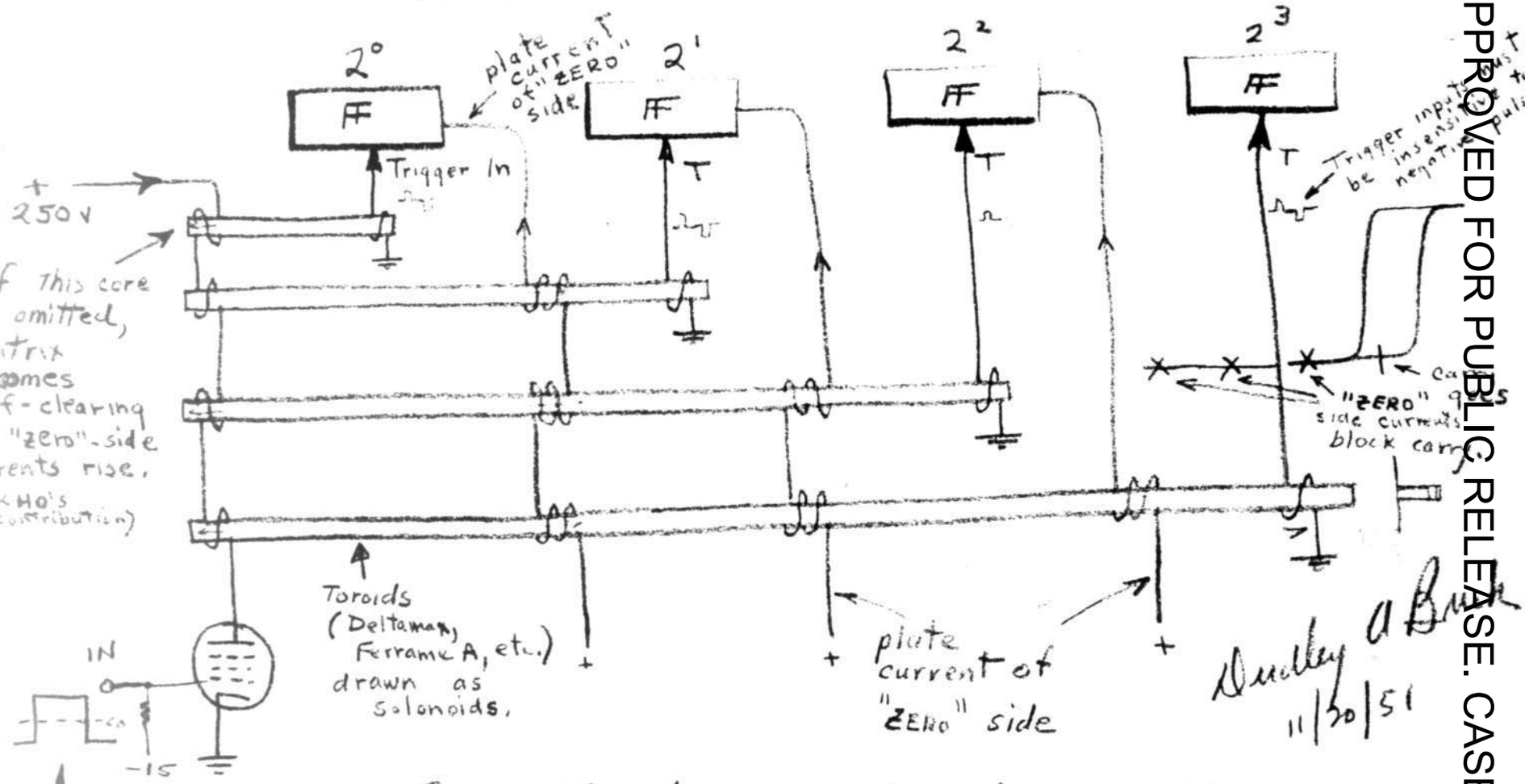


FIG. 5 BIASED MAGNETIC PULSE GATES

A-50621

SA-50532

HIGH-SPEED CARRY FOR TRIGGERABLE FLIP-FLOPS WHEN USED AS A BINARY COUNTER

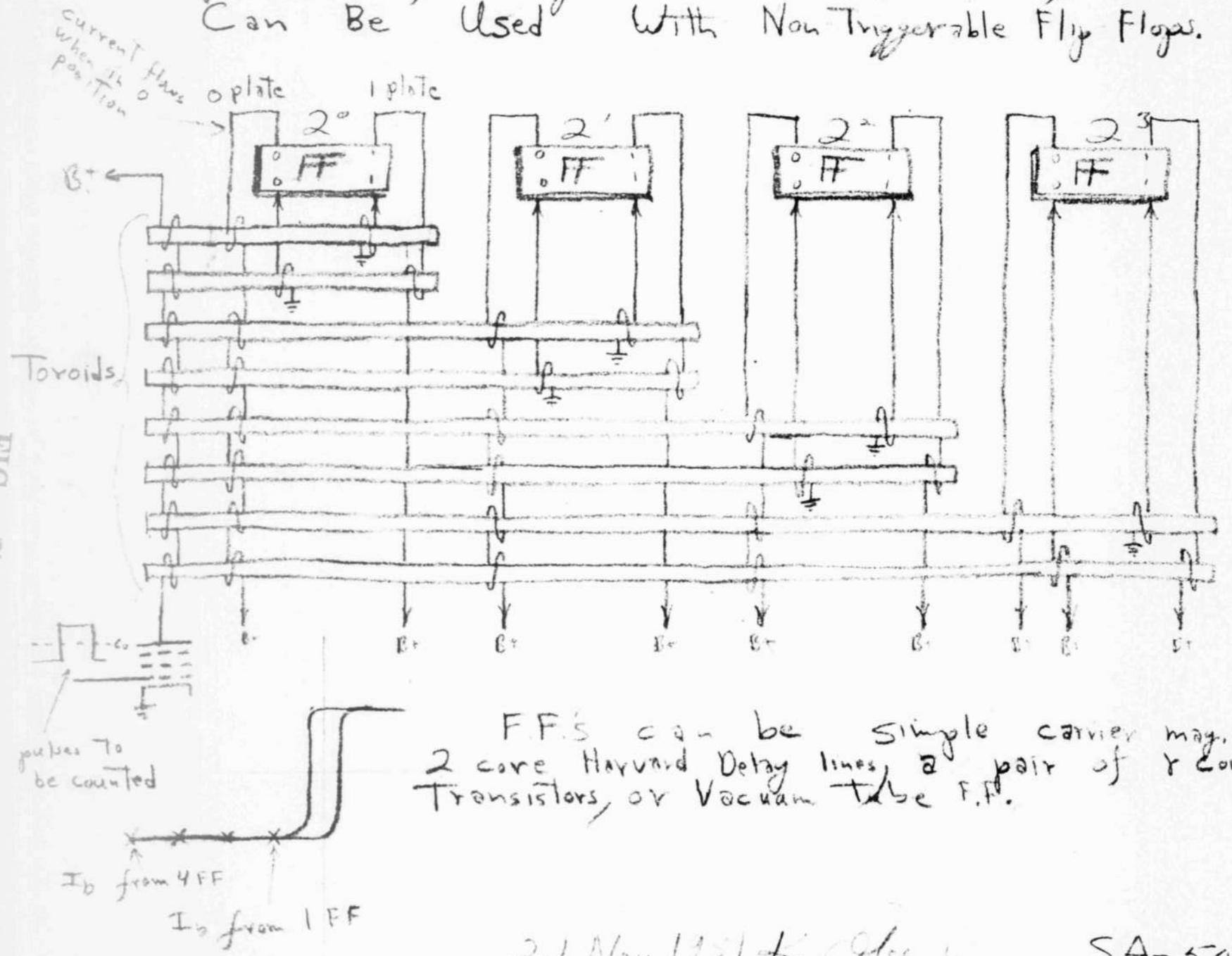


Since 2° stage is only stage which can originate a carry, this high-speed "instantaneous" carry scheme may be used. Possible advantages faster carry, FF output need not trigger next stage, easier to preset, more reliable Triggering.

FIG. 6

SA-50561

Adaptation of Dudley Buck Counter (SA-50532) That Can Be Used With Non Triggerable Flip Flops.



FF's can be simple carrier mag. FF, 2 core Harvard Delay lines, a pair of γ Connected Transistors, or Vacuum tube F.F.

21 Nov 1951 K. Olsen

SA-50561