Digital Computer Laboratory
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SUBJECT: DRIVING CURRENT MARGINS ON MEMORY TEST SETUP I*

To: N.H. Taylor

From: S. Fine

Date: March 6, 1953

Abstract: The sources of noise in an array consist of inductive and capacitive coupling between driving lines and sensing winding, the outputs of half-selected cores and the differences in magnetic properties of the cores. The margins on driving currents are determined by these factors. The lower current limit is dependent mainly on the amplitude of disturbed-ONE and the upper limit by the amplitude of disturbed-ZERO and the half-selected outputs. Experimental results check the validity of a derived equation for determining current margins.

A. Noise sources

Difficulty has recently been experienced with discrimination of signal from noise in the Metallic Array Model I. Some noise signals have been large enough to cut ONES down to the size of noisy ZEROS when the constellation of stored information yielded noises of certain polarities and magnitudes.

There are four sources of noise. Two of these are due to capacitive and inductive coupling between the driving lines and the sensing winding. These sources of noise would be present in the absence of cores in the array. The third type of noise originates from the cores themselves and is due to the half-amplitude current pulses flowing

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* Widrowitz, B., "16 x 16 Metallic Memory Array Model I", R-216, Digital Computer Laboratory, M.I.T., September 25, 1952

through the cores on the selected X and Y driving lines. Differences in magnetic properties of the cores produce considerable variations in the cores' readout signals. The deviations about a mean may also be defined as noise, and this presents a fourth possible source.

B. Inductive and Capacitive Coupling

1. Discussion of noise mechanism.

If the sensing winding were fabricated with precise symmetry, the mutual inductance between the sensing winding and any driving line, including the XY windings, would be zero. This is not quite mechanically possible, however, and the actual value of this parameter may be unpredictable within a power of ten. The range of unpredictability may be controlled by careful construction. Perfection in construction will not eliminate noise due to capacitive coupling between the sensing winding and a driving winding, and the usual geometric aberrations will produce only second-order effects on this coupling. When a di/dt is applied to a driving line, that line is not an equipotential because of its distributed self-inductance. The unavoidable voltage gradient of the driving line is in part transferred to the sensing winding by means of the distributed mutual capacity.

2. Measurements of the noises.

The noises due to inductive and capacitive coupling were indistinguishable, both being roughly proportional to the di/dt of the drivers. There was no advantage in separating these effects, for their sum was the factor of interest. This was measured by writing all ONES into the array and driving the memory lines separately. Since the sensing winding links every other core in the opposite sense, the core noises should cancel except for core variations. Present are uncancelled core noises and coupling noise. A dummy array, identical to the original except that the metallic cores are replaced by fiber washers, was pulsed in the same manner. Less variation and somewhat smaller amplitudes of noises were found in the dummy array. As would be expected only coupling noises were present.

C. Delta Noise*

1. Source of delta noise.

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* Guditz, E.A., "Delta$_{ns}$ in Ceramic Array #1", Engineering Note E-488 Digital Computer Laboratory, M.I.T., October 14, 1952

In order to deliver excitation to a selected core in a coincident-current memory plane, the cores along the selected coordinate lines must be disturbed. This is unavoidable. When these cores are disturbed, they experience internal $d\theta/dt$ while following minor loops on the B-H plane. They are capable of inducing signals in the sensing winding which is threaded through every core in the memory plane. If the sensing winding linked the rows of cores parallel to the driving lines, the noise outputs of the non-selected cores would superpose in reinforcement. If, however, the sensing winding were passed through every other core in the same direction, the alternation from core to core would allow noise bucking.

There are several reasons for the imperfect cancellations that have been observed. Chief among these are the variations in magnetic properties of individual cores, and the differences in noise outputs of cores storing ZERO and those storing ONE. The latter is much more significant and gives rise to "delta noise." If the signal induced in a single-turn pickup winding by a core storing a ONE when driven by a half-amplitude switching current is called HSI, and the corresponding output of a core containing a ZERO is called HSO, then

δ = HSI - HSO is the delta noise.

Several methods have been employed to measure the size and effects on current margins of delta. A single delta is small, usually much smaller than a ONE, and has to be measured indirectly. It was found that a given constellation of ONES and ZEROS along a set of selected lines will not always yield a given amount of delta noise. As one might expect, the noise outputs of these half-selected cores depend upon the history of disturbances of each core from the times when the individuals were most recently switched. The half-selected output of an undisturbed ONE, HSI_1, is much smaller than the size of the corresponding ONE readout. It is due to a half-amplitude current pulse applied in a direction tending to switch that ONE; it does not decay to a null until the driving current is removed if the driving current is left on only long enough to switch a core. This suggests that some form of slow switching is taking place, most likely a departure from the saturation hysteresis loop onto some minor loop that is not very different from the major loop. Subsequent half-selected readouts after the first are all almost identical and turn out to have amplitudes that are much less than HSI_1 at the optimum sensing time.

$$HSI_1 > HSI_2 \approx HSI_3 \ldots\ldots\ldots$$

The HSO, the half-selected output of a core containing ZERO, is hardly affected by disturbance at low and medium driving currents and is very much smaller than HSI_1.

$$HSO_1 \approx HSO_2 \approx HSO_3 \ldots\ldots\ldots$$

Let HSO be the non-selected output of a ZERO after any number of disturbs. Then,

$$\delta_1 = HSI_1 - HSO, \delta_2 = HSI_2 - HSO, \delta_3 \approx HSI_2 - HSO \quad \text{etc.}$$

At lower currents, since $HSI \gg HSO$,

$$\delta_1 \approx HSI_1, \delta_2 \approx HSI_2 \approx \delta_3 \approx \delta_\infty$$

so that the noise of a single delta is approximately equal to the output of a half-selected core containing a ONE.

2. Measurement of delta noise.

Several methods have been employed to measure the size of delta, and to estimate its effects upon current margins. A single delta is small, usually much smaller than a ONE. In order to get this quantity, it was found necessary to measure the cascaded effect of many cores and thence to arrive at an average figure. This was achieved by writing a pattern into the memory so that all cores whose sensed output is positive held ONES and the others held ZERO. A single half-current pulse was applied to the Z-plane winding so that all cores were half-selected in the read direction. The resulting sensed output is the sum of 128 deltas. The Z-plane winding was pulsed a second time to obtain the sum of 128 second deltas. As expected, the second, third, and later deltas did not change in amplitude.

A second method of measuring delta is with the single-core pulse tester. The results of both methods compared favorably.

D. Core Variations

Because of manufacturing difficulties, the variation in core

switching time and voltage amplitude in different cores is great, and it is necessary to test each core carefully and to select only cores within an allowable percentage deviation. This variation or spread in ONES can be considered as a noise in the calculation of probable current margins. The lowest core output is a factor determining the lowest allowable driving current. The variation in delta is the major factor in current margins. Since it will be assumed that the amplitude distribution of the HSI output is the same as the distribution of the ONES and that delta is approximately equal to HSI, then delta will have the same amplitude variations as ONE output.

The output voltage amplitude variation among the curves of Memory Plane 1 is 20% about a mean value. For the present plane, Memory Plane 6, it is 12% about a mean value. (During the year of operation of Memory Plane 1, no noticeable change in core variation was detected.)

E. Current Margins

1. Definition and measurement

Current margins are to be defined as the mean limits of driving current that can be tolerated without interruption of the normal operation of the memory. It is necessary to know the current margins so that a satisfactory method of marginal checking can be incorporated into a computer. Current margins are also a convenient means of judging the qualities of cores.

At present the only means of determining the current margins is by single or multi core testing or by building a magnetic-core memory plane and varying the driving currents until normal operation fails. Obtaining current margins by single-core testing is not as inclusive as the other method in that certain factors encountered in the operation of an array of cores, such as the effects of a first and second delta, are not present to affect the current margins.

2. Determination of lower current margin

A method of calculating current margins from known core characteristics will be derived. It was noticed through experimentation that the lower current margin is determined by the smallest ONE output. This output, amplified, has to be equal to or greater than the bias voltage used to keep the "and" gate cut off at the sensing amplifier output. If the current is reduced too far, the ONE output is not above the gate level, and the ONE is lost. Also, in any memory plane using two-to-one

selection and always a complete read-write cycle there can be only two first deltas. Using these two facts, the smallest ONE output at the lowest current margin can be determined.

The worst operating condition should be considered in determining the lowest current margin. It is understood that in coincident-current operation, the sensed output of a selected core consists of the summation of all the voltages induced in the sensing winding, i.e., disturbed-one voltage plus all half-selected voltages. The worst pattern at the lowest current margin therefore must have the selected core holding ONE and all other cores in the selected lines alternating ONE and ZERO, the polarity of the disturbed ONE being opposite the half-selected ONE output. See Figure 1-a. The resulting signal output is the disturbed ONE minus two first deltas. The second-delta signals have a small amplitude at the lowest current margin and can be disregarded. The resulting output after amplification must be equal to the gate bias voltage.

$$V_g = (1_{D_S} - 2\delta_{1_S})\, G$$

V_g = gate bias voltage

G = sensing amplifier gain at normal operation

δ_{1_S} = (HSI - HSO) average value of first delta at lowest current

1_{D_S} = smallest disturbed-ONE at the lowest current = $1_{A_S}(1-c_1)$

1_{A_S} = average value of 1_D at lowest current

c_1 = percentage distribution of disturbed-ONE about a mean value

$$\frac{V_g}{G} = 1_{A_S}(1-c_1) - 2\delta_{1_S}$$

The distribution of delta is not being considered at the lowest current margin because the average delta magnitude is small.

From single-core pulse tests enough points to plot a distribution curve of ampere-turns against voltage output for the disturbed-ONE output and first and second delta were obtained. See Figure 2. Near the lower current margin region the first delta output is small and the

amplitude of the disturbed-ONE has the most effect on the margin. A straight-line relationship can be approximated near this region with reasonable accuracy. From this assumption the equation for 1_D is,

$$1_D = K_1 I_s + K_2$$

and for the first delta is,

$$\delta_1 = K_3 I_s + K_4$$

Substituting the above values in the preceding equation and solving for I_s, the lowest current

$$I_s = \frac{V_g/G + 2K_4 - K_2(1-C_1)}{K_1(1-C_1) - 2K_3}$$

3. Calculation of largest operating current.

Increasing the driving current to a large value moves the mmf applied to a given core out to a point near the knee of its B-H loop. Increasing the current a small amount after this point has been reached will cause a great change in the half-selected output voltage. The core starts to switch, and its distrubed-ONE output drops. Increasing the current still further will allow the half-selecting pulses to switch the core, and the disturbed-ONE output will drop toward zero. The largest operating current is reached long before this occurs. The highest current margin therefore is determined mainly by the delta outputs.

As in the case of the lower current margin, the worst operating condition must again be assumed, that is, the condition where an operational error occurs and a ONE is rewritten in place of ZERO. This will happen when the summation of the disturbed-ZERO plus all half-selected outputs becomes as large as a ONE. For this case the worst pattern consists of the selected core holding ZERO while half of the remaining cores in the selected lines hold ONE. The half-selected outputs of these cores should be of the same polarity as the disturbed-ZERO output. See Figure 1b. The equation of the resultant signal output is,

$$V_g = (0_{D_L} + 2\delta_{1L} + (N-2)\delta_{2L})G$$

δ_{1L} = first delta at largest current

δ_{2L} = second delta at largest current

O_{DL} = disturbed ZERO at largest current

N = number of cores in a given line

The amplitude of the first delta is large now, and its distribution must be considered. If the assumption is made that its percentage distribution is the same as the distribution of disturbed-ONE, then the largest first delta,

$$\delta_{1L} = \delta_{AL}(1 + C_1)$$

δ_{AL} = average first delta at the largest current

C_1 = percentage distribution in cores

The distribution of the second delta will not be considered because the magnitude of the second delta is small compared to the first delta.

A linear relationship of delta and current can be approximated at the higher current range.

$$\delta_1 = K_5 I_L + K_6 \quad ; \quad \delta_2 = K_7 I_L + K_8$$

A linear relationship of disturbed-ZERO and current can likewise be approximated.

$$O_D = K_9 I_L + K_{10}$$

If the distribution in disturbed-ZERO and disturbed-ONE are assumed the same,

$$O_D = (K_9 I_L + K_{10})(1 + C_1)$$

The critical output voltage is now,

$$V_q/G = (K_9 I_L + K_{10})(1+C_1) + 2(K_5 I_L + K_6)(1+C_1) + (N-2)(K_7 I_L + K_8)$$

Solving the equation for I_L, the largest current,

$$I_L = \frac{V_g/G - (1+C_1)(2K_6 - K_{10}) - K_8(N-2)}{(1+C_1)(2K_5 + K_9) + K_7(N-2)}$$

For exceptionally good cores, the second delta is very low in amplitude and may be disregarded, even at I_L, that is, K_7 and K_8 may be taken as zero is value.

$$I_L = \frac{V_g/G - (1+C_1)(2K_6 - K_{10})}{(1+C_1)(2K_5 - K_9)}$$

The percentage of current margins about a mean value can be found by the equation -

$$\pm \left(\frac{I_L - I_S}{I_L + I_S} \right) \times 100\%$$

4. Obtaining equation constants.

C_1, the core distribution, is determined by the final selection of cores. The value should be kept as low as possible. From single or multi-core tests, a plot of disturbed-ONE, disturbed-ZERO, first delta and second delta against ampere-turns for average cores can be obtained. Equations for the above factors can be determined from the plotted curves and all K constants found.

E_g, the bias voltage of the sensing gate tube, is a circuit parameter. G is the sensing amplifier gain at normal operating conditions. Increasing or decreasing the gain will not change the percentage of current margins but will affect the maximum and minimum driving currents.

F. Validity of Derived Equations

1. Memory Plane #1.

Figure 2 is a plot of disturbed ONE, disturbed ZERO, first and second delta outputs against driving currents. Linear relationships of voltage output and driving current can be approximated from the plotted

curves. All constants needed are then obtained from the linear equations.

As indicated on Figure 2, the disturbed ZERO and the first and second delta outputs are finite, even at low driving currents. By using simplified equations, it will be shown that this plane cannot hold a "worst" type of pattern at normal operating currents, and therefore it will not hold a "worst" pattern at a higher or lower driving current.

"Worst" type pattern with a disturbed ONE output.

The output signal is the smallest disturbed ONE less 2 largest possible first deltas and less 14 largest second deltas. This, amplified, must be equal to or greater than the bias voltage V_g.

$$V_g \leq [1_D(1-C_1) - 2\delta_1(1+C_1) - (N-2)\delta_2(1+C_1)]\,G$$

$V_g = 25$ volts

$G = 7000$

$C_1 = \pm 20\%$

$1_D = 7$ mv
$0_D = 0.6$ mv
$\delta_1 = 0.5$ mv
$\delta_2 = 0.1$ mv
} From fig. 2 at $I_m = 240$ ma.

$$25 \leq [7(.8) - 2(.5)(1.2) - 14(.1)(1.2)] \times 10^{-3} \times 7000$$

$$25 > 19.04$$

This indicates that the output signal from the sensing amplifier is below the 25-volt gate needed to rewrite the ONE.

"Worst" type pattern with disturbed ZERO output.

The output signal consists of the largest disturbed ZERO plus 2 largest first deltas plus 14 largest second deltas. This signal, amplified, should be less than the gate biasing voltage.

$$V_g > [O_D(1+C_1) + 2\delta_1(1+C_1) + (N-2)\delta_2(1+C_1)]\,G$$

$$25 > [0.6(1.2) + 2(.5)(1.2) + 14(.1)(1.2)] \times 10^{-3} \times 7000$$

$$25 < 25.2$$

This indicates that the output signal is larger than the 25-volt gate level and would cause a ONE to be rewritten in place of a ZERO.

These types of errors did indeed occur at normal operating currents for plane #1. At higher and lower currents, the situation was worse; current margins were "less than ± 0%."

2. Memory Plane #6

From data taken on Memory Test Setup I using plane #6, the curves of Figure 3 were plotted. It was found that the magnitude of the second delta was too small to be measured accurately and so would be assumed zero throughout the useful current range. Also, the magnitude of the first delta and disturbed ZERO were small at the lower driving currents and could be assumed zero at this margin. Linear equations were approximated for the disturbed ONE at the lower current limit and the disturbed ZERO and first delta at the upper limit. The constants needed were determined from these equations.

Lower Current Margin.

$$I_S = \frac{V_g/G + 2K_4 - K_2(1-C_1)}{K_1(1-C_1) - 2K_3}$$

$\delta_1 \approx 0$ therefore $K_3 = K_4 = 0$

$$I_S = \frac{V_g/G - K_2(1-C_1)}{K_1(1-C_1)}$$

$V_g = 25$ Volts

$C_1 = 12\%$ distribution in amplitude of cores

$G = 1500$

$K_1 = 0.74$

$K_2 = -0.103$

$$I_S = \frac{25/1500 - (-.103)(1-.12)}{(.74)(1-.12)} = 0.164 \text{ Amperes}$$

Upper Current Margin.

Equation for exceptionally good cores will be used.

$$I_L = \frac{V_g/G - (1+C_1)(2K_6 + K_{10})}{(1+C_1)(2K_5 + K_9)}$$

$K_5 = .25$

$K_6 = -.06$

$K_9 = .21$

$K_{10} = -.05$

$$I_L = \frac{25/1500 - (1+.12)[2(-.06) + (-.05)]}{(1+.12)[2(.25) + (.21)]} = 0.260 \text{ Amperes}$$

The current margins are:

$$\pm \left(\frac{I_L - I_S}{I_L + I_S} \right) \times 100\%$$

$$\pm \left(\frac{.26 - .164}{.26 + .164} \right) \times 100\% = \pm 22\%$$

The actual current margins of Memory Test Setup I using plane #6 were determined by varying the driving currents until an error occurred. The current margin percentage was approximately ± 20%.

Unfortunately, complete curves like those of Figures 2 and 3 were never taken for these cores in a single-core test setup. However, the few points that were recorded fall close to the curves in the figures.

Signed S. Fine
S. Fine

Drawings:

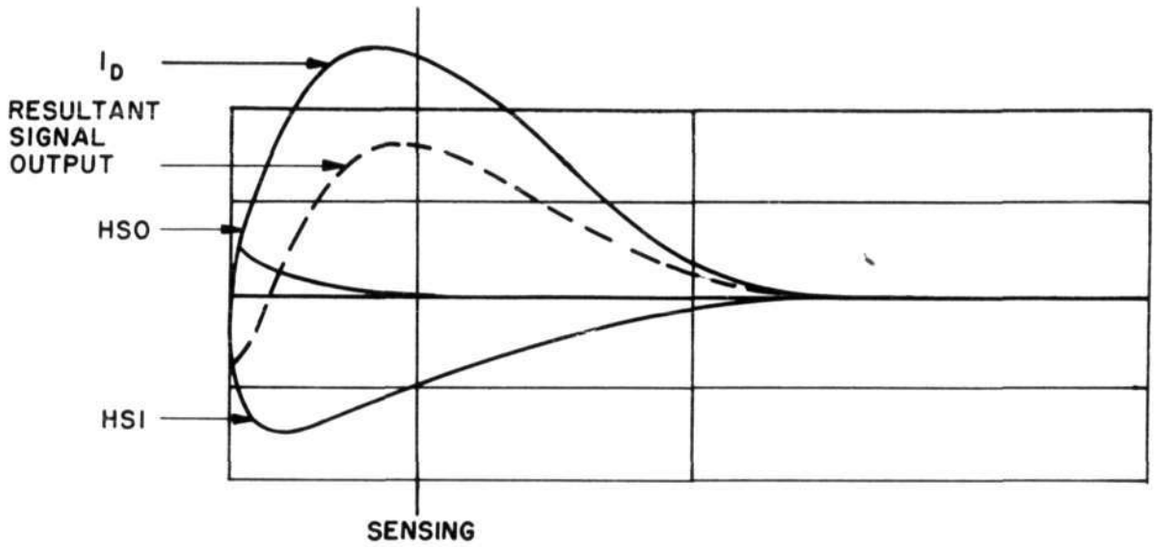
A-54187
A-54186
A-54177

Approved
W.N. Papian

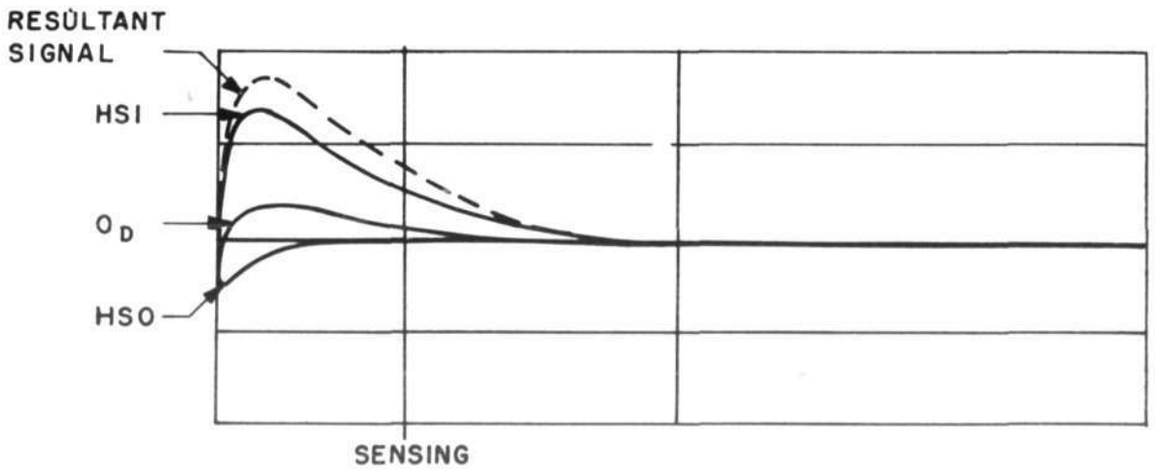
Approved
N.H. Taylor

SF/cs

Drawings attached:
A-54187
A-54186
A-54177



A. DISTURBED "ONE" OUTPUT



B. DISTURBED "ZERO" OUTPUT

FIG. 1

A-54187

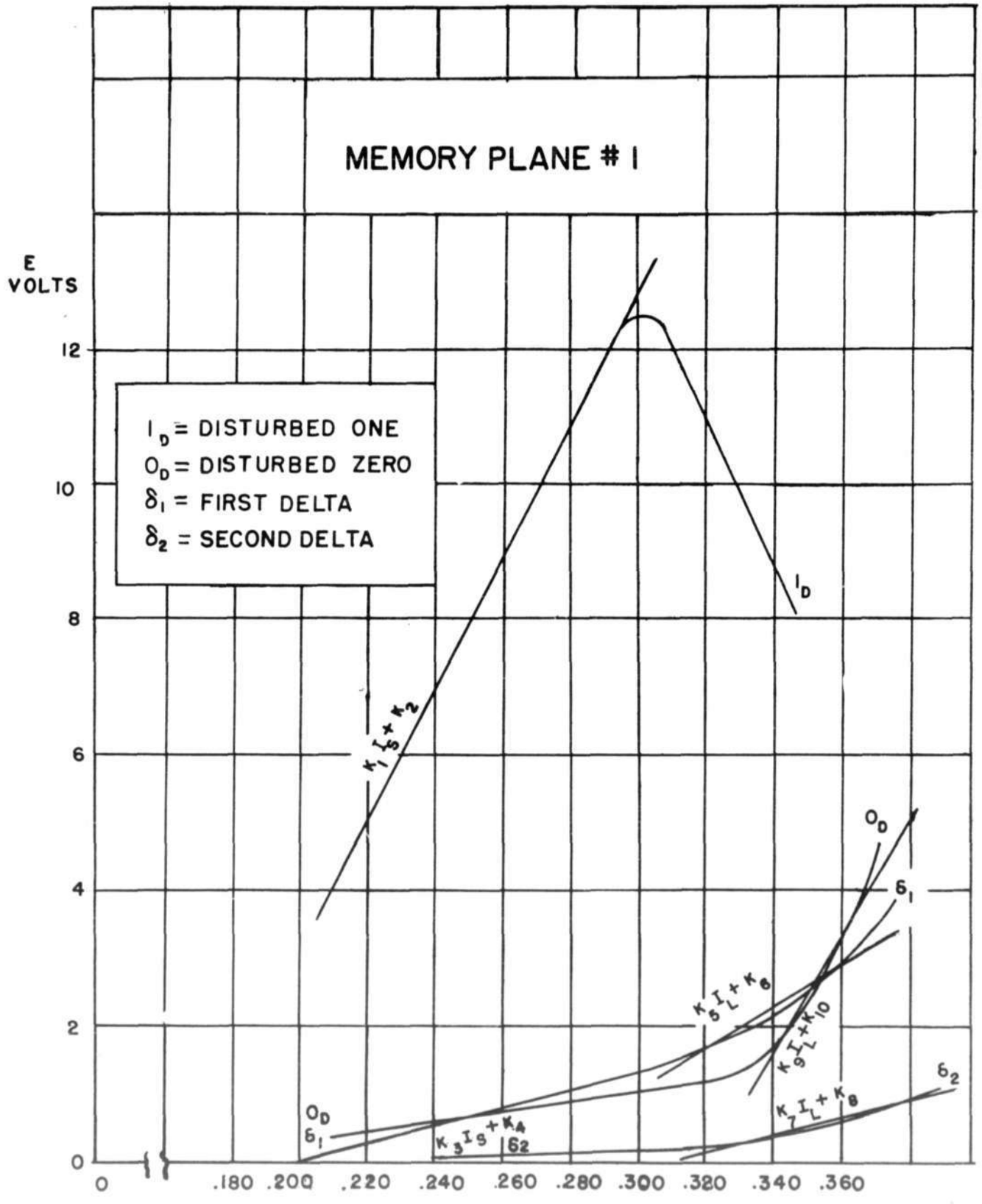


FIG. 2

A-54186

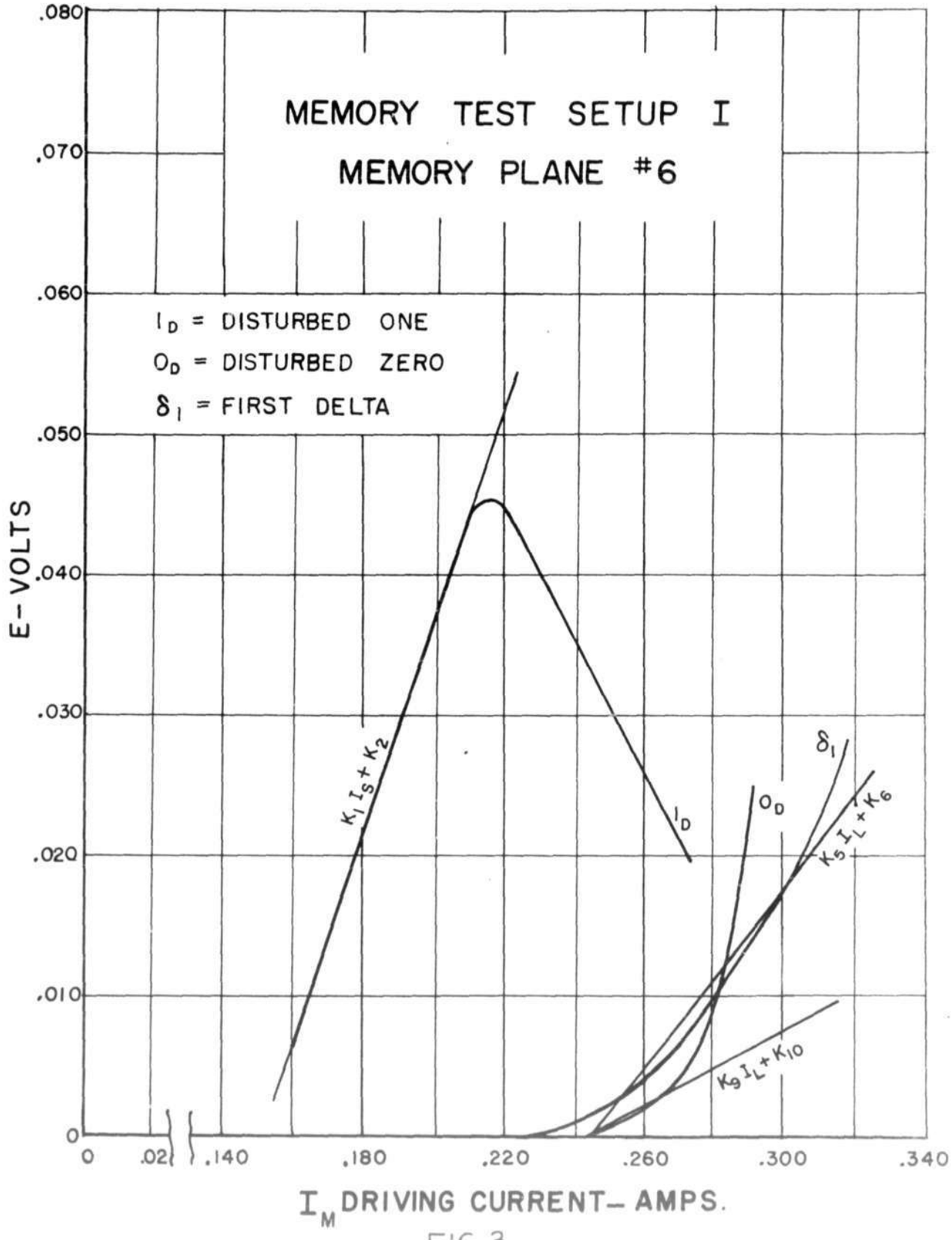


FIG. 3

A-54177