Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BI-WEEKLY REPORT, PART I, APRIL 15, 1949

To: 6345 Engineers

From: Jay W. Forrester

## 1.0 WHIRLWIND I COMPUTER ELEMENTS

### 1.01 Production Report

(H. F. Mercer)

Since April 1 we have received the following panels (production units) from Sylvania:

2 Fuse Panels (completes order)
8 Flip-Flop Storage Registers

The following panels have been completed here since April 1:

Control Switch, Switch Panel
3 Operation Matrix Driver Panels
Storage Switch, Switch Panel
Synchronizer
3 Voltage Variation Panels

### 1.02 WWI System Tests

(G. C. Sumner)

System testing has been continued for the past two weeks except for the time that operation was demonstrated to ONR visitors.

Testing has uncovered two interesting conditions:

1. Contrary to previous thoughts the delay of interconnecting cables and transformers is not quite enough in the "digits from right or left" lines in shifting registers. For example, in the BR a particular digit receives a pulse at the

1.02 WWI System Tests (continued)

grid of the flip-flop which arrives from the adjacent digit before the complete shift command-pulse has passed through the proper gate tube. A considerable margin of operation still exists, however. The possibility of obtaining an interconnecting cable of slightly higher delay than the present RG62U is being investigated.

2. It was found that the 10,000 ohm resistor used in the basic flip-flop circuit from the grid circuit to the cathode allows a bias to be built up on the crystal in series with the grid, when high frequency pulses are applied to the FF grid input. This caused faulty operation in the accumulator when the program called for the accumulator to be cleared just after a multiply operation. If the 10,000 ohm resistor is shunted by a crystal this does not occur.

The time is approaching when additional filament power will be needed. Even at the present time some drifting of filament voltage is being experienced.

1.1 Listed by System Number

104 Control Switch / 201 Storage Switch

(R. E. Hunt)

Switch Panels - Control switch and storage switch switch panels are complete. Resistance checks have been made and the panels have been delivered to WWI.

Matrix Panels - Control switch and storage switch matrix panels. Drafting is complete and the aluminum panels have been fabricated and sent out for painting.

Phenolic panels have been fabricated and assembly started.

Output Panels - Control switch and storage switch output panels are approximately 40% complete in the assembly shop.

106 Time Pulse Distributor

(K. E. McVicar)

Tests on the time pulse distributor have been finished

106 Time Pulse Distributor (continued)

subject to approval of results, and the test specs have been written. Before the panel is finally released it will be tested according to the written and approved test specs.

109 Clock Pulse Control

(J. A. O'Brien)

The finished clock pulse control panel is now undergoing video testing. A large number of modifications have been made in the input and output connections to the panel as a result of the changes imposed by the new method of controlling restorer pulses as proposed in the design of electrostatic storage control. The present design includes one spare flip-flop and three spare gate tubes. It is expected that these will be used however before revision is final. Present tests on the panel indicate a rise time of 0.2 to 0.3 microseconds on the signal applied to the gate tube suppressor grids.

(R. H. Gould)

The clock pulse control panel has been modified to provide proper control with constant frequency restoration of the computer. Further modifications are being contemplated to make use of the flip-flop and gate tubes which have become superfluous. Change notices will be held until a decision is reached on these additional changes.

First tests on the CPC matrix showed a time lag of .6 microsecond between an input pulse to a flip-flop grid and the complete switching of the matrix output. This time lag was reduced to .2 microseconds by changing the matrix output resistors from 3900 ohms to 2200 ohms and changing the matrix driver load resistors from 1000 ohms to 470 ohms.

Timing tests of the matrix-controlled gate tubes show that a flip-flop input pulse (ALARM, RESTART, etc.) must precede the pulse to be controlled by .25 microsecond or more to insure positive operation. This seems to be sufficiently fast to give satisfactory operation in the computer.

111 Synchronizer

(H. S. Lee)

The final assembly has been completed and the panel is in the Inspection Dept. for inspection and testing.

112 Restorer-Pulse Generator

(K. E. McVicar)

Test specs on the restorer-pulse generator are being revised and enlarged to include more extensive video tests and detailed trouble location information.

202 Toggle Switch Storage Switch

(C. W. Watt)

Sheet metal panel is complete, painted, and now is being marked. Terminal boards have been fabricated. About on schedule.

Toggle Switch Storage Output - Final assembly is complete, 2½ weeks ahead of schedule.

404 Comparison Register Check

(H.S. Lee)

All drafting has been completed. Fabrication of the aluminum panel has started, however, it is several days late as projects of higher priority caused the schedule to alter slightly.

(J. A. O'Brien)

The preliminary test specifications of the comparison register check panel are in the process of preparation.

500 Input and Output Registers

(A. K. Susskind)

The design of input-output control as indicated on SD-33818-1 is proceeding. Part of the necessary equipment will be obtained from the following existing panels which are to be modified: 1 A-register, 1 program-register, and 2 check registers. A panel containing 2 DC flip-flops, 4 gate tubes, and 1 buffer amplifier will be designed.

500 Input and Output Registers (continued)

Finally, 2 register-driver type I panels and 6 standardizer amplifiers complete the list of necessary equipment. Construction and modification is not yet scheduled.

601 Check Register

(C. W. Watt)

Quantity requirements have been increased from 35 to 37 to provide 2 panels for in-out control. All 37 aluminum panels have been made, and are now being painted. Phenolic panels are being made.

602 Alarm Indicator Control

(H. S. Lee)

The video layout is approximately 1/3 completed. It is expected that the detailing of the aluminum panel will start Monday, April 18, 1949.

1.2 System Engineering

(H. S. Lee)

Installation - The installation of power cables, transformers etc. in racks C12 and C13 has been completed. The necessary wiring between these racks and the power racks is now being installed. It is expected that these two racks will be ready for operation on Wednesday, April 20.

1.21 Power Control and Distribution

(H. S. Lee)

Voltage Variation Panels - Due to a sudden increased need for these panels the shop is starting a full time assembly program for them. An output of ten panels per week is scheduled with a completion date of May 29 for the final lot of fifty-seven.

1.22 Power Cabling

(H. S. Lee)

Drafting of power cables for racks, C12, C8, C9, C10 and C11 has been completed. Drafting of cables racks

1.22 Power Cabling (continued)

C7 and C6 has started and is progressing satisfactorily. Fabrication of cables for racks C13, C12 and C8 has been completed. A construction requisition for the cables for racks C9-10-11 will be sent to the shop within the next few days.

1.23 Video Cabling

(R. H. Murch)

Flip-flop storage register #2 and flip-flop storage output horizontal video cables have been received from Sylvania and installed.

About 90% of central control cables that are measured have been received from Sylvania.

1.24 Standardizer Amplifier

(R. E. Hunt)

Drafting is now complete on this unit. Fabrication of 8 units will start immediately.

1.25 Time Schedules

(R. A. Osborne)

All detailed time schedules have been posted for March and copies distributed.

The summary schedule for Summary Report 18, March, has been posted.

1.3 Auxiliary Equipment

1.31 Power Supplies

(J. J. Gano)

Filament Alternator Regulator - A breadboard assembly has been partially tested and appears satisfactory. A d-c amplifier to be used with the Brush Oscillograph has been constructed and is being tested. Its use will permit further tests on regulator response when subjected to sudden load disturbances. The power supply being constructed should be ready for testing next week.

| WWI Drawing List | Block Diagram | Block Schematic | Circuit Schematic |
|---|---|---|---|
| System | B-37071-5 | | |
| Control | B-37098-4 | | |
| Master Clock | B-37159-2 | | |
| 101 Pulse Generator | B-37155-3 | B-32385 | E-32333-4 |
| 102 Program Counter | B-37062-4 | B-32213-1 | D-31516-6 |
| 103 Program Register | B-37067-3 | B-39289-2 | D-33836 |
| 104 Control-Switch Matrix Panel | B-37066-3 | C-33843 | R-32722-5 |
| 104 Control-Switch Switch Panel | B-37066-3 | | Z60CS00-2-D |
| 104 Control-Switch Output Panel | B-37066-3 | | Z60CS00-B |
| 105 Operation Matrix Driver Panel | | S600M00 | Z600M00-1-E |
| 105 Control-Pulse Output | | R60CP00 | S60CP00-1-B |
| 106 Time-Pulse Distributor | B-37068-4 | T60PD00-3-A<br>T60PD00-4-B | |
| 106 Time-Pulse-Distributor Counter | | T60PD00-3-A | Y60PD00-C |
| 106 Time-Pulse-Distributor Output | | T60PD00-4-B | Z60PD00-1-D |
| 109 Clock-Pulse Control | B-39817-3 | C-32642-4 | R-31916-7 |
| 110 Frequency Divider | B-37154-3 | B-32264-1 | R-31729-2 |
| 111 Synchronizer | B-37172 | C-33485 | R-33486-1 |
| 112 Restorer-Pulse Generator | B-37160-1 | B-32209-4 | D-31909-8 |
| 200 Test Storage | B-37156-2 | | |
| 201 Test-Storage Amplifiers | B-37121-2 | C-32855-2<br>C-33768 | D-33706-1 |
| 201 Storage-Switch Matrix Panel | B-37121-2 | D-32855-2 | R-32722-3<br>D-33706-1 |
| 201 Storage-Switch Switch Panel | B-37121-2 | | Z60CS00-2-D |
| 201 Storage-Switch Output Panel | B-37121-2 | | Z60CS00-B |

| WWI Drawing List | Block Diagram | Block Schematic | Circuit Schematic |
|---|---|---|---|
| 202 Toggle-Switch Storage Switch Panel | B-37122-3 | C-33768 | D-33706-1<br>C-33707 |
| 202 Toggle-Switch-Storage Output Panel | B-37122-3 | | E-32721-3 |
| 203 Flip-Flop-Storage Output | B-37060-5 | B-32269-1 | E-31635-4 |
| 203 Flip-Flop Storage Register | B-37057-4 | B-32268-1 | E-31621-4 |
| 203 Flip-Flop Storage Control | B-37061-7 | D-32106-3 | |
| 301 A-Register, Digit 0 | B-37056-3<br>B-37072-7 | B-31574-1 | D-31573-7 |
| 301 A-Register, Digits 1-15 | B-37056-3 | B-31211-3 | D-31276-12 |
| 302 Accumulator, Digit 0 | B-37173 | D-32851 | R-32850-2 |
| 302 Accumulator, Digit 0, Aux. Panel | B-37173 | B-32492-2 | D-32602-1 |
| 302 Accumulator, Digits 1-14 | B-37173 | D-31213-3 | R-31275-9 |
| 303 B-Register | B-37097-4 | B-31212-5 | D-31277-6 |
| 304 Sign Control &<br>308 Divide-Error Control | B-37072-7 | C-31576-3 | E-31619-2 |
| 305 Step-Counter | B-37074-6 | D-31828-1 | D-39764-3 |
| 305 Step-Counter Output | | A-32723-1 | D-32735-2 |
| 306 Multiply &<br>307 Shift Control | B-37072-7 | C-31532-3 | E-31588-5 |
| 308 Divide Control | B-37072-7 | C-31552-3 | R-31718-5 |
| 309 Special Add Memory & Overflow | B-37072-7 | C-31575-5 | E-31632-5 |
| 310 Point-Off Control | B-37072-7 | C-31600-6 | E-31717-6 |
| 403 In-Out Register | B-37119-2 | E-32434-2 | D-31277-6 |
| 404 Comparison Register | B-37120-2 | B-32578-1 | E-32576-5 |
| 404 Comparison-Register Check | | B-33488-1 | E-33515-1 |
| 601 Check Register | B-39816-3 | B-32577-1 | E-32576-5 |
| 601 Check-Register Check | B-39816-3 | B-32018-1 | E-32023-2 |

| WWI Drawing List (continued) | Block Diagram | Block Schematic | Circuit Schematic |
|---|---|---|---|
| Alarm-Indicator Control | B-37175 | B-33603 | E-33651 |
| Standardizer Amplifier | | B-33881 | C-33880 |
| Bus Driver, Arithmetic Element | | A-32297-1 | D-31727-7 |
| Bus Driver, Flip-Flop Storage | | A-32296-1 | D-31726-7 |
| Register Driver, Type I | | B-32207-1 | E-32261-7 |
| Register Driver, Type II | | B-32691-2 | D-32690-2 |
| Bus Connections | B-37124-3 | C-37123-3 | |
| Fuse-Indication Panel | | | W60PP00-7-D |
| Voltage-Variation Panel | | | W60PP00-6-C |
| WWI Power-Connector Pin Connections | | | B-31955-6 |
| Digit-Interlock Panel | | | W60PP00-8-B |
| Fixed-Voltage Switching Panel | | | T-60PP00-11-B |
| Power-Interlock & Indication Panel | | | Z-60PP00-12-B |

## 2.0 WHIRLWIND I RESEARCH

### 2.1 Circuits

#### 2.11 Flip-Flop Design and Stability

(R. L. Best)

Tests have been run on a 6Y6 flip-flop that is d-c coupled to its load. 6SN7 cathode followers are used to couple the plate waveforms to the opposite grids, so that there will be no drop across the "off" plate resistor. It develops 28 volts across 400 ohms, and therefore can drive a very heavy load. The minimum cathode trigger amplitude is 14 volts unloaded, or 16 volts when driving 100 micro-micro farads (at 2 m.c.). This corresponds to 4.5 volts for the standard WWI flip-flop, loaded with two gate tubes. Sixteen volts is too high to be used in many of the existing circuits.

In general, I believe that it would be better to use a smaller flip-flop, with buffers on the output rather than a powerful flip-flop such as this, which requires a buffer within itself anyhow, and would often require a buffer to trigger it. However, there may well be special places where this is the most economical circuit for the job.

The shop is now working on breadboards for two 6AN5 flip-flops; one a d-c flip-flop d-c coupled to its load, and the other an a-c flip-flop a-c coupled to its load

### 2.2 Components

#### 2.23 Vacuum Tube Studies

(John Olivieri)

Forty-five 7AD7 and 45 7AK7's have been marked, tested, and burned for 100 hours. Forty-five 7AD7 and 45 7AK7's are now being burned in the racks.

2.23 Vacuum Tube Studies (Continued)

The 6SN7 rack has been worked on and 6SN7's will be burned for 100 hours.

Sixty special 6AG7's were received from RCA and were tested. These tubes have cathode sleeves with high, intermediate and low silicon.

Ten 6AN5's, 10 5687's and 60 7AD7's were tested for B. Frost.

Two more 3E29's have been returned as failures. These tubes became gassy without being in operation.

Tubes for the Switch Panel, Control Switch/Storage Switch and for the Switch Panel, Toggle Switch Storage were completed and delivered.

Tubes of all types were inventoried and chart of present needs and reserves made.

(H. B. Frost)

On April 12 a group of 39 special 7AD7 tubes and 20 F8B 7AD7 tubes were removed from the life test racks and tested, using both standard tests and pulse tests. Of the 39 special tubes, the only ones showing any deterioration after 1400 hours were those made with a high silicon (599 alloy) cathode sleeve. The effective resistance of the interface in these tubes was of the order of 5 ohms, which does not interfere with normal operation. Ten F8B tubes running in the same panel showed a little interface resistance after 1400 hours, but only one tube had a measurable resistance (about 5 ohms). Ten F8B tubes operating in a panel with an 8 volt filament supply showed more deterioration after 1000 hours. Effective interface resistance varied from a value too small to be measured to a value of 24 ohms. All these resistances were measured using 6.3 volt filament supply, zero bias, and 250 volt plate and screen supply, using a pulse method.

A group of 10 5687 tubes were removed after 495 hours in the life test rack. They had been operated

2.23 Vacuum Tube Studies (Continued)

with normal filament voltage, #1 plate carrying about 40 ma and #9 plate cutoff. Of these tubes, 5 which were made in the first quarter of this year (code 3229-13) were very poor. The normally-on side had already developed an effective interface resistance of the order of 20 ohms in all tubes, while the normally-off side had developed an effective interface resistance of the order of 200 ohms. Another group of five 5687 tubes made in the last quarter of 1948 (code 3228-52) were better. The on-side effective interface resistance was still of the order of 20 ohms, but the off-side effective interface resistance was of the order of 50 ohms. This information will be transmitted to Tungsol.

Information from Raytheon indicates that 6AN5 tubes have shown no interface development. Two 6AN5 life test panels have been designed and built; operation will be started in the near future. Dick Best is to investigate 6AN5 flip-flop possibilities.

2.3 Systems

2.31 Five-Digit Multiplier

(R. W. Read)

The life test on the five-digit multiplier began on April 11, when the 15v bias generator was put back in operation. Errors immediately dropped by about 70 per cent. Marginal checking has been used to remove faulty components. Reliability is apparently very high.

A certain pattern to some errors indicates that transients may be entering by means of the A.C. lines. A recorder has been on the line for monitoring purposes. Sudden failure of a T-connector in the coaxial cabling caused a chain of errors; the T was open circuited. It may have been the source of other intermittent errors.

## 3.0 SPECIAL CIRCUITS

### 3.2 Test Equipment

#### 3.21 Standard Test Equipment

(R. L. Massard)

Video Amplifier - All video amplifiers specified have been completed and are in use. The cannon-type power connector cables have been installed, and also the one-stage d-c filament supply. The drawings of the video amplifier (D-33501), the amplifier power supply (SA-33357), and the probe power supply and control panel (SB-33410) have been completed. The complete report on the whole system, R-164, will be available shortly.

A gated video amplifier is being considered as a thesis topic. If feasible, this particular type of amplifier will result in great power savings and/or greater bandwidths, output voltages, and gain. A number of gating methods are being considered.

#### 3.22 Special Test Equipment

(H. Kenosian)

The Megasweep Booster amplifier was improved to pass 38 megacycles at the half-power points. The unit is now being used in conjunction with a sweep frequency oscillator for testing the band pass characteristics of coils. These coils are a part of the RF readout system in the storage tube program.

## 4.0 BLOCK DIAGRAMS

(J. M. Salzer)

M-828 has been issued to explain the action of the in-out orders and to describe their timing.

An entirely revised block diagram for the arithmetic element was prepared.

The name of ACO Carry has been changed to overflow in order to avoid confusion with the carry on the ACO panel. In practice it has been found convenient to number the carry FF's according to the digit number of the panel on which they are physically located; this numbering also agrees with the indicator light arrangement. This means that the number of the AC carry FF's runs from 0 through 14. Logically the number of the carry now designates the digit into which we carry.

(R. P. Mayer)

There has been some discussion in the past concerning the possibility of allowing the arithmetic element and electrostatic storage to operate simultaneously whenever possible. One disadvantage to this arrangement is the possibility of confusion when trying to locate troubles. One advantage to this "as-es overlap" is a saving in time.

In order to determine the probable overall saving in time, a number of codes are being analyzed in an effort to estimate the percentage use of arithmetic and other orders. The codes being considered are: the codes presented in the Application Study Group (including the ballistics problem, in-out conversion, sines, etc.); E-161, code for solution of simultaneous equations by elimination; R-156, intact stability study programmed for a digital computer; R-155, application of digital computers to simulation of the anti-submarine problem. Any suggestions, concerning other large-scale codes that might also be included, will be welcomed.

  

## 5.0 CHECKING METHODS

(G. C. Sumner)

A meeting of those interested in trouble location and checking was held April 4 to discuss the present status of the problem. Three other meetings of smaller groups were also held. These meetings, more of which are indicated, have served to clarify objectives and to formulate compromises necessary to a system usable during the early stages of WWI operation.

(C. W. Adams)

At recent discussions several philosophies of checking and trouble-location have been weighed and a few tentative conclusions have been reached. The generally accepted goal is a program which will automatically check all functions of the computer under the most extreme conditions in a minimum of time and storage. This program could then be performed repeatedly with an automatic marginal checking procedure in progress. This goal will not be reached for a long time, and it seems necessary to plan the work in such a way that it will be of use in preliminary checking at each stage in the development of the program.

In particular it is desirable to coordinate the development of the checking with the installation of components of the computer. Thus checking the arithmetic element and central control will come first. Since little is known about central control checking procedures and the control is soon to be installed (and aside from that, since central control is basic) the problem of checking control will be considered first.

The overall problem will be further subdivided into the functions of the computer which are associated by marginal checking. In this way programs will be evolved which can be repeatedly performed while one of a few of the voltage variation channels are varied, and at the successful conclusion of such a procedure one would have assurance that all functions affected by the particular variation channels have been checked and found to have margins of operation which practically guarantee safe operation for the next few hours. Thus different programs will be written for use with each variation channel of group of channels and when each channel has been varied (while its particular check problem is being cyclically performed) the entire computer will be shown to have a margin of satisfactory operation.

5.0 CHECKING METHODS (cont)

In developing these programs, all of which may be eventually grouped into the one check program which is the ultimate goal, G. Cooper and C. Adams are starting with the simplest possible programs and gradually increasing the complexity until all functions in the particular channel have been checked. In addition to giving a solid logical procedure to work along, this system can possibly yield a workable means of trouble location as well as checking. Thus if a check problem shows a fault, that check problem can be synthesized in the machine (manually) in the same fashion that it was developed on paper, the exact step at which the failure occurs noted, and the trouble thereby partly isolated (since each increase in complexity checks only a few circuits which have not previously been checked). The first such program to be investigated, on which work is starting, is to start the computer from a cleared position with all storage cleared. Since operation zero will be only program timing, during preliminary testing using test storage, only a few functions will be checked. What functions are really checked in this simplest of all programs remains to be seen.

(J. M. Salzer)

The problem of Input-Output checking with the use of the Eastman-Kodak Film Reader-Recorder was closely investigated in E-225. On basis of this study certain modifications were suggested.

It appears that the checking of communication between the Reader-Recorder and WWI can be made nearly perfect presuming no error in the manual preparations and in the programming. The manual preparations involve the proper connection of cables between the Reader-Recorder and WWI, while coding with Input-Output requires the supply of the right order and the right number of orders. Thus there is premium on the correct manual operations and on the correct programming. Only much more complex checking equipment could reduce the responsibility on the human.

(G. Cooper)

The work done on arithmetic modifcation of operations has been written up.

Much of the time has been spent considering and discussing various aspects of checking. More or less general agreement has been reached on the manner in which checking problems are to be devised. It is felt that several simple problems which are in the nature of trouble location sequences would be more suitable for a starting point than a true checking problem which will simply indicate the presence of

5.0 CHECKING METHODS (cont)

trouble rather than its location. It is believed that this approach will eventually lead to a true checking problem in addition to the trouble location sequences. These sequences will be coordinated with marginal checking.

As a starting point, the operation denoted by 00000 with all registers cleared is being studied to determine the extent of the checking which will be accomplished through its use. This operation has been chosen because we can arrange everything by pressing the computer clear button, setting toggle-switch storage to zero, and pressing the restart button. The computer will automatically perform this operation without further ado.