

6345
Memorandum M-237

Page 1 of 9 pages.

Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BI-WEEKLY REPORT, PART 1, FEBRUARY 6, 1948
To: 6345 Engineers
From: Jay W. Forrester
Date: January 2, 1948

1.0 WHIRLWIND I COMPUTER ELEMENTS

1.1 Listed by Block Diagram Number

100 Operators' Console

(C.W.Watt) A conference should be held shortly to crystallize thinking about the console & trouble-location board. The latter may involve a lot of equipment, most of which is as yet undefined.

(H. Kenosian) The modified push-button circuit for the operators' console is now being constructed in breadboard form for tests.

The modified circuit will enable the saving of many tubes by permitting a single pulse-forming circuit to be channelled to any circuit desired.

101 Master Clock

(H. Kenosian) The schematic for the Master Clock has been completed by the Drafting Room in sketch form (SD-39545). It is not planned to build any of these units in the near future, since its function can be handled by existing test equipment.

102, 103, 601, Program Counter, Program Register, Check Register
(H. Fahnestock)

Circuit schematics of these registers will be modified to include changes in basic circuits and will become grade II. They will be furnished to Sylvania in the next two weeks which is way ahead of schedule. This will facilitate procurement of parts and permit preliminary layout on the basis of which to order racks.

103 Program Register

(H. Fahnestock) We have received the sample prototype program register digit panel from Sylvania, together with layouts and mechanical drawings. This was built to demonstrate construction and quality control standards, and appears very satisfactory. It is now undergoing detailed inspection. The order was placed December 16, delivery estimated January 15, delivery made February 5.

106 Time Pulse Distributor

(H. Kenosian) All preliminary sketches for time pulse distributor control have been completed. The circuits will be drawn up in final form when the sketches are discussed with the engineers concerned.

The modified restorer pulse-generating circuit has been found satisfactory. This circuit saves one tube.

107 Operation Timing Matrix

(J.A. O'Brien) The development of this unit is being studied by myself and Slavin of Sylvania. The principle problems are space limitations on the horizontal drivers and the output gate tubes. The matrix is quite large and to increase its size is undesirable from the point of view of increased capacitance to ground; therefore we are considering some methods shortening the output lines.

203 Flip-flop Storage

(H. Fahnestock) The flip-flop storage has been rearranged. Formerly we planned 80 panels of one digit each and 16 output panels. M-236 gives the details of the new plan. There will be two types of panels; one contains two digits and the other a digit and an output section. Circuit schematics will be available to Sylvania February 23 and March 8 without modifying the existing schedule.

300 Arithmetic Control

(G.C. Sumner) The schematic diagram of the Sign Control and Divide Error panel has been almost completed by the drafting department. Schematics of two other panels of arithmetic control are in process in the drafting room. A sketch of the Point-Off-Control panel has been made. This panel, which was mentioned in the previous bi-weekly report, consists of two flip-flops and associated components, totaling 16 tubes. It will enable determination of the location of the first significant digit of a number in the accumulator.

301 A - Register

(G.C.Sumner) A sketch of additional circuits to be included in AR-0 has been made. AR-0 will include the following, in addition to circuits in the other 15 A-register digit: one cathode follower buffer on the 1-side of the flip-flop, AR sign gate tube, and magnitude gate tube. The drawing should be ready by February 13.

(C.W.Watt) Schematic of A-Register and component list are now in Sylvania's hands. Both are Grade II and prototype layout is proceeding at Sylvania.

302 Accumulator

(N.H.Taylor) The final schematic for the accumulator is being checked together with the video layout drawings. Minor changes have been necessary due to the revisions in the "Basic Circuits". Construction of the prototype accumulator should start within the next two week period.

303 B-Register

(C.W.Watt) The Schematic of the B-Register, is now complete and in Sylvania's hands. It is a grade II drawing and they have been authorized to proceed with the video layout.

1.2 System Engineering

1.21 Power Control and Distribution

(C.W.Watt) Power Control: An informal conference with Forrester and Everett was held Monday, February 2, to discuss the problem of overall power distribution to the system. Conclusions were as follows:

1. From the viewpoint of marginal checking, a register-wise connection of the input power would be best. That is, each register, 16 digits long, would be fed power separately from every other register, and the voltages on that register would be varied independently.
2. Fusing would be done only at the main distribution racks.

Subsequent discussion with Brown and Taylor indicates some compromise between distribution fusing and local fusing is needed.

Attention must be given to the problem of decoupling the panels or racks or registers. D.C. troubles should be located by D.C. methods, especially during installation and test.

1.3 Auxiliary Equipment

1.31 Power Supplies

(H.S.Lee) As a result of the conference of January 30, wherein it was decided to standardize on one type filament transformer of 10 ampere capacity (secondary rating), a new recapitulation of transformer requirements has been made. Insofar as can be ascertained at this time WWI will require approximately 537 transformers of this type. Also tentative specifications for this type transformer have been drafted and will be presented for approval on or before February 11.

1.32 (Air Conditioning)

(J.C.Proctor) The general air conditioning problem was again discussed with Mr. Kaufman of Carrier, and a number of points settled. M-223 gives details of this conference.

A location on the main roof directly over the computer room has been selected for the air conditioning equipment, and an estimate has been obtained for the necessary structural supports and shelter.

1.4 Unclassified

Basic Circuits

(J.A.O'Brien) The name of the standard circuits has been changed to basic circuits. The latest revisions of the basic circuits are now in the drafting room and will be completed next week.

Further details are included in Memorandum M-229.

WWI Computer Room.

(R.E.Hunt) The results of a floor loading study are given in M-226. With certain rack arrangements the room is adequate; other arrangements might require some reinforcing. Levels were taken in the computer room. The total floor level differential is 3.6 inches. Sylvania has been given a rough contour drawing for use in designing levelling jacks for the computer bags.

2.0 WHIRLWIND I RESEARCH

2.1 Circuits

2.11 Flip-flop Design and Stability

(A.B.Horton, Jr.) Work is progressing on a suitable triggering method for the a-c flip-flop. A trigger circuit

consisting of a 7F8 double-triode seems to have promise and a 6SN7 could be used. This circuit receives positive trigger pulses on the control-grids and applies amplified negative pulses to the plates of the a-c flip-flop. At present, the trigger circuit operates the flip-flop upon receiving pulses of approximately 15 volts minimum amplitude. Work will be continued on this circuit.

The d-c accumulator flip-flop of the experimental multiplier digit has been replaced by an a-c flip-flop. The standard trigger-tube, buffer amplifiers, and neon-bulb driver were left intact. The a-c flip-flop operated satisfactorily under these conditions. Work will be continued as soon as the four-position crystal-matrix switch is replaced by a whiffle-tree switch. The panel layout for the whiffle-tree switch has almost been completed in the drafting room and construction will be begun as soon as possible.

W.P.Horton has begun preliminary work on testing the a-c flip-flop. Tentative plans have been made to construct a life-test rack.

2.13 Bus Drivers

(C.A.Rowland, Jr.) It has been decided to add a 7AD7 or 6AG7 buffer amplifier to precede the 6Y6 bus drivers. It is hoped that a satisfactory limiting circuit can be devised in the input of the amplifier preceding the 6Y6.

2.2 Components

2.22 Pulse Transformer

(G.S.Hoberg and C.A.Rowland, Jr.) A quantity of .001" x .25" hipersil ribbon has been ordered from Westinghouse for winding experimental cores of sizes and shapes which should permit better pulse transformer performance than is possible with commercially available cores. An appreciable reduction in size for given performance characteristics seems possible.

Experimental transformer 102B is thought to be applicable to the gate drivers in WWI. It has a 5:1 ratio and will work out of a 6Y6 into 47 or 93 ohm impedance levels.

2.23 7AK7 Tests and Specifications

(D.R.Brown) Dick Fallows and I were in Emporium on February 2 and 3. We were there to observe measurements of the 7AK7 characteristics on the Characteristic Curve Tracer. The characteristics were obtained at fixed control-grid and screen voltages; the plate voltage was swept over the desired range by superposition of a 60-cycle sine-wave voltage. The results obtained while we were there did not agree with data from static

measurements. Factors such as poor power-supply regulation and inadequate meters contributed to the disagreement.

Pulsed life tests, to be conducted at Emporium, were discussed. We will send circuit specifications and pulse equipment as soon as possible.

2.25 Tube Testing

(N.H.Taylor) We are enlisting the aid of some members of the Storage Tube Group to help us in studying the nature of the tube failures which have been found in 1500 hours of multiplier operation. This program will be started by measuring gas pressures in the tubes in question and comparing the pressure to that observed in new tubes. This program is being initiated after discussion with members of the Research Lab. for Electronics and Sylvania Electric Co., and the consequent lack of information which these parties were able to furnish us on tube deterioration.

Tube Investigation

(R.L.Ellis) Some investigation has been made on the labelling of tubes. Glass paint would not stick to the metal tubes. By experiment it was found Insulox #10 (aluminum) sticks well, will stand the heat and can be applied with a pen. The number at the base of the tube refers to the test records where the first or pre-tests can be found. The number at the top of the tube is the standardized, circuit assignment number.

Eighteen 6AS6 and 65 6AG7 tubes have been pre-tested and are ready for assignment to the multiplier digits.

A general check-up has just been completed on the tube tester.

2.3 Systems

2.31 Five Digit Multiplier

(N.H.Taylor) Multiplier operation has been resumed after a two-week period which has been used to change the power supply. The rotary equipment units now being used will allow much more quantitative testing to be carried on free from transients due to outside causes.

New matched pairs of 6AG7 pentodes have been placed in all flip-flop circuits. These will be tested periodically to check previous experience as to plate current decrease.

6345
Memorandum 237

Page 7

110 volt a-c line regulation is still a problem and it is hoped that this will receive prompt attention so that filaments will not be subject to the wide variations which occur during the night.

N. Daggett has started to study the multiplier circuits more quantitatively than has been possible in the past. He will make detailed studies of wave shapes, voltage levels, noise levels, and make the necessary changes in circuitry to obtain optimum performance.

One of the problems that remains unsolved if we are to make optimum use of the multiplier is that of counting the number of errors that occur in the solution of a given problem over a long period of time. At present it is necessary to view each solution then compare it with the known answer. This should be done automatically, and some record kept of the errors which occur.

(H.L. Ziegler) Though the installation of the motor-generator power supplies has been completed, no attempt is being made to keep the multiplier in continuous operation to continue the life tests. Instead of continuing the life tests, efforts are being made to improve circuit design and layout.

Use of the new power supplies has greatly increased the stability of the multiplier but errors are still being introduced by shifts in frequency of the Clock Pulse Generator. These frequency shifts have been observed to be due, at least in part, to line voltage fluctuations.

The Addition Control which was held up for several weeks because of circuit difficulties is now being tested.

(H. Kenosian) Final tests on the crystal-controlled clock circuit for the 5 Digit multiplier have been completed. Designs and recommendations for permanent auxiliary equipment have been submitted.

A 32:1 low frequency flip-flop divider has been installed to replace the G.E. Decade Sealing Unit for synchronizing the sweep of the synchroscope.

(N. Daggett) A waveform cleanup program has been started for the multiplier. The chief difficulty encountered has been getting circuits to perform properly with intermittent chains of pulses.

3.0 SPECIAL CIRCUITS

3.2 Test Equipment

3.21 Standard

(John O. Ely) Testing of breadboard models of

1. A multivibrator type delay circuit,
2. A phantasiron type delay circuit,
3. A cathode-coupled flip-flop with saw-tooth generator (to be used with pick-off diode in a delay circuit), and
4. A dual-pentode flip-flop with two gate tubes d-c coupled,

is proceeding.

Most of the testing to date has been done on item 4, the dual-pentode flip-flop. The original design did not provide enough gain around the loop so that a very unstable flip-flop resulted. Some time has been spent in adjusting this circuit and attempting to devise a simple method of testing its stability and response. Testing of the other three items has consisted mainly of checking circuits and static levels against design values. Rudimentary functional tests indicate considerable design adjustment on all three circuits to achieve operation which will be indicative of the suitability of the circuit for application to standard test equipment.

Tests have been made on 6 type 12L8GT dual pentodes to determine both cut-off voltage and plate and screen currents with the control-grid at cathode potential. These data are available to any interested persons.

Testing of the four breadboards listed above will continue.

3.22 Special

(H. Kenosian) Variable Delay Pulse and Gate Generator
The first of two of these units has been completed and is now in use. The second unit is now being checked.

Variable Frequency Clock-Restorer Pulse Distributor
The frequency divider section is nearly complete, and the distributor section has been laid out.

Single Pulse Synchronizer

An improved delay circuit is being installed in one of the units so that a greater range of delay can be realized. The improved circuit will make the delay independent of the amplitude and shape of the input wave form.

6345
Memorandum 237

Page 9

This unit was originally designed for a specific application which called for a minimum delay over a small range. However laboratory use has shown that a wider delay range is desirable for general applications.

Video Amplifier

(R.L.Massard) A single ended stage has been added to the input end of the amplifier, making a total of one single stage drawing three push-pull stages; the first push-pull stage acts as a phase inverter. The overall gain was increased and the hand width was not cut down by adding a stage to the input. The gain-frequency curves have in the past been inconsistent due to d-c wall supply variations, consequently regulated d-c supplies are being modified and put in to use. The bandwidth of the amplifier is 1/mc., but the phase-shift characteristic needs great improvement.

Special Test Equipment - Frequency Divider

(R.L.Best) The design of the frequency divider is completed and is available to anyone who wishes to have one made. It will sync to anything from clock pulses (1 - 6 mc) to 100 kc sync pulses, putting out a jitter-free pulse at a repetition rate of from below 500 cycles to 25 kc. The output pulse may be delayed over a 20 microsecond range in steps equal to the period of the original signal.

4.0 BLOCK DIAGRAMS

(E. Blumenthal) Block diagram revisions have continued. All that remains is work on bus connection diagrams, control functions, and timing of new orders. Progress on the first two must await more concrete information on electrostatic storage control, while the latter is dependent on the ultimate choice of the positions of the register number and operation code number within an order.