

UNCLASSIFIED
~~CONFIDENTIAL~~

PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 6
MARCH 1948

Submitted to the
SPECIAL DEVICES CENTER, OFFICE OF NAVAL RESEARCH
under Contract N5ori60
Project NR-720-003

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Cambridge 39, Massachusetts
Project DIC 6345

CONFIDENTIAL

TABLE OF CONTENTS

	Page
FOREWORD	1
Project Whirlwind	
The Whirlwind Computers	
Reports	
GENERAL STATUS	2
Time Schedules	
CONSOLIDATION OF OPERATION-TIMING AND PROGRAM-TIMING MATRICES	9
VACUUM TUBE LIFE AND FLIP-FLOP INSTABILITY	9
CHECKING OF BASIC CIRCUITS	11
STORAGE	12
Test Storage	
Electrostatic Storage Tubes	
MATHEMATICS	14
Polynomial Approximations for Known Functions	
Double-length Operations in WWI	
CONTROL DESK OPERATIONS	16
ACTIVITIES OF THE TEST EQUIPMENT COMMITTEE	16
TELETYPE PROGRAM	16
TROUBLE-LOCATION	17
Test Problems	
Power Distribution and Switching for Marginal Operation	
VISITS	19
Visitors to the Laboratory	
Visits by Project Staff Members	
APPENDIX	20
Reports and Publications	

This document contains information affecting the national defense of the United States within the meaning of the Espionage Act, 50 U.S.C., 31 and 32, as amended. Its transmission or the revelation of its contents in any manner to an unauthorized person is prohibited by law.

FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Special Devices Center of the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to The Special Devices Center, Office of Naval Research, Port Washington, Long Island, New York; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

GENERAL STATUS

Although much of the Project activity still consists of research and development, the construction stage has now set in: Sylvania Electric Products is building prototypes of numerous functional elements of the WWI computer.

Major emphasis of the Project has been the production of a working computer. Much research remains to be done on the utilization of high-speed digital computers, and a small staff of mathematicians has been working on problems of computer applications. The articles on Mathematics, page 14 of this report, describe examples of the investigations being made.

As described under "Tube Life" and "Checking of Basic Circuits", some fundamental aspects of the computer design are still matters of concern. Active programs are under way to examine these elements, and any improvements that are developed can still be incorporated in Whirlwind I.

Of basic importance to a large-scale computer is the memory element, which remembers, or stores, the numbers and the information with which the computer is working. The stored information may be either (1) program instructions, mathematical tables, or values of constants inserted before the beginning of a computation; or (2) interim results derived by the machine during the course of a computation. An article in the February report pointed out the important influence played by storage access time on overall computer speed. Development of the electrostatic storage tubes that will form the memory element of the Whirl-

wind Computers is showing satisfactory progress; construction of the first full-size tube is described on page 12. This tube was made to develop the glass-working, mechanical, and vacuum techniques required in full-scale tubes. It served this purpose satisfactorily. Emission of current from the holding gun is low, adversely affecting tests of the tube's storage operation. The storage surface is of calcium tungstate, not the metallized mosaic now being studied in the smaller research tubes.

Time Schedules

On the following three pages is a summary schedule covering Whirlwind I planning and construction. Posting to show progress of work follows the Gantt Chart method, which is described fully in The Gantt Chart by Wallace Clark, 1923, the Ronald Press, and the more recent Planning of Research and Development Work by Dwight L. Williams, Wallace Clark & Co., New York, N. Y. Explanatory notes will be found in the right-hand margin of each chart.

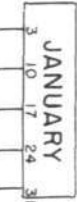
It will be seen that no schedule has yet been established for Storage Control Circuits or for Servo & Simulation Research beyond July 3, or for Input Keyboards and Output Printers beyond June 1. These three are items which are not required until after the initial installation and testing are in progress, and schedules will be established as soon as feasible.

Average delay behind the schedule is from one to two weeks. Notes indicate reasons for delays of special interest.

SUMMARY - WHIRLWIND I SCHED ULES

OPERATIONS	1948													
	MIT	S	JANUARY	FEBRUARY	MARCH	APRIL	MAY	JUNE	JULY	AUGUST	SEPTEMBER	OCTOBER	NOVEMBER	DECEMBER
TOTAL PROJECT STATUS														
17 A-REGISTER														
18 B-REGISTER														
17 ACCUMULATOR														
36 FLIP-FLOP STORAGE REGISTER														
18 FLIP-FLOP STORAGE OUTPUT														
34 BUS DRIVERS														
18 PROGRAM REGISTER														
13 PROGRAM COUNTER														
18 CHECK REGISTER														
18 INPUT-OUTPUT REGISTER														
18 COMPARISON REGISTER														
REPETITIVE UNITS TO BE BUILT BY SYLVANIA														
CONTROL SWITCH														
OPERATION TIMING CONTROL														
PROGRAM TIMING MATRIX														
TIME PULSE DISTRIBUTOR														
TIME PULSE DISTRIBUTOR CONTROL														
MASTER CLOCK														
FLIP-FLOP STORAGE REGISTER DRIVERS														
ARITHMETIC REGISTER DRIVERS														
INPUT-OUTPUT REGISTER DRIVERS														
NON-REPETITIVE UNITS TO BE BUILT BY SYLVANIA														
CONTROL SWITCH														
OPERATION TIMING CONTROL														
PROGRAM TIMING MATRIX														
TIME PULSE DISTRIBUTOR														
TIME PULSE DISTRIBUTOR CONTROL														
MASTER CLOCK														
FLIP-FLOP STORAGE REGISTER DRIVERS														
ARITHMETIC REGISTER DRIVERS														
INPUT-OUTPUT REGISTER DRIVERS														

LEGEND



PROTOTYPE

Period of one month comprising the total number of days in the month.

Operation to be performed and estimated time allotted for its completion. Estimates made in January 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

MIT	S
	✓

Column showing whether M. I. T. or Sylvania will do major portion of the job.

NOTES

C Changes in specifications have delayed this item.

S Studies and specifications still incomplete, principally due to lack of staff time.

CONSOLIDATION OF OPERATION-TIMING AND PROGRAM-TIMING MATRICES

Recent changes in the computer block diagrams eliminate the program-timing matrix and consolidate its function with that of the operation-timing matrix. This is possible because the program timing pulses were merely special cases of the more general operation timing pulses. The following is a more complete explanation for those who have studied Block Diagram Report R-127.

The control is the part of the computer which receives the operation order for a particular operation and then distributes to the other parts of the computer the proper sequence of pulses to carry out the operation. The heart of the control is a 32-position switch, called the operation switch, which translates the coded order into a "gate" at one of 32 terminals corresponding to the desired operation. This "gate" is used to pass pulses from the time-pulse distributor so that, during a particular operation, a pulse may be sent to a part of the computer at any one of the eight times within the time-pulse-distributor cycle. For example, during the operation *mh*, multiply and hold, a pulse which starts the multiplication is sent from the control to the arithmetic element at Time Pulse No. 1 (TP1). More than one operation may require that a pulse be sent to a given place at a given time. For example, the operation *mr*, multiply and round off, also requires that a pulse to start the multiplication be sent to the arithmetic element at TP1. Also, pulses at a given time may be required at different parts of the computer, either for the same operation or for different operations. For example, a pulse at TP1 is sent from the control to stop the pulses going to the time-pulse distributor during operations *mh* and *mr*. During operation *dy*, divide, a pulse is sent to the arithmetic element at TP1 to subtract the A-register from the accumulator. Also at TP1, for every operation defined, a pulse is sent from the control to clear the storage switch. Since this pulse is sent to the storage switch for every operation, the pulse need not be gated by the operation switch. Approximately 20 of a total of 80 pulses from the control are required for every operation and need not be gated by the operation switch. The interconnections to provide a pulse during a particular operation at the correct time are made in two large matrices called the operation matrix and operation-timing matrix (see the accompanying block diagrams). The connections to pulses at a particular time which need not be gated by the operation switch have been made in a smaller matrix called the program-timing matrix. The program-timing matrix provides the pulses required

during each cycle for all operations. These pulses actuate the program counter, which keeps track of the storage location of the next order; the storage, where the order is stored; the program register, which holds the order after it is read out of storage; etc.

In order to increase the flexibility of the Whirlwind I control, and to obtain the ability to suppress the pulses from the program-timing matrix for some future undefined orders, the program-timing matrix has been consolidated with the operation-timing matrix. Now all pulses from the control must be gated by the operation switch. This means that all the 20 pulses which came from the program-timing matrix are now gated by the operation switch for every defined operation.

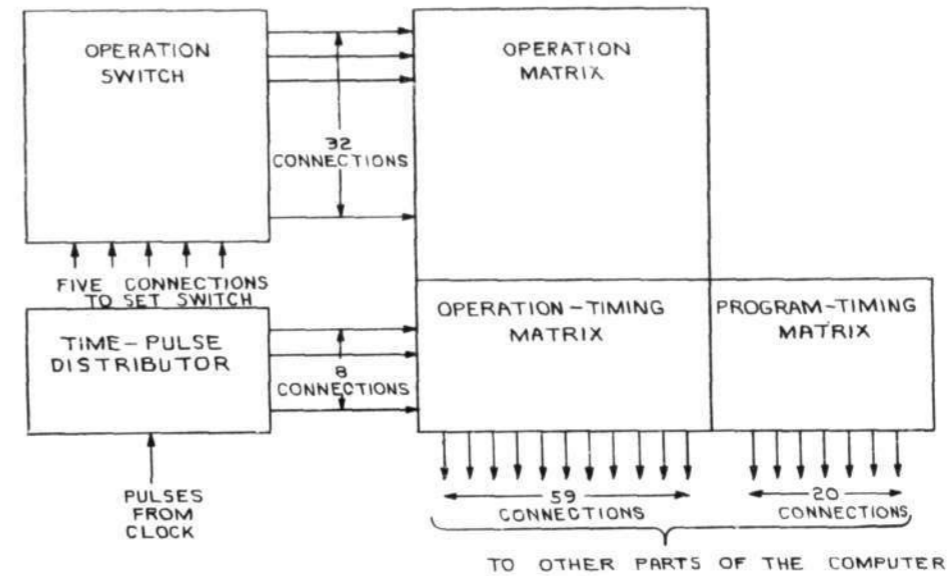
This scheme increases the physical size of the operation matrix and the operation-timing matrix, but eliminates the program-timing matrix and provides greater flexibility of the timing of the computer operations. A large number of spare channels will be provided which may be used for new orders.

VACUUM TUBE LIFE AND FLIP-FLOP INSTABILITY

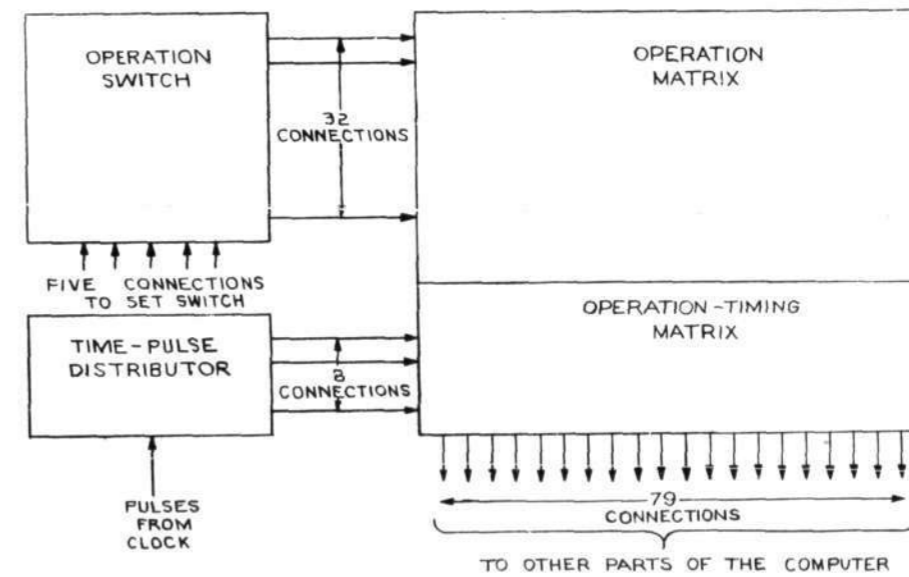
The reliability of the individual components of a large-scale computer is extremely important because of the large number of components employed. The failure of a single component may introduce an error in the result. Also, computation must be stopped so that the faulty component can be located and corrected. Vacuum tubes are far less reliable than other computer components, the average life of receiving-type vacuum tubes being of the order of 5,000 hours. Approximately 3,500 tubes will be employed in Whirlwind I.

A large number of diverse factors influence tube life. These include: mechanical failures such as interelectrode shorts, loss of emission due to evaporation of barium from the cathode, release of gas and consequent poisoning of the cathode, changes in contact potential, thermionic emission from the control grid, and others. The relative importance of these factors is difficult to determine, and will be different for different tube types and operating conditions. Mechanical failures occur suddenly and cannot be predicted. However, a large percentage of the mechanical failures occur during the first few hundred hours of operation. Mechanical failures in the computer can be reduced by preaging the tubes for several hundred hours before they are placed in the computer. Also, switching the heaters on and off is known to cause mechanical failures to occur more frequently. Switching of heater power will be held to a minimum in Whirlwind I.

CONTROL BEFORE CONSOLIDATION



CONTROL AFTER CONSOLIDATION



The release of gas from the internal parts of the tube will be inhibited if the temperature of those parts can be kept low relative to their temperature during exhaust. To minimize tube failures due to release of gas, thermionic emission from grids, etc., tubes in Whirlwind I will wherever possible be operated at less than half of the manufacturer's rated electrode dissipation. Tube life is undoubtedly closely related to cathode temperature. The rate of evaporation of barium from the cathode surface and repletion of the barium layer are functions of cathode temperature. Heater voltage will be carefully regulated in Whirlwind I in an effort to obtain constant and uniform cathode temperatures. Life tests are being conducted which will assist in determining the optimum heater voltage for each tube type.

Very little dependable information on tube life is available, particularly at the operating conditions encountered in electronic digital computers. Some data on tube life with the tube types and operating conditions to be encountered in Whirlwind I have been obtained from the five-digit demonstration multiplier and the flip-flop life-test rack.

Initial and final static characteristics have been measured on 52 type 6AS6 tubes and 64 type 6AG7 tubes which were operated in the five-digit multiplier for 1500 hours. The 6AS6 is a Western Electric miniature pentode with a sharp-cutoff suppressor grid; it is similar to the 6AK5. The 6AS6 tube exhibited an average decrease in static plate current of 8.6 percent in 1500 hours. In the multiplier, the control grids of the 6AS6's were biased below cutoff and pulsed at a low duty cycle by 0.1-microsecond pulses. The 6AG7 is a high-current, high-transconductance metal tube. The static plate current of the 64 tubes decreased an average of 44 percent during the 1500 hours. The 64 6AG7's were used under five different operating conditions. Fourteen tubes, used in flip-flops, with duty cycles of approximately one-half, exhibited a plate-current decrease of 33 percent. This was sufficient to cause some flip-flops to become unstable and behave as one-shot multivibrators, introducing errors in the computation. Seventeen 6AG7's with control grids biased below cutoff and pulsed with 0.1-microsecond pulses at a low duty cycle exhibited a plate-current decrease of 66 percent. These 17 tubes were operated under conditions very similar to the operating conditions of the 6AS6 tubes which decreased only 8.6 percent in plate current.

An investigation to determine the cause of the large percentage decrease in static plate current of the 6AG7 has led to some interesting observations. At the present time, measurements indicate the same explanation for all decreases in plate cur-

rent of 6AG7's. Numerous measurements on new 6AG7's and on the 6AG7's used in the multiplier show that the tubes in the multiplier have developed what appears to be a resistance in series with the cathode. At a cathode current of 30 milliamperes, the voltage drop across this resistance is approximately 1.2 volts in the tubes showing the most pronounced effect. Notice that the effect is most pronounced in tubes which are normally biased below cut-off. The reason for the apparent resistance is unknown. Among several explanations that have been offered are a voltage drop across the cathode interface and an effect upon the cathode caused by gas inside the tube.

Sixteen 6AG7 tubes have operated for 2000 hours in the flip-flop life-test rack and have exhibited an average plate-current decrease of 14 percent. After 665 hours of operation, two flip-flops became unstable. In one case, the instability was due to an abnormally high screen current in one tube, 22 milliamperes instead of the usual 10 milliamperes. In the other case, the instability was found to be due to a decrease in plate current of one tube from 27 to 19 milliamperes. At 1430 hours, two additional flip-flops became unstable. The instability was found to be due to a decrease in plate current of one of the tubes in each flip-flop. In one case the plate current had decreased from 27.5 to 16.5 milliamperes and in the other it had decreased from 26 to 16.5 milliamperes.

Certain modifications in circuit values are being studied to make flip-flops less sensitive to vacuum tube changes. At the same time tube life tests are being planned to provide better information on the relationship of computer circuits to tube performance.

CHECKING OF BASIC CIRCUITS

To prevent duplication of design efforts and to facilitate synthesis of computer systems, a set of diagrams for basic circuit types has been compiled. With whatever slight modifications as are dictated by particular applications, these basic gate tube circuits, buffer amplifiers, flip-flops, gate generators, etc., are being used throughout Whirlwind I design where their individual functions are required.

A program of investigation has been set up under which all of the basic circuits will eventually be given detailed performance tests. The results of the investigation will be used to establish specifications for each of the various basic circuits as regards values and tolerances of circuit parameters, supply voltages, and pulse shapes.

In addition it is expected that the tests will reveal unexpected faults in some of the circuits which may then be corrected by modifying the circuit or

modifying the operation of the computer. Tests will also provide a basis upon which to predict and evaluate the performance of the computer.

The investigation of the basic indicator circuit has been completed, and modifications to improve it have been proposed. This circuit is used to light small neon lights which indicate the position of a flip-flop. The brilliance of the neon lights varied from very dim to very bright over the range of pulse frequencies expected in the computer. The proposed modifications include a re-wiring of the neon lights and a positive bias on the tube that provides the current for the neon light. These changes will reduce the changes in light intensity with changes in pulse repetition frequency.

Investigation is also proceeding on the basic gate tube circuits. Data on this investigation are not complete, but it has been found that the impedance between the suppressor grid of the gate tube and ground is very important in that the output signal amplitude is inversely proportional to suppressor impedance. This is due partially to feedback through the plate-to-suppressor capacitance, but mostly to suppressor self bias. In other respects, gate tube performance has been as was expected.

Investigation of the basic flip-flop and basic bus driver circuits will be started in April. These tests are proceeding somewhat more slowly than had been expected because of the care that must be taken to obtain regulated independent power supplies, and to insure proper operation of all test equipment.

STORAGE

Test Storage

Electrostatic storage for WWI will not be available until after the arithmetic element and some other portions of the computer are completed and ready for testing. To facilitate interim tests, a small amount of non-electrostatic storage capacity is being provided. This memory element will enable the machine to carry out limited calculations which can be used as a basis for getting the rest of the computer into working order.

"Test storage" will consist of 5 flip-flop registers and 27 toggle-switch registers. The desired register will be selected by a 32-position matrix switch. Sixteen-digit binary numbers will be stored in these registers by manual operation of switches, and will be read out through gate tubes to other computer registers. In addition, the 5 flip-flop registers will be equipped with read-in gate tubes to permit acceptance of numbers from other registers of the computer.

These test-storage registers will be of value even when electrostatic storage becomes available and the computer is operating normally. They can be used for checking electrostatic storage, and will provide useful register capacity for a number of purposes for which manual storage of numbers is desirable. However, it will probably not be worth while to incorporate this type of storage in future machines for which electrostatic storage is immediately available.

Electrostatic Storage Tubes

The first large size (5-inch) electrostatic storage tube has been assembled and processed. (A 5-inch tube has a target nominally 5 inches in diameter.) This tube is similar in operation to the small research tubes previously constructed, having a high-velocity well-focussed electron beam for storing digits as spots of positive or negative charges on a storage surface and a low-velocity diffuse beam spraying the surface to maintain the stored charges. A wire mesh screen held closely in front of the storage surface acts as the collector of secondary electrons and a metal backing plate picks up the signal current by capacitive coupling to the storage surface. The constructional details of the 5-inch tube, however, are quite different because special methods must be employed to keep the wire mesh screen flat during the heating and cooling cycles encountered in the processing procedure.

Front and rear views of the storage assembly are shown in Fig. 1 and 2. The 40-mesh nickel wire screen, mounted on a nickel frame, is stretched over an outer support ring so that it is spaced 0.015 inch from the storage surface and held in tension by 18 tungsten cantilever springs. The construction is such that as the temperature cycles of the processing cause expansion and contraction of the wire screen, the tungsten springs keep a uniform tension in all directions. The storage surface itself is an anodized aluminum disc with a dielectric secondary-emitting surface of calcium tungstate added. The aluminum disc acts as the signal plate.

Fig. 3 shows the completed tube. The pyrex glass cylinder used for the body of the tube is 5-1/2 inches in diameter. The electron guns are mounted in separate 50-millimeter necks to provide shielding between guns. The overall length of this tube, 28 inches, will be reduced in later tubes, but no effort has as yet been made to package the unit efficiently. The large number of parts with their associated glass seals provide many gas sources and potential leaks. This tube was therefore subjected to very careful baking, r-f heating, and activation

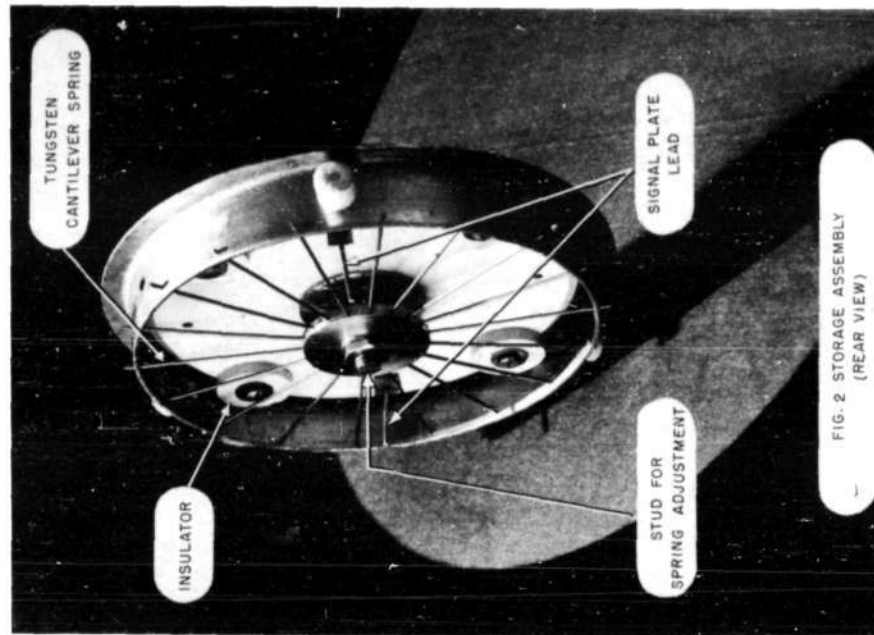


FIG. 2 STORAGE ASSEMBLY (REAR VIEW)

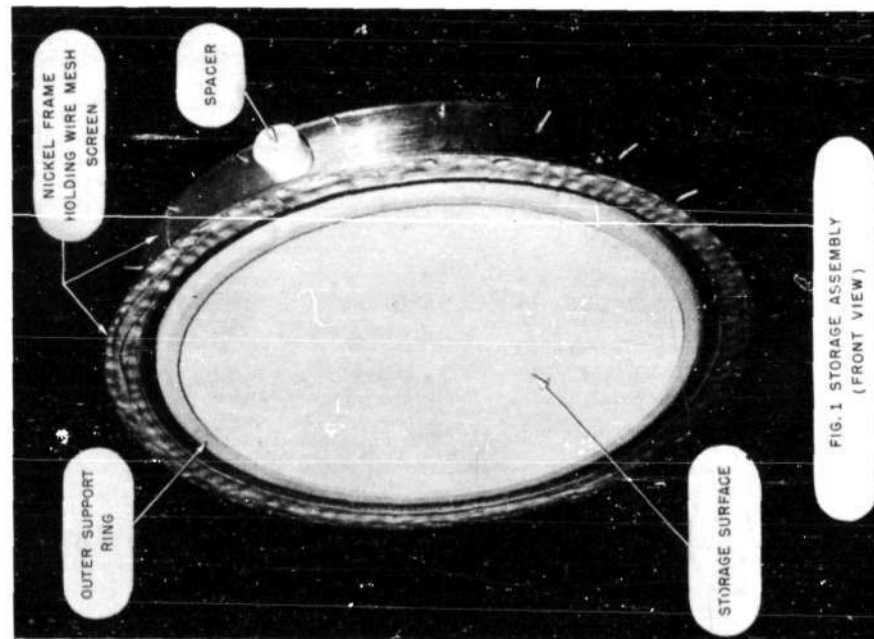


FIG. 1 STORAGE ASSEMBLY (FRONT VIEW)

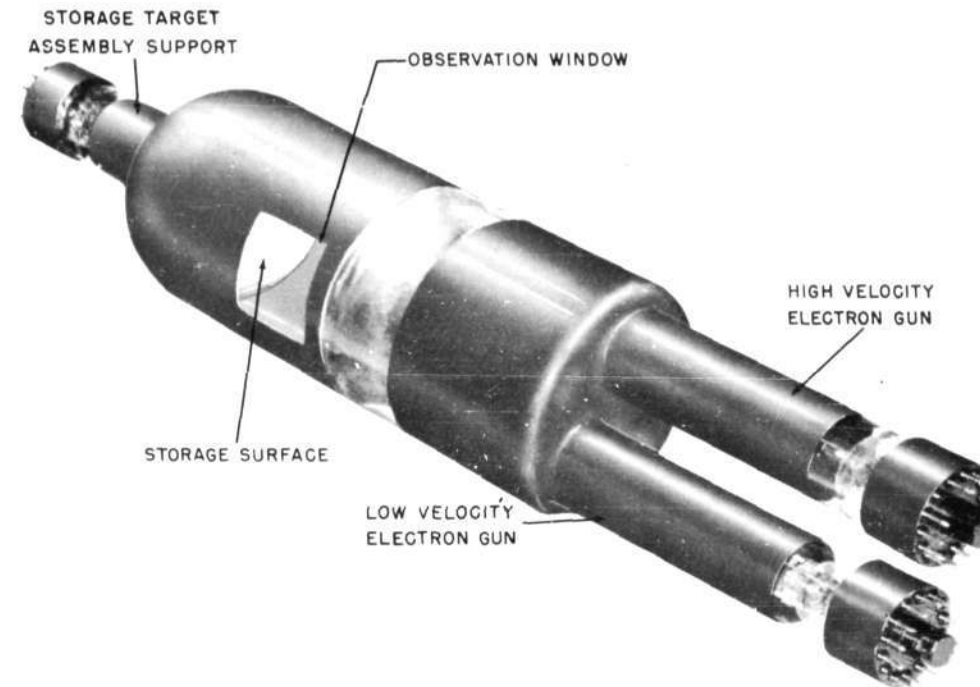


FIG. 3 FIVE-INCH STORAGE TUBE

to prevent gas contamination. The tube has not yet been tested but preliminary indications point to a good vacuum.

The calcium tungstate surface used in this tube is the same as that used in some of the earlier small tubes. Operation with this surface has been studied and found satisfactory for preliminary storage tube tests. Later tubes will use conducting mosaic surfaces to obtain greater stability and faster operation, but the calcium tungstate surface was picked for the first few 5-inch tubes because of the ease of construction and the visual indication provided by this phosphor.

Life tests on the secondary-emission characteristics of possible emitting surfaces are being conducted to determine the best material for use in the conducting mosaics mentioned above. A new type of research tube has been made to simplify the measurement of the secondary-emission characteristics and a life rack built for these tubes. For those surfaces with promising secondary-emission characteristics, several life test tubes will be constructed and tested. Half of these tubes will be aged with a low-velocity electron beam to simulate holding-gun operation, and the other half with a

high-velocity beam to simulate the reading and writing gun operation. Thus the effects of the two storage tube guns on secondary-emission life can be studied separately. It is also planned to measure the beam current in these tubes to gather life test data on our electron guns.

The tube construction program was materially aided by the addition of two new employees: Mr. William E. Pickett, an experienced glass and lamp worker, and Mr. Ingvar Paulsen, a mechanical technician who will design and make jigs and fixtures.

MATHEMATICS

Polynomial Approximations for Known Functions

The values of known functions, such as the trigonometric functions, exponentials, and natural logarithms, may be stored in "tables" in the storage element of a computer, or they may be calculated by polynomial approximations as they become needed. Of these two methods, calculation has the important advantage that it occupies much less storage capacity.

In problems requiring trigonometric functions, a preliminary step is the determination of the quadrant and sign, essentially reducing the angle to one in the first quadrant. If multiples of $\frac{\pi}{4}$ instead of $\frac{\pi}{2}$ are used, the problem reduces to the determination of $\sin x$ or $\cos x$, with x in the closed range 0 to 0.7854. For such values the ordinary Maclaurin's series for $\sin x$ and $\cos x$ to four terms give values correct to within 4×10^{-6} . The evaluation of such a series requires 4 multiplications and 4 additions, only a few more operations than linear interpolation; and in place of 900 items for functions at intervals of tenths of degrees, we need store only 8 coefficients.

For inverse sines, the polynomials described above may be solved by Newton's method of approximation, using as the first approximation for $\sin^{-1} x$ the two terms $x + \frac{x^3}{6}$. For $\cos^{-1} x$, $\sqrt{2-2x}$ may be taken as the first Newton approximation for x in the closed range 0.7 to 1.

For the exponential function, the factor e^x may be calculated from its series with five terms to within 8×10^{-6} for x in the closed range -0.25 to 0.25. This may be combined with values for -0.5, 0.5, and those at intervals of unity, tabulated and stored, to produce all values by two multiplications. Again, for finding natural logarithms a few of these stored values and $\ln 2$ may be used to reduce the situation to finding $\ln x$ for x in the closed range 0.75 to 1. This may be done by Newton's method and the exponential polynomial, starting with $-\ln x = 3/2 - 2x + x^2/2$ as a first approximation.

For the inverse trigonometric functions in limited ranges, small fractions of a quadrant, or for $\ln x$ in limited ranges, a single approximating polynomial of low degree is possible. This is also true of smooth empirical functions if the problem involves them only in a relatively small range.

Double-length Operations in WWI.

In any extended computation, the error resulting from rounding off products and quotients at each step accumulates and can become large enough to make the results inaccurate or even useless. The only way to reduce this error is to carry more significant digits through the computation. By using two registers to store each number (for instance the number 12345678 could be stored as 1234 in one register and 5678 in the next register), the number of significant digits carried can be doubled and the accuracy therefore very greatly improved. If still greater accuracy is required 3 or more registers can be used.

The arithmetic element of the Whirlwind computer can operate on only one register length at a time, but by a suitable combination of single-length operations, any desired operation can be performed

on double-length numbers, yielding double-length results. In a similar manner operations can be performed with numbers whose lengths are any multiple of the computer register length. Since the number of orders required to carry out a double-length operation is in many cases quite large, subprograms are used to eliminate the need for repetition of the orders each time the operation is to be performed.

By a subprogram is meant a program or sequence of orders designed to carry out one frequently repeated operation (e.g. addition of two double-length numbers). This program is stored in some one position in storage. Whenever the program is needed in the course of the computation, the coder needs only to shift control from the main program to this subprogram by means of a suitable order and to have control returned to the main program at the end of the subprogram. In this fashion repetition of the sequence in the main program, which would be both tedious and wasteful of storage, is avoided.

Each time the subprogram is to be used, the numbers of the storage registers from which the numbers to be operated on are to be taken and to which the result is to be sent must be inserted into the subprogram by the computer itself, since the numbers will be different each time. A group of five automatic subprogram orders (as, ax, ay, az, ro) were included in the WWI control so that the heaviest part of the burden of this insertion process can be carried out in the subprogram, thereby minimizing the orders required in the main program. These special orders were provided to compensate for the short (16 binary digit) register length of the WWI computer which was selected to limit the size of this prototype machine.

By means of these automatic-subprogram orders in conjunction with a group of suitably written subprograms, the basic double-length operations of addition, subtraction, and multiplication can be ordered as easily and with as little storage as the corresponding single-length operations. The computing time is of course materially increased due to both the increased complexity of the operation and the need to insert new register numbers in the subprogram each time. Coding of subprograms requires about 20 storage registers for addition or subtraction, 50 for multiplication, 90 for division. Computing time for the operations will be increased over corresponding single-length operations by estimated factors of about 7.5 for addition and subtraction, 15 for multiplication, 25 for division.

These factors can be substantially decreased by slightly increasing the allowable roundoff errors in the double-length computation, thus decreasing the required number of single-length operations, or by

doing all or part of the computation in the main rather than the subprogram. This latter method can reduce the time factor to as little as 2 for addition and 6 for multiplication, but at the expense of a considerable increase in main program orders which occupy additional space in storage. Computations with numbers three or more registers in length require correspondingly greater times.

Control, order modification, indexing, and other "red tape" operations can still be done with single-length numbers. Since these operations form the bulk of most automatic calculation, particularly in control problems, the increase in computing time due to the use of double-length quantities is not as severe as it might first seem. The factor might be of the order of 5 for calculations using all double-length numbers, and from 2 to almost unity for control problems where only a very few quantities need be double-length.

Storage of double-length numbers requires twice as many registers as are needed for single-length numbers. Since the operations require about the same number of orders in the main program (for automatic subprograms) as do single-length operations, plus permanent storage of the subprograms, complete double-length computation will probably reduce the effective storage capacity of WWI to a little over half of normal. The reduction will be much less for control problems.

CONTROL DESK OPERATIONS

At the control desk of the computer will be consolidated, in addition to the circuits required for normal operation, controls for trouble location and for marginal checking. Preliminary conferences in March outlined the control desk functions.

To aid in preliminary operation and installation and later for trouble location, pushbuttons on the console will permit manual selection of any of some 150 control pulses in the computer. These pulses, available individually or in combination, can be used to produce many arbitrary checking routines in addition to all sequences found in the normal computer operating orders.

For inspection of the computer while it is operating at high speed, a coincidence pulse system is being planned. The nature of the computer cycling is such that any arbitrary step in a long sequence of computation (for a test problem without undetermined subprogram operations) can be identified by the simultaneous setting of the program counter, the time-pulse distributor, and the step counter. Coincidence counters at the console will permit selection of such an arbitrary step; the operator has a choice of computer responses when this step occurs:

- 1) A trigger pulse can be obtained to permit observation of behavior of computer circuits on a synchroscope.
- 2) The computer can be stopped to permit reading of numbers in registers.
- 3) The contents of any register can be transferred to the output and automatically checked against a preset correct value.
- 4) The preceding check can be made and the computer restarted at the beginning of the test problem.

This fourth mode of operation permits repeating and checking solutions in searching for an intermittent fault.

Plans for the automatic variation of selected supply voltages as mentioned in Summary Report No. 3 are nearly complete. Either manual or automatic cycling of voltage variation on each supply circuit will be available. Up to 200 such circuits are being provided initially. It is anticipated that after the marginal checking system has been studied in actual operation, this degree of flexibility will not be required in future computer designs.

ACTIVITIES OF THE TEST EQUIPMENT COMMITTEE

Four members of the Project staff, drawn from different divisions, have formed a committee to coordinate the test equipment program for the Project. Their duties include approving and scheduling the purchase and construction of all laboratory test equipment, both for preliminary investigations and for trouble-shooting and maintenance of WWI. They are also responsible for planning an adequate future program, foreseeing and meeting the Project's increasing needs.

The Project uses large quantities of special test equipment that is not commercially available. Examples of such test equipment are:

Gate and Delayed-Trigger Generator - a unit which generates an output pulse at an adjustable time after receiving an input pulse. The unit will also generate a gate of arbitrary length. A sufficient quantity of these units will produce any desired arrangement and sequence of pulses and gates. They are widely used for controlling WWI elements during design and test.

Register Panel - a flip-flop and two gate tubes with trigger tube and output buffers, multiple inputs on grids and cathode, indicator lights, and very flexible connections. It can be used for counting, synchronizing, pulse distribution, and system mock-up.

There are many others, such as pulse generators (clocks), single-pulse synchronizers, binary

counters, frequency dividers, video amplifiers and probes, mixers and coders, and much special-purpose one-of-a-kind equipment. The utility of such equipment is greatly reduced unless the various units are designed to work together and are available in such diversity and quantity that the bulk of the Project test work can be done using equipment already at hand.

The committee is also responsible for coordinating the procurement of test equipment for WWI production test at Sylvania Electric, including tube testing and preaging.

TELETYPE PROGRAM

Present plans are to use teletype equipment for printing final results and possibly for input typewriter use. Teletype tape would not always be used, the units sometimes transmitting directly to or receiving from the computer film reader-recorders. There are two major reasons for the choice of such equipment.

1. Teletype equipment is commercially available and requires no development work. The equipment for connecting it to the film reader-recorders is very similar to that used for connecting the computer to the film units. Teletype appears to have satisfactory characteristics, at least for present requirements. More elaborate printing and input typewriter devices may be developed later when engineering time is more available.

2. One of the best possibilities for the effective use of a computer by a group not at the computer location lies in teletype communication. The distant group would prepare their problems including detailed coding and transmit the information to the computer by teletype. There it would be stored temporarily on tape or film until computer time became available. Computer results would be recorded on film and sent to the originator by teletype at leisure.

No modification of the teletype equipment is planned. Information will be transmitted or received in standard 5-pulse teletype code. The computer will first convert this code to some more orderly one, perhaps 4-digit binary-coded decimal, and then into 16-digit binary. The reverse process will be used for results to be printed. The conversion load on the computer is not great. Conversion can be made as fast as information can be transferred from the film reader. Machine orders, spaces, carriage return, punctuation, will be put into the computer in standard code from the input tape and properly distributed to the output tape under the control of the computer. In this way, headings and page composition of the computer results will be controlled by the computing program as in-

initially prepared.

TROUBLE-LOCATION

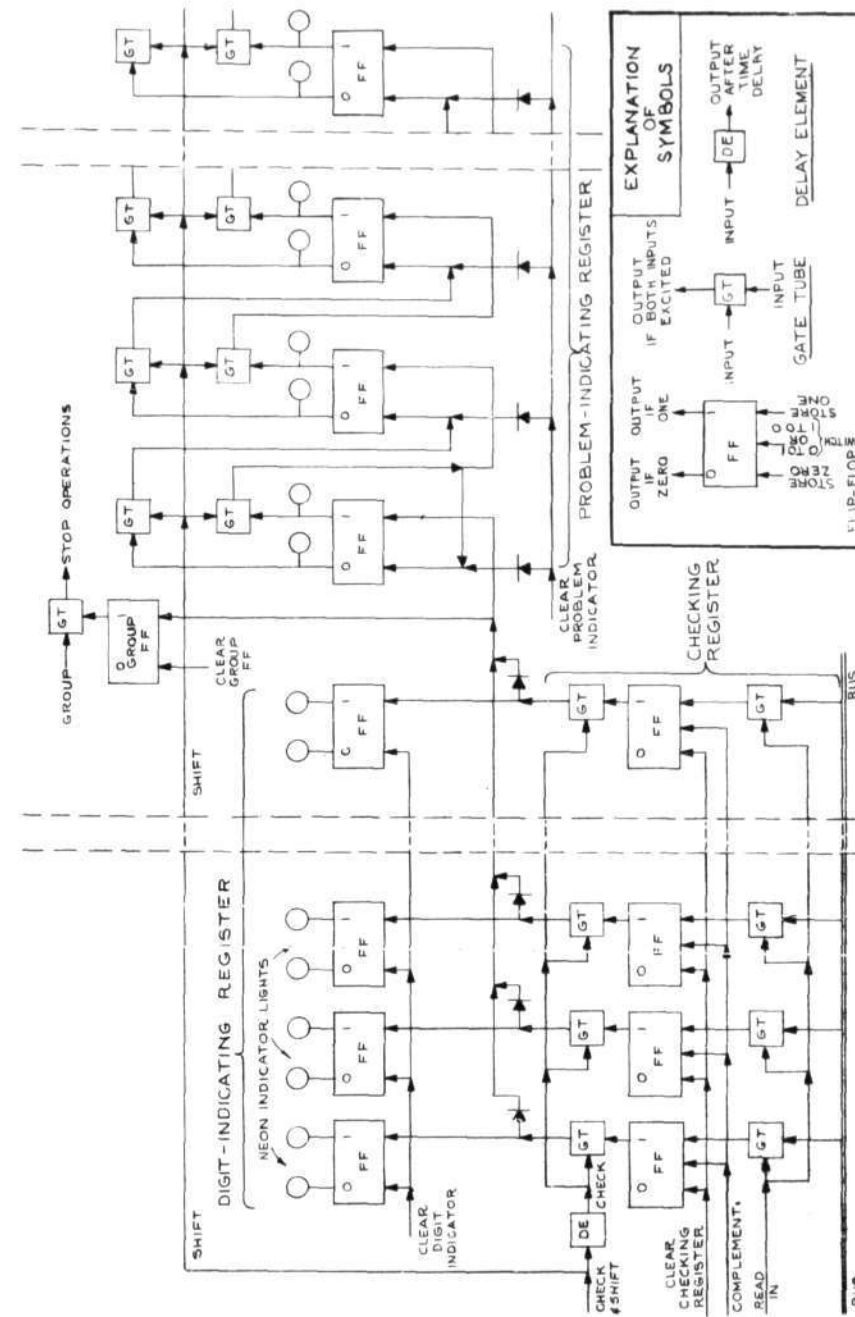
Test Problems

Two staff members have been working on the design of an automatic method for finding the location of an equipment fault in the arithmetic element of a computer such as WWI. The method assumes that the computer control and input devices are working, that the effects of the fault do not vary with time during the checking process, and that only one portion (considered as a unit for checking purposes) of the arithmetic-element electronic apparatus contains a fault at any one time. Although at first these assumptions appear unduly restrictive, it is believed that this method will have great value in increasing the usefulness of the computer by reducing maintenance time.

It is proposed that the arithmetic element be instructed by control to solve a specially prepared list of so-called trouble-location problems provided by the input device. Comparison of the response to the various required operations with what is known to be the correct response would then provide information indicative of the nature and location of the fault. These trouble-location problems will be used only after the incorrect solution of a check problem sequence has established that a fault exists in the machine.

A functional diagram of a system for automatically utilizing information obtained from trouble-location problems is shown on the following page. The machine operations are coded and performed so that if a 1 ever exists in the checking register when a "check" pulse occurs it indicates an error and a 1 is stored in one or more of the flip flops of the digit-indicating register, and also in the leftmost flip-flop of the problem-indicating register. "Shift" pulses move the contents of the problem-indicating register one space to the right each time a check is made. When a group of problems has been completed, a "group" pulse ascertains the contents of the "group FF", which will contain a 1 if any error has been made.

If the "group" flip-flop does not contain a 1 when the "group" pulse occurs, the next problem group of the sequence is run off. If it does contain a 1 when its gate tube is pulsed, operations will be stopped. The neon lights on the digit-indicating register will then be a coded representation of the digit column in which a failure occurred. The lights on the flip-flops of the problem-indicating register will show to which problems of the group being considered the arithmetic-element response was



incorrect, and will thus be a coded representation of the nature of the failure. Reference to a code book by the operator will then provide an interpretation of this information in terms of the physical location of a fault in the computer.

In addition to the equipment shown on the drawing, an electronic counter will be required to count the number of "group" pulses. The binary number contained in this counter when operations are stopped will then indicate the problem group in which an error was made evident. While this information could be supplied to the output typewriter, it is questionable whether the convenience so afforded justifies additional code-changing equipment.

When used in conjunction with techniques (see the following section) for varying circuit voltages and pulse-repetition frequencies to make intermittent faults caused by marginally operating components appear like steady-state faults, the proposed system should prove of value for locating intermittent as well as steady-state faults.

This trouble-location scheme has not yet been evaluated sufficiently to justify a decision as to its inclusion in WWI.

Power Distribution and Switching for Marginal Operation

A system for checking for failures under marginal operating conditions is being developed. This system will allow the plate, screen, and bias voltages of groups of tubes to be varied above and below their normal values to determine if such variations will produce an error in a cyclic test problem being run by the computer. To facilitate such marginal checking the d-c power to each register will be distributed through a number of voltage-variation panels each of which supplies one d-c voltage to the tubes having the same function within the register. These voltage variation panels contain relays for inserting a variable-voltage generator in series with the supply line passing through that panel; they also contain controls for setting the upper and lower limits on the voltage excursion to be produced in that line. Selection of the particular voltage-variation circuit in series with which the variable voltage generator is to be inserted will be accomplished by a selective switching circuit employing a telephone type cross-bar switch. The cross-bar switch that has been obtained will allow any one of 400 panels to be chosen. The control circuits will provide for three types of marginal checking: (1) selection of panels in an automatic sequence by use of rotary switches producing an automatic voltage-variation cycle at each

panel, (2) selection of panels by manual switches after which an automatic voltage-variation cycle occurs, or (3) manual panel selection and manual voltage-variation control. An arrangement of time-delay relays and relay interlocks is intended to prevent the introduction of transients into the computer circuits by any switching process. The check-problem sequence to be solved by the computer will be completed many times during a single voltage-variation cycle. If an error is produced at any time during the check, automatic sequencing will be stopped and an indication of failure will automatically be provided to the operator. The prepared sequence of trouble-location problems (see preceding section) will then be run off in an attempt to ascertain the location of the failure.

To date, work has been done on formulating the requirements of a marginal checking system, personnel have been assigned to design the electrical and mechanical layouts, and preliminary proposals on these designs have been written.

VISITS

Visitors to the Laboratory

Dr. Alston S. Householder and Dr. George Garrett, representing the Division of Carbide and Carbon Chemicals Corporation at the Oak Ridge National Laboratory, came to MIT to discuss availability of digital computing equipment. Since their computing requirements will initially be limited, the recommendation was made that, after proper arrangements, a representative be sent to MIT next fall to study Whirlwind equipment for a few months. This might be followed by their use of the WWI computer at MIT and by remote use from Oak Ridge via teletype connection. Complete computing equipment could later be installed at Oak Ridge when it becomes necessary.

Colonel Carl Swyter and Eugene F. Grant of the guided missile branch of the Air Forces discussed application of Whirlwind equipment to their field of interest.

Visits by Project Staff Members

During March MIT staff members attended technical conferences on input-output devices at Eastman Kodak and on vacuum tubes at the Emporium plant of Sylvania. Three men attended the conference of the AIEE at Philadelphia on long-life vacuum tubes; and at the IRE National Convention Mr. David Brown presented a joint paper with Mr. Nathaniel Rochester of Sylvania on multi-position germanium crystal rectifier switches.

APPENDIX

REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were issued during March.

Report R-122, Low-Power Pulse Transformers, being of interest to workers in the computer and pulse-circuit fields, was reproduced by photo-lithography and given wider circulation than is usually accorded to Project reports.

No.	Title	No. of Pages	No. of Dwgs.	Date	Author
SR-3	Summary Report No. 3			12-47	
R-122	Low-Power Pulse Transformers	69	62	12-47	T. F. Wimett
E-103	Ion Current Measurements in 7AK7 and 6AG7 Tubes	3	9	2-20	M. H. Hayes & J. J. O'Brien
E-104	Basic Circuits	5	13	3-5	J. A. O'Brien
E-105	Power Requirements for WWI	3	3	3-9	H. S. Lee
E-106	IN38 Germanium Crystal Diode Rating Tests	4	-	3-8	R. L. Ellis
E-107	Consolidation of Operation Matrix and Program Timing Matrix	2	-	3-24	J. A. O'Brien
M-217	Description of Whirlwind I Codes	13	-	1-22	C. W. Adams
M-243	Proposal for Deflection-Circuit Development	5	1	2-17	J. O. Ely
M-251	Standards Committee Meeting on Power Connectors	2	-	3-2	H. Fahnestock
M-252	Proposal for Investigation of Storage-Tube Output Circuits	3	1	3-3	C. Campling
M-259	Lock-In Tube Sockets	1	-	3-4	J. W. Forrester
M-262	Power Supplies and Distribution Conference	3	1	3-4	J. W. Forrester
M-264	Eastman Conference, March 2, 1948	3	-	3-5	H. R. Boyd
M-267	Bi-Weekly Report, Part I, March 5	14	-	3-5	
M-268	Bi-Weekly Report, Part II, March 5	14	-	3-5	
M-271	Progress Report: High Speed Pulse Recording on Magnetic Tape	6	1	3-6	E. S. Rich
M-273	Creep Test of 5" Anodized Storage Surface	2	1	3-10	R. Shaw
M-274	Crystal-Rectifier Requirements	1	-	3-10	D. R. Brown
M-276	Tube Construction and Test Program of the Storage Tube Group	9	-	3-1	(S. H. Dodd (W. J. Nolan (P. Youtz
M-285	Power Supply Proposal No. 1	2	-	3-12	H. R. Boyd
M-287-1	Project Whirlwind Seminar Schedule March 10 - April 14	1	-	3-16	R. R. Everett
M-289	Progress Report: A Storage Tube Output System	3	-	3-13	C. Campling
M-290	Holding-Gun Research Tubes	3	-	3-15	M. Florencourt
M-292	Requirements for Voltage Variation Panels	2	-	3-16	C. W. Watt
M-293	Meeting of Electronic Group, Mar. 5, Design Problems of Arithmetic Element Control	2	1	3-16	G. C. Sumner
M-294	Proposed Panel-Selection Circuit	4	1	3-16	E. S. Rich
M-295	Investigation of 7AK7 Processing, Emporium, Pa., Mar. 2	2	-	3-16	D. R. Brown
M-299	Whirlwind I Heater Grounds	1	-	3-17	H. Fahnestock
M-302	Quantity of Aluminum Channel Required for WWI Installation	1	-	3-18	C. W. Watt

<u>No.</u>	<u>Title</u>	<u>No. of Pages</u>	<u>No. of Dwgs.</u>	<u>Date</u>	<u>Author</u>
M-303	Photographs of Storage Tube Assemblies	2	-	3-18	M. Florencourt
M-304	Whirlwind I Standards: Construction of Test Equipment	1	-	3-19	H. Fahnestock
M-305	Progress Report: A Trouble Location Scheme for a Digital Electronic Computer	2	-	3-18	(G. Hoberg (E. Blumenthal
M-306	Overloading of Neon Indicator Lamps in Basic Circuit IND-1	4	5	3-22	J. Hunt
M-310	Bi-Weekly Report, Part I, March 19	22	-	3-19	
M-311	Bi-Weekly Report, Part II, March 19	20	-	3-19	
M-312	Power Cabling, Proposal No. 1	3	3	3-26	H. S. Lee
M-313	Proposed Elevating Test Truck for WWI	3	2	3-23	R. E. Hunt
M-314	Connections and Changes on Basic Circuits BA-1 and GG-1	1	2	3-23	J. A. O'Brien
M-317	Progress Report: High Speed Pulse Recording on Magnetic Tape	3	-	3-19	E. S. Rich
M-318	Progress Report: Investigation of Electronic Computer Output Circuits	1	-	3-20	F. Foss
M-319	Arithmetic Control and AC-0 Preliminary Notice of Work Load	2	-	3-24	H. Fahnestock
M-320	Pulse Transformer Test Unit	1	-	3-24	R. Everett
M-321	Meeting of the Electronics Group, March 12 and 19, 1948	1	-	3-25	J. J. O'Brien
M-322	Additional Voltage Requirements for WWI	1	-	3-26	C. W. Watt
M-324	Filament Transformers, WWI	2	-	3-26	(J. Forrester (H. Fahnestock
M-326	WWI Rack Door Material	1	-	3-31	R. E. Hunt
M-327	Arithmetic Control Time Schedules	1	-	3-31	H. Fahnestock
M-330	WWI Control: Time Schedules	2	-	4-1	H. Fahnestock
M-333	Progress Report: Investigation of Electronic Computer Output Circuits	2	-	3-31	F. Foss
<u>Translation</u>					
M-225	Theory of Secondary Electron Emission from Metals -H. Frohlich (ANNALEN DER PHYSIK, 1932, Series 5, Vol. 13, p. 229)	5	-	2-2	M. Florencourt