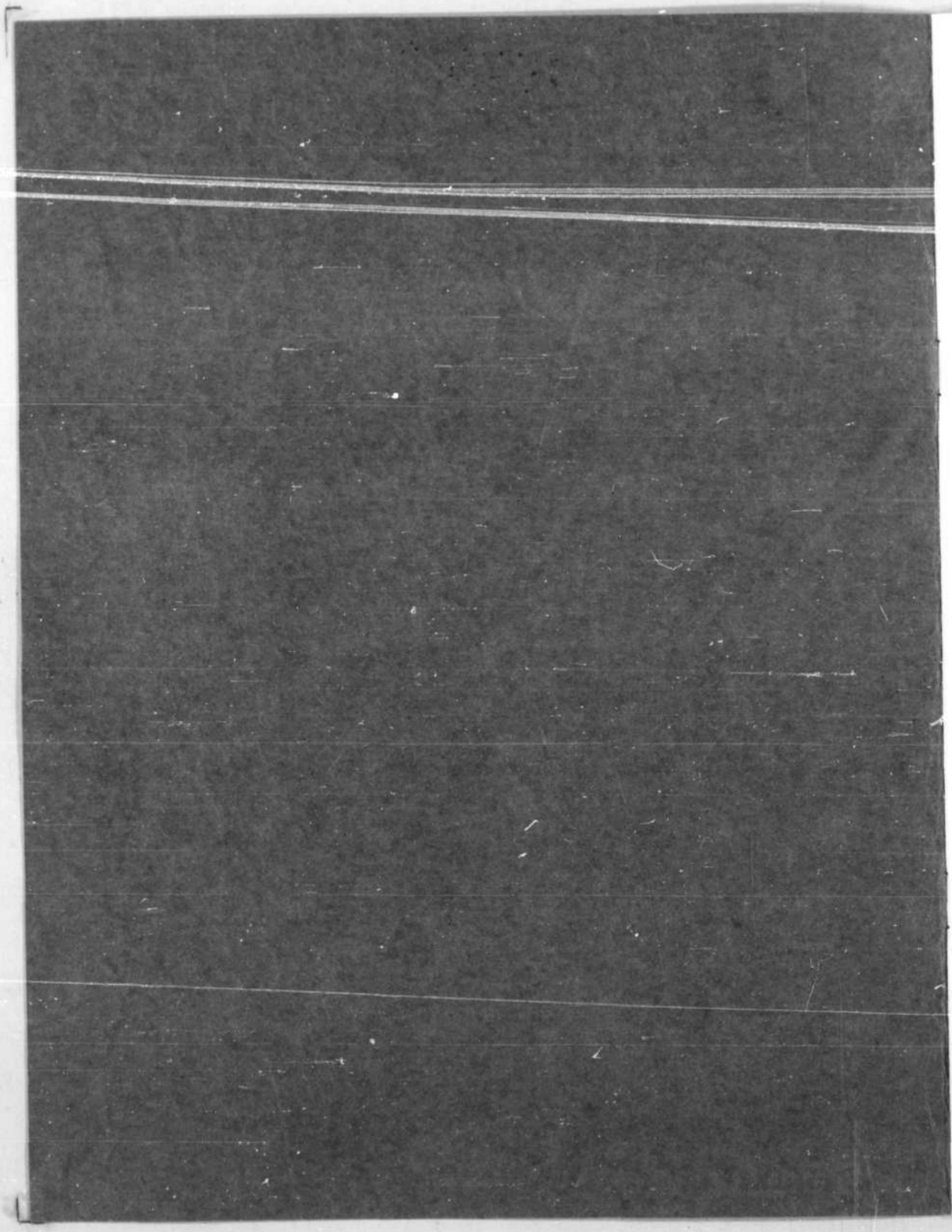

CONFIDENTIAL

PROJECT WHIRLWIND

(Device 24-x-3)

SUMMARY REPORT NO. 16

JANUARY 1949

Submitted to the

OFFICE OF NAVAL RESEARCH

Under Contract N5ori60

Project NR-048-097

SERVOMECHANISMS LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Cambridge 39, Massachusetts

Project DIC 6345

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FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to design of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being developed, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I will use numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Five special orders expedite the subprogramming of multiple-length operations, so that coding is no more complicated than for single-length numbers, but computing time is substantially increased. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of monthly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of publications issued during the period covered by this Summary appears at the end as an appendix. Authorized personnel may obtain copies of any of them by addressing a request to the Office of Naval Research, Navy Department, Washington 25, D. C.; or where approval has previously been arranged, to Jay W. Forrester, Project Whirlwind, Servomechanisms Laboratory, Massachusetts Institute of Technology, Cambridge, Mass.

GENERAL STATUS

The arithmetic control and all units of the arithmetic element have been installed. During January the equipment functioned properly on multiplication and shifting operations. Other arithmetic operations will be checked in February.

The fourteenth beryllium-on-mica storage tube was completed and several are now on life test. Some tubes have operated several hundred hours without significant changes in characteristics.

The semiannual revision of time schedules appears in this report. The new summary has been reduced to one page and does not show as much detail as previously. It is believed this will be more useful to the reader. The summary, as before, will be posted from sheets showing full detail. So far as is known, this summary now covers all components and all research and development required to make WWI ready for preliminary operating tests. Only one of the two banks of storage tubes is included for the initial test period. Because major research questions have been answered, the detailed schedules are now extended to the final assembly of the Whirlwind I computer. This date, which is estimated about February 15, 1950, represents an earlier completion of that phase of the project than shown in the Long Term Whirlwind Schedule in Summary Report No. 11 for August 1948. The reduction in estimated time results from more rapid progress on storage tubes than was expected and from a more detailed analysis of the work remaining.

A final posting of the July-through-December schedules is included in this report for comparison with the new schedule. The new schedule is based on a study of each part of the computer yet remaining to be completed and on an estimate of the man-weeks of staff time, construction, drafting, and installation which each will require. These estimates are more complete, and it is expected somewhat more accurate, than those for the last semiannual period. The latter were in error by about one part in six - that is, work estimated for completion at the end of December was completed at the end of January.

The new estimates assume the present Project Whirlwind personnel and make a complete allocation of all available time. In general, the completion dates are set by man-hours for available design and construction, not by the research status of the jobs. As design and construction on different parts of the equipment are finished personnel will be transferred to installation and test.

INSTALLATION AND TESTING OF WWI

During January, installation of the arithmetic element progressed to the point where trial performance of arithmetic operations was possible. After integration of test control and arithmetic control with the A-register, B-register, and accumulator, multiplication of two arbitrary 15-digit binary numbers was successfully carried out first step-by-step at a push-button rate, then cyclically at the normal 2-mc prf (maximum time required = 25 microseconds per multiplication). Division was also performed successfully in a step-by-step manner, with promise of high-speed operation within a short time.

These accomplishments represent a significant milestone. Although WWI computing techniques had been shown feasible by the Demonstration Multiplier (see Summary Report 3), the work of the past month has now proved conclusively that the arithmetic element is capable of functioning as required in WWI.

The relatively short time required for achieving successful multiplication demonstrates the effectiveness of the testing which had been carried out on each individual panel of the arithmetic element. (See Summary Report 12.) Preliminary tests on the system were also of much value. When interconnection of panels was first begun last month, two parallel test programs were set up. After the panels were installed and power was made available, one systems group worked on the repetitive elements of the principal registers, while a second group worked on test control and its interconnection with WWI arithmetic control. High-speed multiplication

continued on page 12

SUMMARY - WHIRLWIND I SCHEDULES

LEGEND

JULY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

MIT	S
	✓

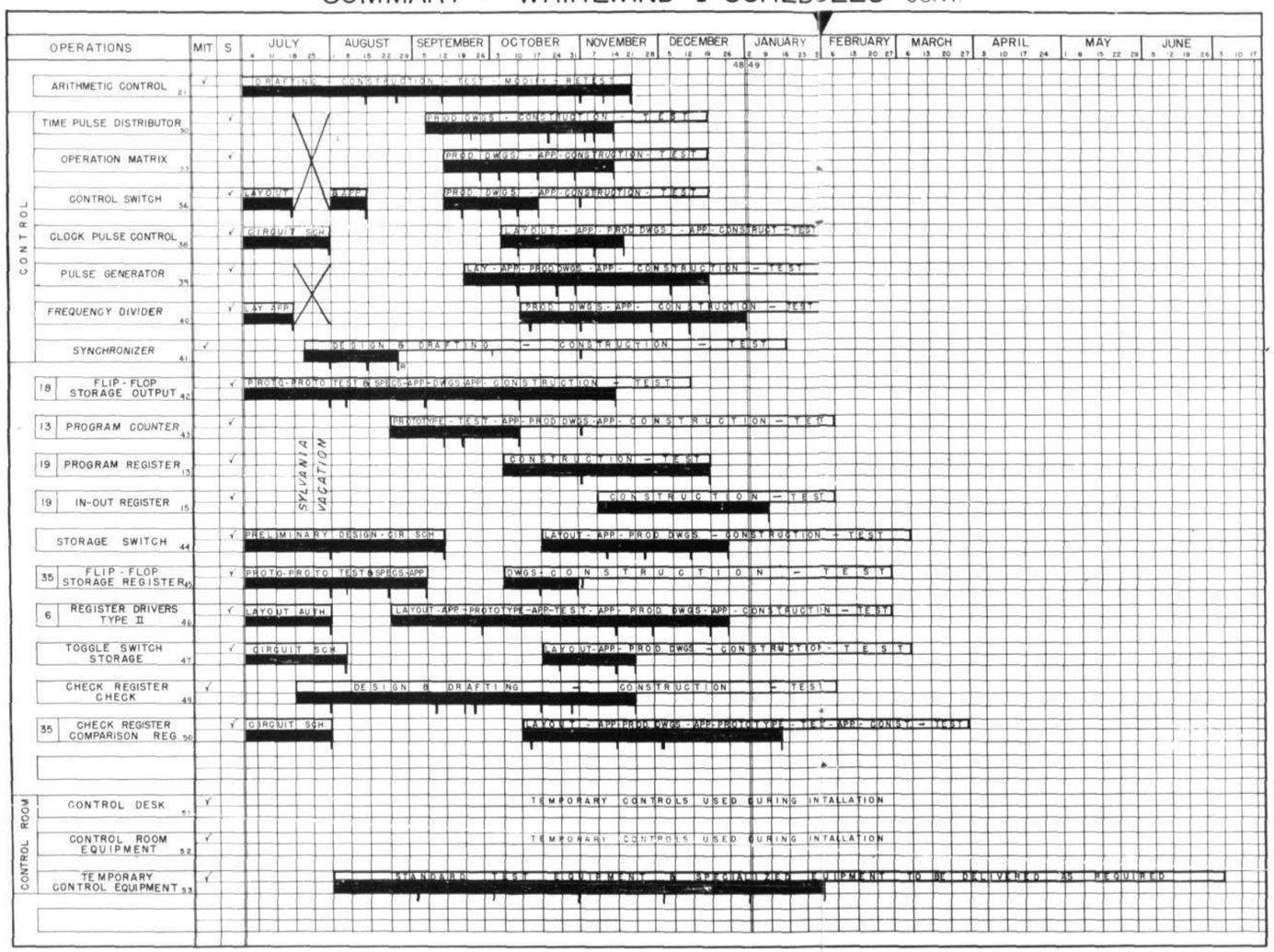
Column showing whether M.I.T. or Sylvania will do major portion of the job.

NOTES

R Revised schedule does not call for same completion date as originally planned.

For a long-range plan from 1944 to 1952 showing the relation of this detailed schedule to past and future work, see Summary Report No. 11, August 1948.

SUMMARY – WHIRLWIND I SCHEDULES CONT.



LEGEND

JULY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

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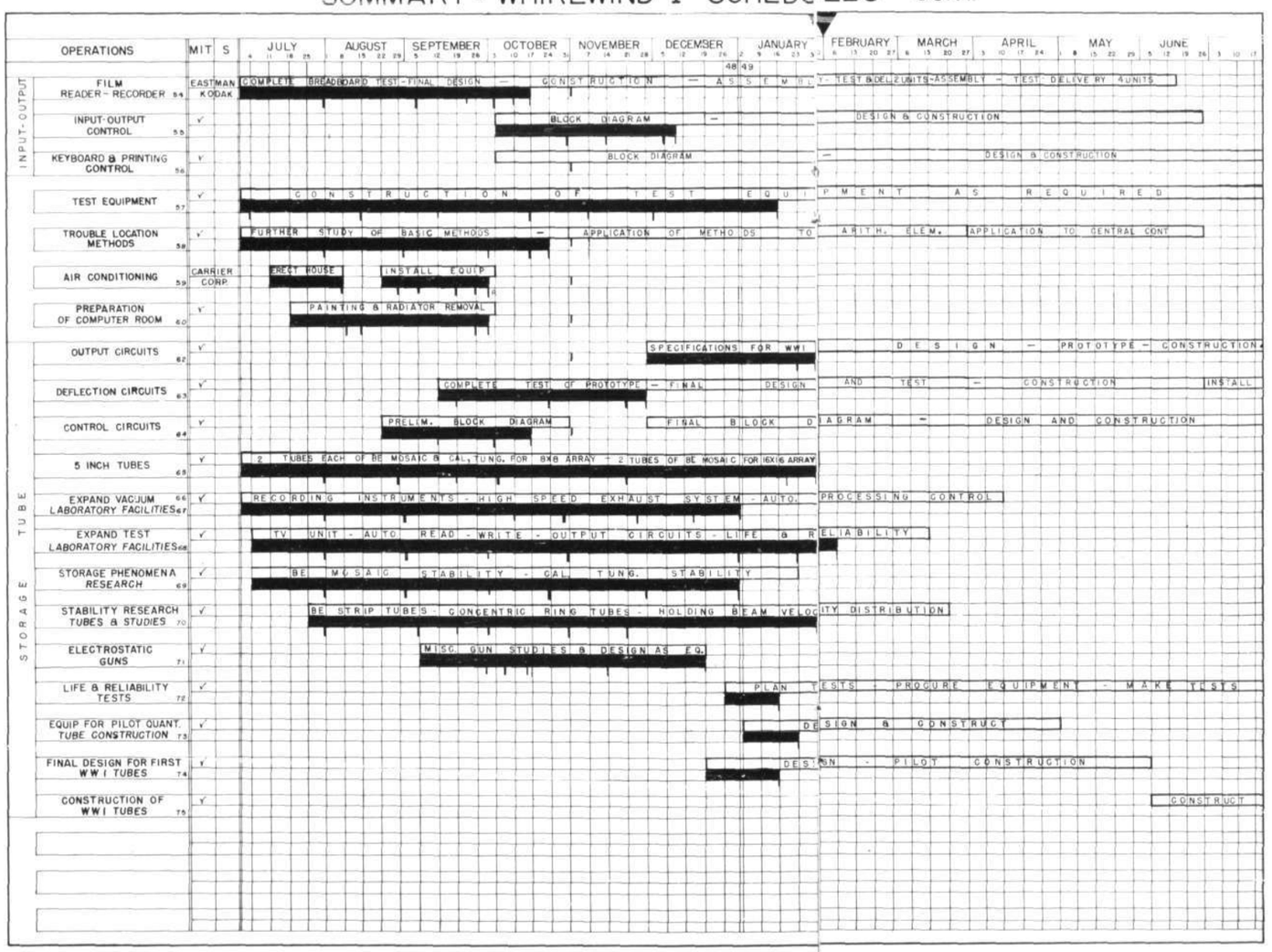
SUMMARY - WHIRLWIND I SCHEDULES -CONT.



LEGEND

JULY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and estimated time allotted for its completion. Estimates made in July 1948.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of latest posting.

Summary line. Shows overall status of the project.

MIT	S
	✓

Column showing whether M.I.T. or Sylvania will do major portion of the job.

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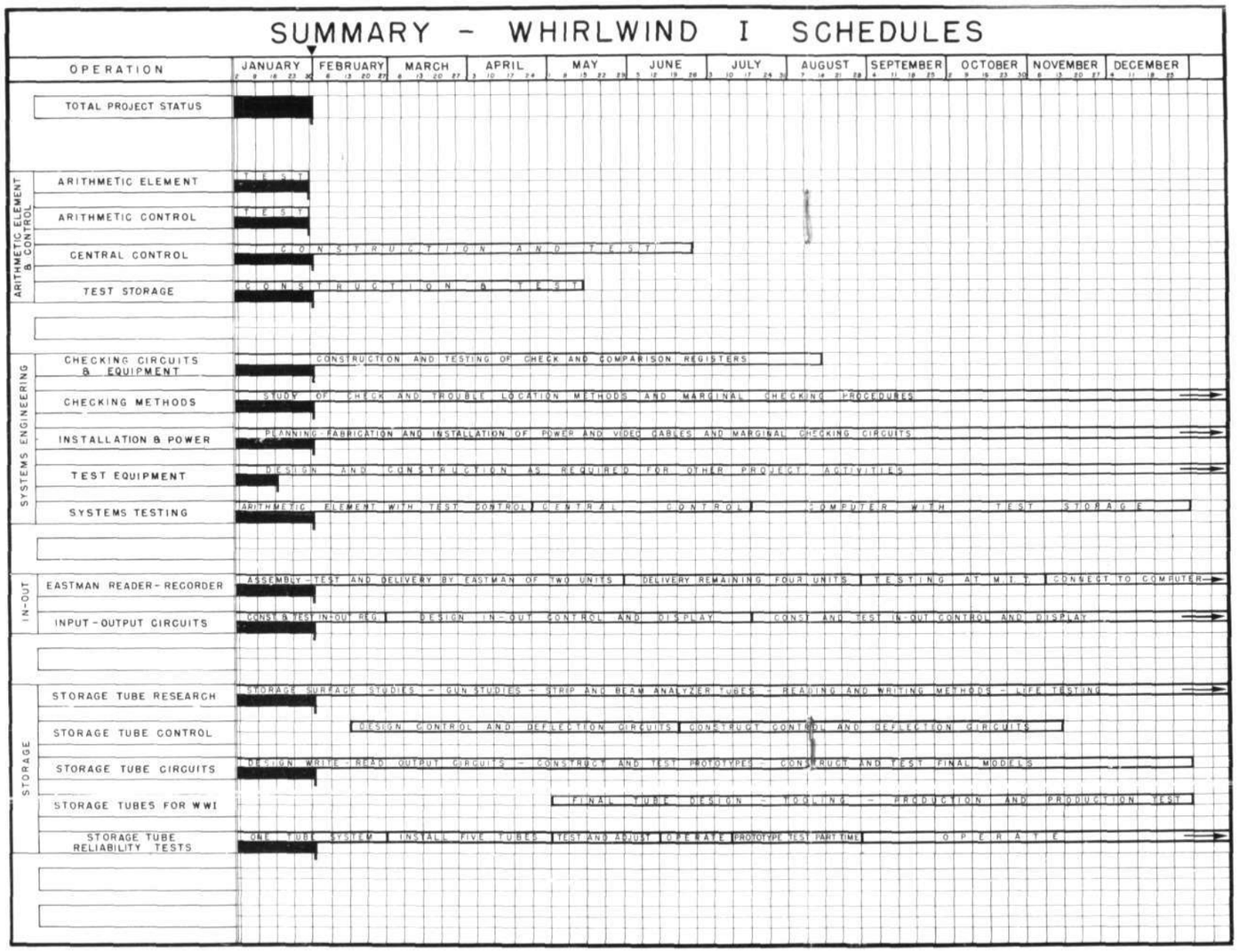
SUMMARY - WHIRLWIND I SCHEDULES



JANUARY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and the estimated time allotted for its completion. Estimates made in January 1949.

Indicates extension of the work into next year.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

▼

Date of the latest posting.

Summary line. Shows the overall status of the project.

For a long-range plan from 1944 to 1952 showing the relation of this detailed schedule to past and future work, see *Summary Report No. 11, August 1948.*

was performed successfully within one day after merger of these two programs by installation of interconnecting cables.

When integration of the arithmetic element with test control has been completed in all respects, and qualitatively correct performance of all basic arithmetic operations has been achieved, all important information on pulse amplitudes and timing will be recorded for future reference. Some preliminary quantitative measurements of this type have already been made (see Summary Report 15, December). These data will be of great value as a basis for trouble location. Additional knowledge to aid trouble-location and reliability studies on the actual WWI equipment will become available after the installation of marginal checking equipment within the next few months.

At the end of January the following WWI equipment was installed and operating:

1. All 16 A-register panels
2. All 16 B-register panels
3. All 16 accumulator panels
4. All 16 arithmetic-element bus-driver panels
5. All 7 arithmetic-element register-driver panels
6. All 7 arithmetic-control panels
7. All test equipment required for the test control system (See Summary Report 13)

In addition, all 16 program-register panels were installed but not yet in use.

As they are completed, units of WWI central control now in the construction stage will be installed to replace portions of the test-control system now in use. This activity will continue throughout the summer.

STORAGE TUBE RELIABILITY TESTER

Work was continued during the month of January on the storage-tube reliability tester described briefly in Summary Reports 14 and 15. This installation is to provide facilities for operation of from one to five electrostatic storage tubes under conditions simulating as closely as possible those which will be encountered in a high-speed electronic digital computer such as WWI. The equipment is so designed that when installation is completed, five-digit words may be: (1) stored on any desired position on the storage surfaces of the five tubes by means of a push-button; (2) maintained stored in a static condition under the action of the holding beam alone; (3) read from any desired storage position, displayed, and rewritten in the same position on the storage surface by means of a push-button; (4) read in from teletype equipment and stored on any number of adjacent positions up to the full capacity of the storage tubes used; (5) read out to teletype equipment; (6) read from each storage position in turn, displayed, and rewritten on the position from which they were just read at frequencies up to 40,000 complete operations per second (minor changes will permit operation of these circuits at frequencies up to 150,000 per second); (7) read from each storage position in turn, displayed, stored temporarily in a flip-flop register, and then written on another storage position at comparable frequencies.

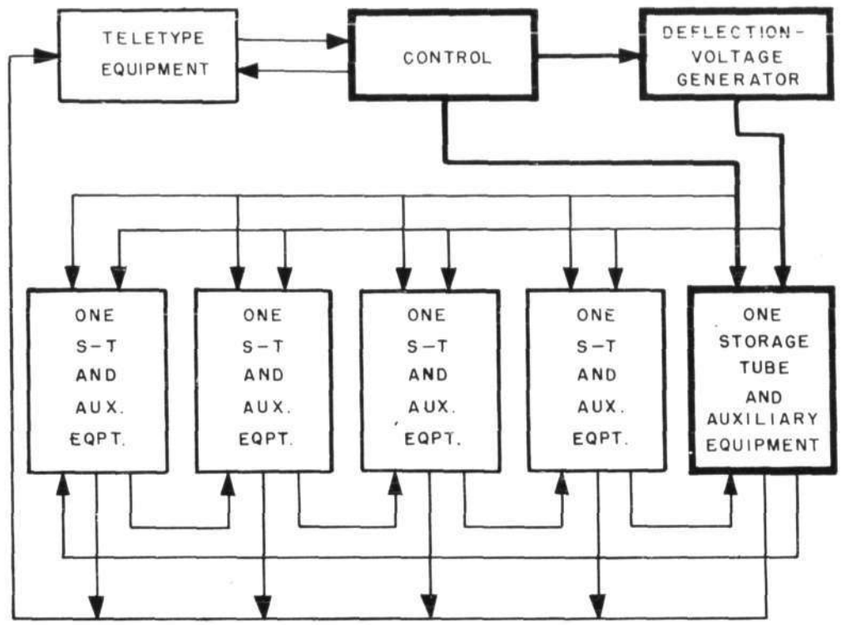
Two methods of error detection will be available. First, if information is stored in such a way that a simple geometric pattern is obtained on the display screens during high-speed cyclic operation, any error will produce a defect in the pattern and will be apparent on visual inspection. Second, if a coherent message is read in from the teletype equipment and then read back out at intervals, any errors will show up in the message read out. It is planned to make extended runs covering periods up to several days in order to determine both the frequency at which errors occur and the manner in which the error-occurrence frequency changes with life.

In the accompanying block diagram the position of the system which has been installed and operated is shown by heavy lines, while the portion yet to be installed is shown by lighter lines.

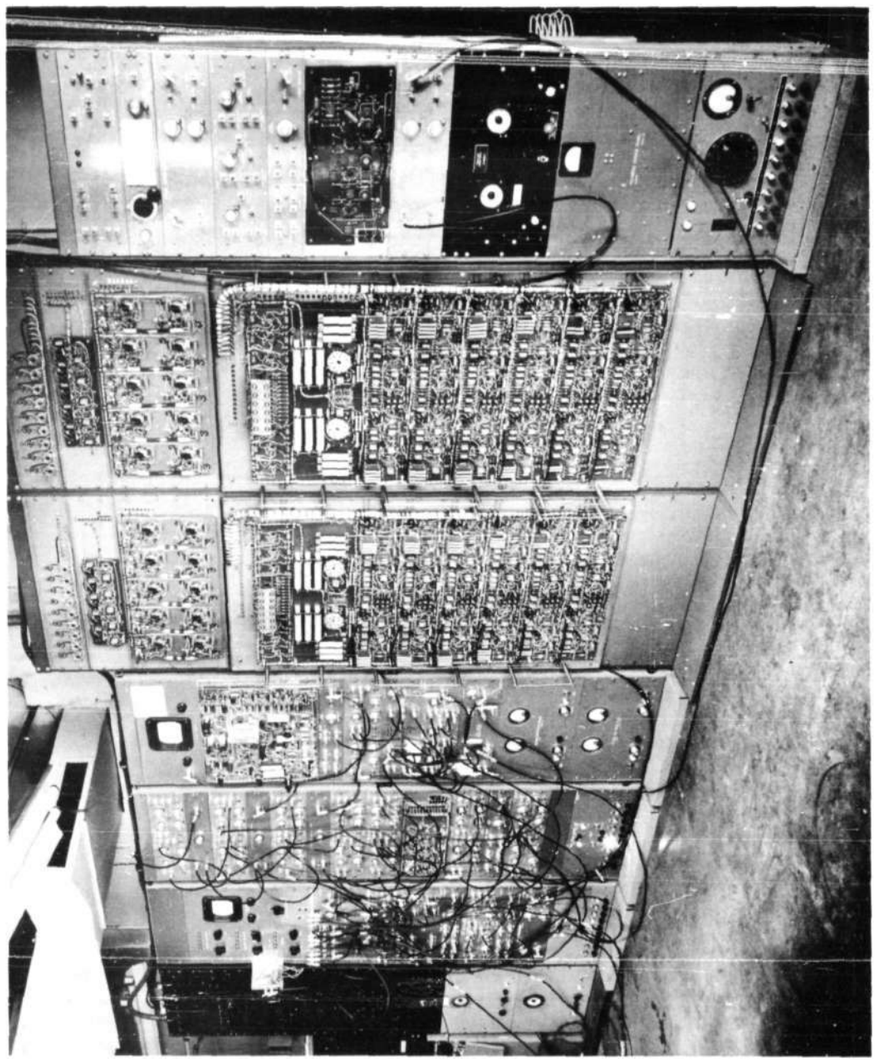
That portion of the system designated as the control consists mainly of standard test equipment plus a main control panel. Test equipment is used to generate all control pulses and gates necessary for the operation of the deflection circuits and the five storage tubes. On the main control panel are located:

1. A 5-inch cathode-ray tube which has its deflection plates connected to the output of the deflection-voltage generator in the same manner as are the deflection plates of the storage tubes. The beam of this tube is intensified whenever the high-velocity beams of the storage tubes are turned on, thus showing the place on the storage surfaces at which any storage operation is performed.
2. A five-position rotary switch which controls the inter-connections of equipment in the system in such a way that five different general modes of operation are immediately available.
3. Push-button switches for starting and stopping high-speed cyclic operation and for performing single-cycle operations.
4. Three rotary-switch decimal-to-binary converters which allow push-button insertion of numbers into the deflection-voltage generator for both deflection coordinates and into the auxiliary storage register associated with the storage tubes.
5. Remote indicator lights which display, under static operating conditions, the settings of the two deflection coordinates and of the auxiliary storage register.

As pointed out in Summary Report 14, the deflection-voltage generator used is the one constructed early in 1948. It is a high-speed 1024-



STORAGE TUBE RELIABILITY TESTER



SETUP FOR STORAGE TURE RELIABILITY TESTER

position unit designed to control deflection of eight storage tubes. In the present system this generator will be required to drive five storage tubes plus six 5-inch cathode-ray tubes; tests have indicated that under such load conditions deflection voltages may be set up in about three microseconds.

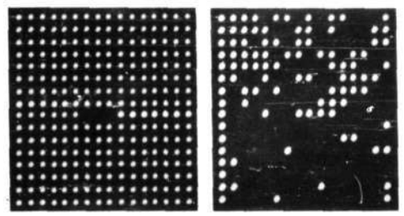
Teletype equipment used will consist of a standard Model 19 page printer set. The transmitter distributer unit will be modified slightly to supply control signals for synchronization of the rest of the system and to transmit information on parallel lines rather than serially when reading into storage.

As shown in the block diagram, the completed reliability-tester system will include five storage-tube positions, each of which will consist of:

1. A storage tube mount which will provide, in addition to mechanical support for a storage tube, all necessary polarizing potentials, bias and focus controls, and metering facilities for the two electron guns.
2. Signal-plate switching and signal output circuits.
3. Auxiliary flip-flop storage registers (standard test equipment) required for read-in and read-out operations.
4. A 5-inch cathode-ray tube on which the signals read from the storage tube will be displayed.

A photograph of the equipment so far assembled appears herewith. On the far left, including the first relay rack visible, are power supplies and distribution panels. At the top of the second rack from the left is the main control panel. The remainder of this rack and all of the third rack is occupied by the test equipment comprising the control. In the fourth rack is mounted one storage tube together with its auxiliary equipment. The bottom third of this rack is occupied by two power supplies which furnish high voltages and bias voltages for the storage tube and display tube. (These supplies also will be adequate to care for most of the additional current required by the other four storage tubes and display tubes when they are installed.) Fifth and sixth in line are two large racks containing the deflection-voltage generator. On the extreme right, the seventh rack contains power control equipment and one special power supply for the deflection-voltage generator; it also mounts test equipment used to supply additional control functions for special tests on the system and on individual blocks of the system.

Temporary video read-out circuits were used during the entire month, since components for r-f read-out were not yet available. Although completely satisfactory results were not obtained because of difficulties with the read-out circuits, patterns containing 256 stored elements (16 x 16 array) were maintained without error under cyclic high-speed operating conditions for periods of more than one hour. Accompanying photographs show the appearance of the display during a type of cyclic high-speed operation in which each stored point is examined in turn, the result displayed, and then re-written on the same point. In these pictures a



STORAGE DISPLAYS

bright spot indicates that the corresponding point on the storage surface is at holding-gun cathode potential, while the absence of a spot indicates that the corresponding point on the storage surface is at collector potential. In the first photograph all spots are negative with the exception of numbers 118, 119, and 120, which have been written positive. The second photograph shows storage of an almost-random pattern in which the larger portion of the stored spots are positive (the entire left-hand vertical column and the two right-hand corners were written negative to show the extent of the array).

During the first part of February r-f read-out circuits will be installed and tested on the single-storage-tube system now in existence. When

sufficient information has been obtained to allow evaluation of the r-f read-out circuits, testing will be suspended and installation of the remaining four storage-tube positions and the teletype equipment will be undertaken.

FLIP-FLOP DEVELOPMENT

The WWI flip-flop uses direct coupling between its two vacuum tubes, but the circuit as a whole is connected to its load (usually a gate tube) through a condenser. The WWI arrangement, arbitrarily defined as an a-c-coupled d-c flip-flop, is discussed at length in Summary Report 3. Although the present design has proved satisfactory for most WWI applications and will be used unchanged throughout WWI, additional work on the flip-flop as a fundamental computing element is progressing along several lines in an attempt to make basic improvements. The continuing research program includes:

1. Detailed study of a low-speed analogue of the present flip-flop to increase the knowledge of its performance characteristics.
2. Design of a d-c flip-flop which can be direct-coupled to a load without imposing the usual disadvantages encountered in the direct coupling of vacuum-tube stages. No restorer pulses (see Summary Report 3) are necessary when d-c coupling is used throughout the signal channels carrying flip-flop waveforms. Several promising designs are being studied, including one described below which results in very short switching times.
3. Design of an a-c flip-flop, i.e., a flip-flop with capacitive coupling between its two vacuum tubes, or in other words, a multivibrator adapted as a binary storage element. This approach is based on the reasoning that since restorer pulses must be made available if the advantages of a-c load coupling are to be obtained, one may as well introduce capacitive cross-coupling between the two tubes of the flip-flop itself and depend upon restorer-pulse action to maintain the resulting multivibrator circuit in one of its two quasi-stable states.

These investigations include studies of ways in which switching times may be reduced by the incorporation of cathode followers as integral parts of flip-flop circuits. The individual projects are treated in more detail below.

Low-Speed Analogue of Flip-Flop

The basic flip-flop of Whirlwind I has been designed for extremely high-speed switching to minimize waste of time during computational procedures, the standard flip-flop circuit having a switching time of the order of 0.2 microsecond. The techniques employed in the design and testing of a high-speed flip-flop are necessarily closely related to the techniques applied to high-frequency circuits; emphasis must be placed upon the minimization of stray capacitances, lead inductances, and unwanted intercircuit coupling. Inherent limitations on the accuracy of high-frequency measuring instruments impose serious restrictions on the accuracy and utility of experimentally derived data. For example, observation of flip-flop voltage waveforms requires the connection of a cathode-ray oscilloscope to the flip-flop, a procedure which appreciably distorts the existing waveforms.

One way to avoid this problem has been found in the construction of a low-speed analogue of the circuit. A low-speed analogue is a circuit in which all resistances, voltages, and currents of the original have been duplicated, but the inductance and capacitance values have been increased by a large factor to produce a corresponding reduction in the response speed of the circuit. An analogue of the basic flip-flop has been tested extensively; the inductances and capacitances of this model have been increased by a factor of 10^6 to cause the switching time of the analogue to be approximately 0.2 second, one second of analogue time corresponding to one microsecond of real time. Voltage and current waveforms during the switching cycle are recorded on chart tape by the use of a direct-inking oscillograph.

The recorded waveforms of the analogue closely duplicate all the corresponding waveforms of the high-speed flip-flop that are known accurately. Various currents and voltages which cannot be measured directly on the high-speed circuit with existing test equipment can be recorded on the analogue; this information is of value in the design of improved flip-flops and in the evaluation of the present basic flip-flop. In addition, various circuit capacitances can be varied on the analogue to observe the effect of these capacitances on circuit performance. Such variation of capacitances on the high-speed circuit can be achieved only over a very limited range of capacitance values because of unavoidable minimum circuit capacitances.

The trigger pulse height, shape, and repetition rate can be varied on the analogue to study their effect on flip-flop operation. By extension of the method now employed to utilize multi-channel recording, all significant voltages and currents of both flip-flop tubes can be recorded simultaneously. Such multi-channel simultaneous recording would permit study of erratic flip-flop action and analysis of marginal checking methods for flip-flop circuits.

D-C Flip-Flop for D-C Load Coupling

The d-c flip-flop used in Whirlwind I is connected to its associated gate tubes through coupling condensers on which the charge must be maintained by the use of restorer pulses. However, in certain circuit applications these restorer pulses are especially inconvenient, and an arrangement in which the gate tubes are connected directly would have the advantage of permitting operation without the use of restorer pulses.

Connecting the plate circuits to ground and using a negative voltage source at the cathode of the conventional flip-flop would provide a circuit with a usable gate voltage at the plate of either tube if it were not for the current which flows through the plate-grid voltage-dividing network even though one tube may be completely cut off. This results in some current through the plate load resistor of the non-conducting tube, with a consequent objectionable negative voltage on the plate during the interval when pulses are to be passed by the gate tube. Although commonly used, this arrangement (see Figure 1, Summary Report 3) is considered undesirable because changes in tube, circuit parameters, and power-supply voltages affect performance appreciably.

In a circuit (Figure 1) with the plate-to-grid voltage-dividing network isolated by a cathode follower, no current flows through the plate load resistor of the "off" tube. This plate will go to ground potential, which is not subject to drift, and an absolutely stable gate voltage is available. When the tube conducts, the plate will become negative, and although this negative voltage may drift somewhat, its variations are unimportant since it is always below the cutoff level of the gate tubes being driven.

An additional advantage of such coupling lies in the reduction of the shunt capacitance affecting the plate circuit. This, along with the high-current tube used, results in excellent rise time of the plate waveform and permits heavy loading of one or both sides of the flip-flop without increasing the rise time beyond usable limits. In one circuit using wire-wound resistors as plate loads, the plate waveform of this type flip-flop had a rise time of the order of 0.06 microsecond, and with one side driving 100 micromicrofarads of shunt capacitance, a rise time of the order of 0.1 microsecond was observed. The circuit is therefore especially suitable for use in matrix switches, where short rise times are desirable and where the shunt capacitances are relatively large.

This d-c-coupled d-c flip-flop is being studied with a view to improving it so that it may be applied in the greatest variety of cases. Problems such as unbalance between tubes, resolution time, and triggering circuits are receiving attention.

To simulate the effect of unbalanced tubes, which were not available in sufficient quantity to make their use practical, resistors were inserted in the plate of one tube, the value of the resistors being increased until unstable operation of the flip-flop was observed. While the immediate effect of unbalance was to increase the trigger voltage required, an unbalance as great as 20 milliamperes

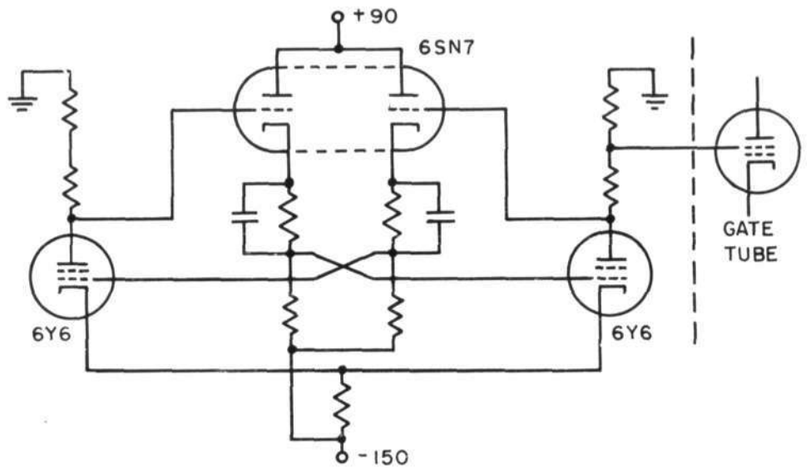


FIG. 1. FLIP-FLOP SUITABLE FOR D-C LOAD COUPLING
(WITH D-C INTERNAL COUPLING)

in the flip-flop tubes still permitted satisfactory operation with trigger pulses of standard 18-volt amplitude.

An attempt is being made to improve the resolution time, which now has a maximum top steady-state switching frequency of about 3 mc. The time constants in the cathode-follower circuit and in the triggering circuit seem to provide the limiting effect. Experiments are being made with different parameters to reduce this limitation, so that the eventual resolution time should approach more closely the very short rise time on the plate waveform.

A-C Flip-Flop

In the multivibrator-type binary storage element known as an a-c flip-flop (see page 5, Summary Report 3, for elementary discussion), one important problem not at first apparent is that of providing a means for complementing. In the WWI-type flip-flop, the parallel R-C cross-feed networks serve as a memory device which effectively remembers the state of the flip-flop before triggering, so that after application of a trigger pulse the flip-flop resides in the opposite state. However, when only capacitors are used for cross-feeding signals from the plate of one tube to the

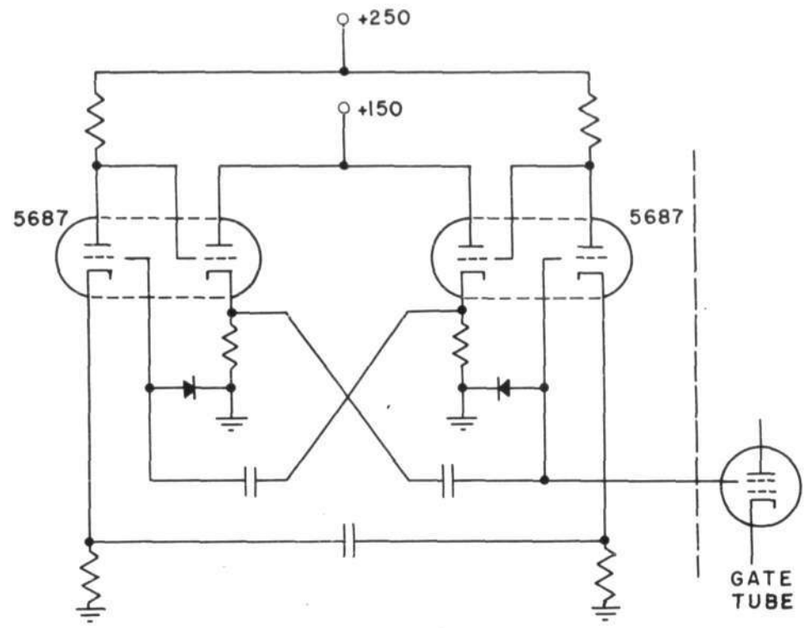


FIG. 2. FLIP-FLOP WITH A-C INTERNAL COUPLING
(AND WWI-TYPE A-C LOAD COUPLING)

grid of the other, this memory function is no longer available as a characteristic of the cross-feed network and must therefore be introduced elsewhere in the circuit. One solution to this difficulty is obtained if small resistors are inserted in series with the cathodes of each of the flip-flop tubes, and the cathodes are coupled together through a capacitor. This arrangement, indicated in Figure 2, has been found to perform satisfactorily and to ensure correct complementing of the a-c flip-flop circuit shown. Trigger pulses for complementing are applied simultaneously at both flip-flop plates; cathode triggering, as employed in the WWI flip-flop, is not used here because it produces pips on the plate waveform which adversely affect the level of the output gate due to the clamping action of the crystal rectifiers.

The work on the a-c flip-flop has demonstrated that pentode and beam-power tubes are not essential to high-speed switching circuits, and that ordinary triodes can be used effectively. To reduce the effect of the high input capacitance of an ordinary triode circuit, triode cathode followers were introduced in accordance with the same reasoning which led to their application in the d-c flip-flop discussed above.

Two dual triodes were utilized as shown in Figure 2. Here each envelope provided one flip-flop tube and its associated catnode follower. The d-c coupling employed between these two units results in none of the usual undesired effects of d-c coupling, and should be thought of here merely as providing a low-impedance voltage source which is to be capacitively coupled to the opposite section of the flip-flop.

The scheme used is convenient in that additional capacitors and crystal rectifiers are not necessary for coupling the flip-flop to its gate-tube load. The usual WWI type of coupling network is already available within the flip-flop itself in the form of the cross-coupling capacitors and clamping crystal rectifiers. Gate-tubes are connected as shown in the circuit diagram.

The flip-flop designed (as a master's thesis project) according to these ideas operated very well. Rise and fall times of 0.05 microsecond were obtained for an output signal of 26 volts, so that the circuit would operate at switching speeds up to 10 megacycles. The circuit also operated perfectly well with intervals as long as 200 microseconds between restorer-pulse pairs. (In WWI the maximum interval is about 50 microseconds.)

MATHEMATICS: CODING OF PROBLEMS

In recent weeks the Mathematics Section has coded several different problems for future use in WWI. Most of these are intended as subprograms, or simply as parts of some complete program. For example, a short code has been written by which the computer can be made to evaluate e^{-x}. The intent, of course, is not to assign the computer simply to the task of evaluating this well-known function, but rather to enable it to evaluate e^{-x} whenever this is necessary as one step in some more complicated problem. Similar subprograms have been written for evaluating log x, for picking the maximum out of a random set of numbers, for arranging a random set of numbers into numerical order, and for selecting a desired value from a table of values.

A program is being coded by which the computer can be used in conjunction with transponder radio direction finders to automatically control ship traffic along a river, channel, or sea lane. This problem was undertaken largely as a realistic example to investigate control techniques, but the solution may be of practical value.

In an S.M. thesis submitted to MIT under the title "Intact Stability Study Programmed for a Digital Computer," a single practical problem - the calculation, from design data, of the stability of a ship at various angles of heel - is reduced to a strictly numerical procedure and is programmed in detail for the Whirlwind computer. This study was based on information supplied by the Bureau of Ships. Even with the limited memory capacity of WWI, problems of the magnitude of intact stability studies, which require twenty to thirty man-days of machine-assisted hand computation, can be reduced to a very few man-hours of data preparation plus a few seconds of computation on the Whirlwind machine.

The entire program requires the storage of 768 control orders in the computer memory. In the course of the computation the computer cycles repeatedly through groups of these orders and actually performs about 1,500,000 operations, requiring about 30 seconds. Only 10,000 operations (about 0.2 second) are necessary for integration over the ship in upright position. Finding cross curves of stability involves integration of the area and moment of the ship at each station up to a rotated waterline. This can be done quite simply (but slowly) with an area-and-moment integraph, but is rather complicated to do numerically. In fact, determination of the cross curves is less than half the job in the hand computation, but in the computer it uses about 99.3% of the computation time. In its present form the program can be used in connection with any ship. Most of the necessary data consists of half-breadths taken at 21 stations and at heights chosen more or less at will.

This program can be put to specific use in intact stability studies. In addition, the work demonstrates that a high-speed digital computer is capable of solving not only inherently numerical problems (such as the part of an intact stability study that yields curves of form in upright position) but also inherently graphical (analogue) problems (such as the part that yields cross curves of stability) not ordinarily thought of as well suited for digital procedures.

VISITORS

During January the Laboratory had among its visitors interested in digital computer applications and progress the following:

Mr. A. Wertheimer, of the Bureau of Ordnance (U. S. Navy), and Mr. S. Feltman of the Ordnance Department (U. S. Army).

Dr. Emanuel Piore of the Physical Sciences Division, Office of Naval Research.

Mr. J. H. Halgren of RCA, to discuss the interface problem in vacuum tubes.

Captain E. K. Walker and Dr. R. C. H. Wheeler of the U. S. Naval Academy, to discuss the use of digital computers in naval ordnance.

Mr. E. G. Cullwick and Mr. Cyril Turner of the Canadian Defense Research Board.

Dr. R. F. Clippinger of the Ballistics Research Laboratory, Aberdeen Proving Ground.

Lt. Commander B. E. Miles and Lt. J. L. Belyea of the Naval Service Headquarters, Royal Canadian Navy.

Mr. R. W. Slinkman of Sylvania and Mr. N. Rochester of International Business Machines Corporation, to discuss tube deterioration.

Among visitors especially interested in storage tubes were the following:

Mr. J. H. Muncy of the Naval Research Laboratory Field Station, concerned with applications of storage tubes to radar.

Dr. A. V. Haeff of the Naval Research Laboratory.

Dr. H. E. Mendenhall and Dr. B. McMillan of Bell Telephone Laboratories, with Professor Wayne Nottingham of MIT.

Mr. J. N. Davis, Dr. H. Jacobs, Mr. L. H. McKee, and Dr. S. T. Martin of Sylvania.

Mr. T. F. Rogers and Mr. J. V. Harrington of the Electronics Research Laboratory (formerly Cambridge Field Station).

APPENDIX

REPORTS AND PUBLICATIONS

The following reports and memorandums on Project Whirlwind work were among those issued during January:

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
SR-14	Summary Report No. 14	17	-	11-48	
E-154-1	Further Development of Beryllium Evaporation Tubes	4	2	1-26-49	H. Klemperer M. Florencourt
E-166	Simulation of Empirical Functions (in Particular, of Aerodynamic Coefficients) by Polynomials	27	-	12-3-48	M. Daniloff
E-170	Codes for the Evaluation of e^{-x} and ln x	9	-	1-18-49	T. W. Hildebrandt
E-171	Summary of Report R-134, The Five-Digit Multiplier	2	-	1- 4-49	R. R. Rathbone
E-173	Storage Tube 56: Construction and Processing	2	-	12-21-48	M. Florencourt
E-174	Storage Tube 57: Construction and Processing	2	-	12-28-48	M. Florencourt
E-175	Storage Tube 60: Construction and Processing	2	-	12-28-48	M. Florencourt
E-176	Changes Required for Clearing Carries on Divide	1	-	1 -18-49	J. M. Salzer R. P. Mayer
E-177	Change Required to Shift Zeros into BR15	2	-	1 -18-49	J. M. Salzer R. P. Mayer
E-178	Standard Tests for Reference in Storage Tube Evaluation	3	-	1 -18-49	S. H. Dodd C. L. Corderman
E-179	Quality Study of WWI Electron Tubes	2	2	1 -18-49	R. L. Ellis
E-180	Storage Tube 62: Construction and Processing	2	-	1 -20-49	M. Florencourt
E-181	Research Tube 47 - Construction and Processing	2	-	1 -21-49	M. Florencourt
E-182	Storage Tube 61: Construction and Processing	2	-	1 -21-49	M. Florencourt
E-183	Storage Tube 69: Construction and Processing	2	-	1 -19-49	M. Florencourt
E-184	Storage Tube 63: Construction and Processing	3	-	1 -25-49	M. Florencourt
E-186	Storage Tube 68: Construction and Processing	3	-	1 -27-49	M. Florencourt
E-188	Tube Characteristic Drawings	5	-	2 - 1-49	A. M. Falcione
M-611-1	The Dispersion of the Holding Gun Beam Within the Collector to Target Surface Field	3	3	12-30-48	J. S. Rochefort
M-673	Tests on Storage Tube 37	3	8	11- 2-48	R. L. Sisson
M-676	Model I Storage Tube	16	32	11- 3-48	S. H. Dodd W. J. Nolan
M-729	Initial Testing of Storage Tube 29	7	5	12- 9-48	C. L. Corderman
M-737	Changes in Test Storage Switch	2	1	12-17-48	J. M. Salzer R. P. Mayer
M-738	Alteration of Clock Pulse Control	2	1	12-17-48	R. P. Mayer
M-739	Storage Tube 54: Construction, Processing, and Testing	2	-	12-14-48	M. Florencourt

No.	Title	No. of Pages	No. of Drwgs.	Date	Author
M-740	Potential Fields and Electron Trajectories in the Holding Gun	6	6	12-20-48	H. E. Rowe
M-741	Special Display	3	1	12-21-48	J. M. Salzer R. P. Mayer
M-742	Storage Tube 41 Tests	4	2	12-22-48	H. Rowe
M-747	High Repetition Rate Write-Read Unit (Preliminary Report)	2	4	12-30-48	N. S. Zimbel
M-750	Representation of Delays in Block Diagrams	1	-	1 - 4-49	J. M. Salzer
M-752	Bi-Weekly Report, Part I, 1-7-49	12	-	1 - 7-49	
M-753	Bi-Weekly Report, Part II, 1-7-49	14	-	1 - 7-49	
M-754	Holding Beam Trajectories and Potential Fields in the Storage Tube	3	4	1 - 7-49	H. Rowe
M-755	Progress Report: A Dual-Triode Capacitively-Coupled Flip-Flop	2	2	12-31-48	M. H. Hayes
M-756	Progress Report: Development of a Low-Speed Analogue for Flip-Flop Analysis	2	-	12-31-48	J. M. Hunt
M-760	Testing of Storage Tube 45	7	11	1 -18-49	A. H. Ballard
M-761	Progress Report: Development of a Low-Speed Analogue for Flip-Flop Analysis	2	-	1 -15-49	J. M. Hunt
M-763	Bi-Weekly Report, Part I, 1-21-49	18	-	1 -21-49	
M-764	Bi-Weekly Report, Part II, 1-21-49	17	-	1 -21-49	
M-765	Eastman Conference - January 25, 1949	3	-	1 -26-49	H. R. Boyd
M-767	Progress Report: Development of a Low-Speed Analogue for Flip-Flop Analysis	2	-	1 -31-49	J. M. Hunt
M-768	Navy Logistics: - Note for Members of the ONR Committee Studying the Application of Computers	7	-	1 -28-49	W. Welchman
C-83	The Process of Turning a Ship	16	2	12-22-48	M. Daniloff
C-84	Applications Group Working Notes, December 21 to 28	3	-	12-23-48	W. G. Welchman
C-85	Applications Study Group Working Notes, December 28 to January 4	2	-	12-29-48	W. G. Welchman
C-86-1	Applications Study Group Working Notes, January 4 to January 11	4	-	1 - 6-49	W. G. Welchman
C-87	Working Notes January 11-18	2	-	1 -12-49	W. G. Welchman
C-88	Flow Diagram II, for Ship Control Problem	5	-	1 -19-49	R. P. Mayer
C-89	Applications Study Group Working Notes, January 20 to 27	2	-	1 -21-49	W. G. Welchman
C-90	Applications Study Group Working Notes, January 27 to February 1	4	-	1 -28-49	W. G. Welchman
C-91	A Ballistic Problem	2	-	1 -31-49	P. Franklin
C-92	Applications Study Group Working Notes, February 1 to 8	2	-	2 - 2-49	W. G. Welchman