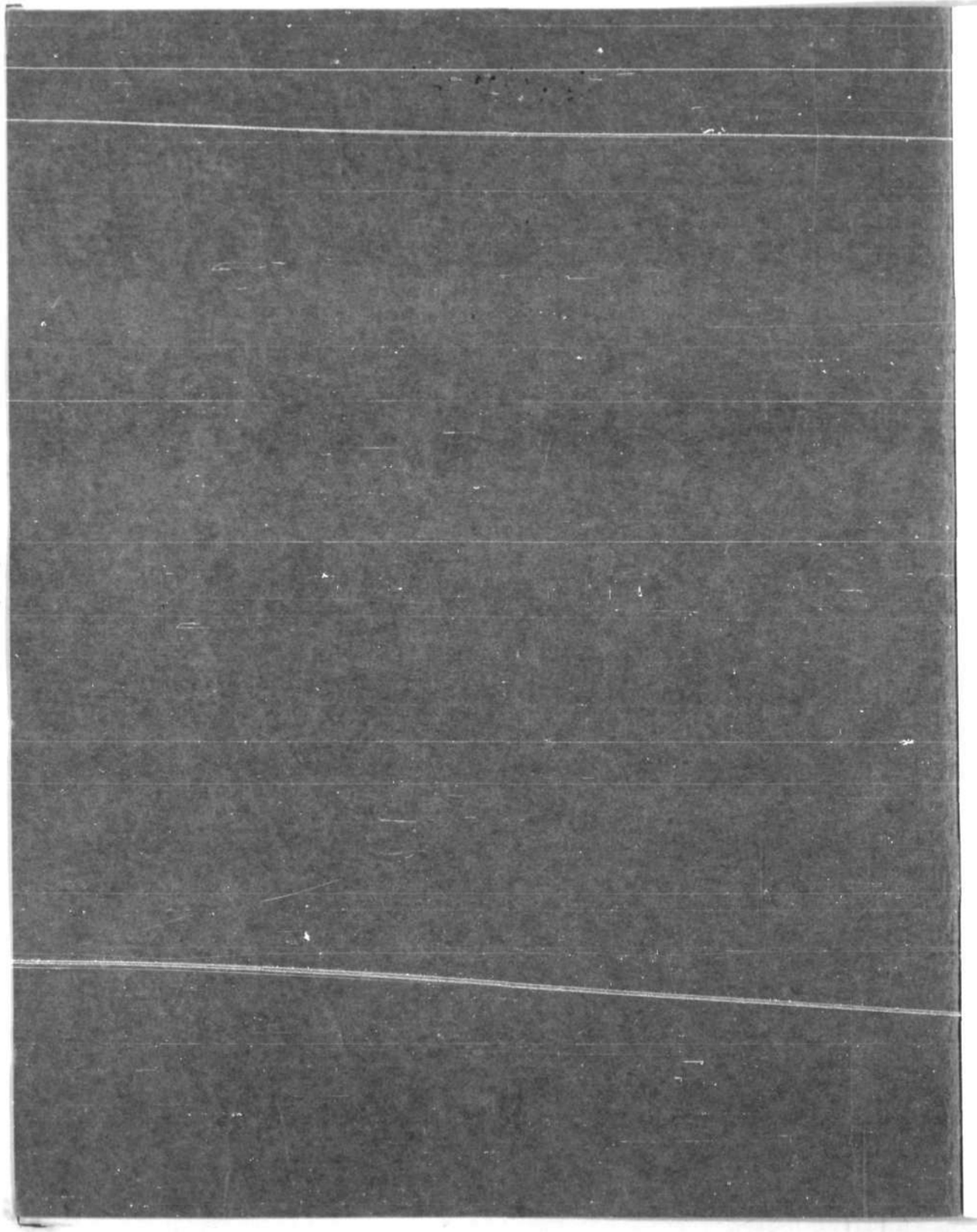

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PROJECT WHIRLWIND
(Device 24-x-3)

SUMMARY REPORT NO. 19
SECOND QUARTER, 1949

Submitted to the

OFFICE OF NAVAL RESEARCH
Under Contract N5ori60
Project NR-048-097

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Cambridge 39, Massachusetts
Project DIC 6345

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FOREWORD

Project Whirlwind

Project Whirlwind at the Massachusetts Institute of Technology Servomechanisms Laboratory is sponsored by the Office of Naval Research under contract N5ori60. The original objective of the Project was the development of a device that would simulate airplanes in flight. An integral part of such a simulator is a digital computer of large storage capacity and very high speed, to provide continuous solutions to the equations of motion of an airplane.

As Project Whirlwind has evolved, applications to other types of simulation and to control have become important. Because the digital computer is basic to all these as well as to important applications in mathematics, science, engineering, and military problems including logistics and guided missiles, nearly all project resources are at present devoted to the design and construction of a suitable computer.

The Whirlwind Computers

The Whirlwind computers will be of the high-speed electronic digital type, in which quantities are represented as discrete numbers, and complex problems are solved by the repeated use of fundamental arithmetic and logical (i.e., control or selection) operations. Computations are executed by fractional-microsecond pulses in electronic circuits, of which the principal ones are (1) the flip-flop, a circuit containing two vacuum tubes so connected that one tube or the other is conducting, but not both; (2) the gate or coincidence circuit; (3) the electrostatic storage tube, which uses an electron beam for storing digits as positive or negative charges on a storage surface.

Whirlwind I (WWI), now being built, may be regarded as a prototype from which other computers will be evolved. It will be useful both for a study of circuit techniques and for the study of digital computer applications and problems.

Whirlwind I uses numbers of 16 binary digits (equivalent to about 5 decimal digits). This length was selected to limit the machine to a practical size, but it will permit the computation of many simulation problems. Calculations requiring greater number length will be handled by the use of multiple-length numbers. Rapid-access electrostatic storage will have a capacity of 32,000 binary digits, sufficient for large classes of actual problems and for preliminary investigations in most fields of interest. The goal of 20,000 multiplications per second is higher than general scientific computation demands at the present state of the art, but is needed for control and simulation studies.

Reports

Summary Report No. 2, issued in November, 1947, was a collection of all information on the Whirlwind program up to that time. The present series of quarterly reports is a continuation of the Summary Report series, designed to maintain a supply of up-to-date information on the status of the Project.

Detailed information on technical aspects of the Whirlwind program may be found in the R-, E-, and M-series reports and memorandums that are issued to cover the work as it progresses. Of these, the R-series are the most formal, the M-series the least. A list of the publications issued during the period covered by this Summary, together with instructions for obtaining copies of them, appears at the end as an appendix.

1. QUARTERLY REVIEW

The general progress of the Project during April, May, and June, the period covered by this report, has been about as predicted in the last Quarterly Review, in Summary Report 18. Included herein are two time schedules, one made in January 1949 covering the calender year 1949 and posted to June 30, the other recently made, covering the period July 1949 to June 1950. The current posting of the old schedule shows the majority of the items quite well on schedule, exceptions being delivery of the Eastman film units, certain aspects of storage tube research, and the storage tube reliability tester, all of which are discussed below. We feel that these discrepancies will not have any material effect on the over-all progress for the calender year. The new schedule takes account of the fact that much of the construction and individual testing has been completed, and rearranges the various items to show when we expect to incorporate these sections of the computer into an operating system, and along what lines we expect to direct subsequent efforts.

The major effort of the system group in the past six months has been devoted to extensive tests of the arithmetic element. We believe the successful operation of a computer of the magnitude of WWI is so dependent on such a test program that it deserves the most careful consideration. Accordingly we are describing it in some detail in Section 2.2.

Construction and preliminary testing of central control and test storage has been completed. Parts of central control are already operating in the system, replacing the test equipment which has previously simulated the necessary functions. The remainder of central control and test storage will be gradually incorporated in the system during July and August, as shown on the time schedules originally published in January in Summary Report 16. In the past few months certain rather fundamental design changes have been made in central control. Their evolution is discussed in Section 2.3. Since the operation matrix is about to be connected into the system, it has become necessary to freeze the orders which would first be wired into it. An up-to-date list and a description of these orders is given in Section 2.4.

The relatively small number of tube and component failures in WWI during the past six months has been gratifying. As tabulated in Section 3, after 1000 hours of operation, eight tubes out of 1200 have failed; six other components have been replaced. On the other hand, the reliability of the five-digit multiplier has been less than our hopes and expectations. Random errors have been occuring at the rate of about one every two days. The reliability test is continuing and we hope to be able to track down the source of these errors. Since the construction of the five-digit multiplier nearly two years ago as a prototype for the WWI arithmetic element, we have improved our circuits, component inspection, and construction methods. We hope, when reliability runs begin on WWI, that this experience will result in more satisfactory operation.

The storage tube group is now engaged in making a pre-production run of tubes to a design which, in the past two months, has proved satisfactory for initial WWI operation. Although the percentage of satisfactory tubes is still low, we feel that standardization of procedures and training of personnel should result in the ability to start production of tubes for WWI in October.

Storage tube research is shown on the summary as behind schedule. This is because certain investigations we planned at the beginning of the year have had to be deferred in favor of the solution of unforeseen problems in producing tubes satisfactory for initial operation.

Life tests are encouraging. In a group of eight tubes on test, there have been no failures. One tube has run 3300 hours, three others more than 1800 hours. The reliability tester, which permits simulated computer operation by cycling a stored pattern through one or more tubes, has not yet been extended to five tubes, but should be completed in July. Delays were caused mainly by troubles in the test equipment associated with the single-tube setup, and shortage of manpower available for this particular project. A more detailed

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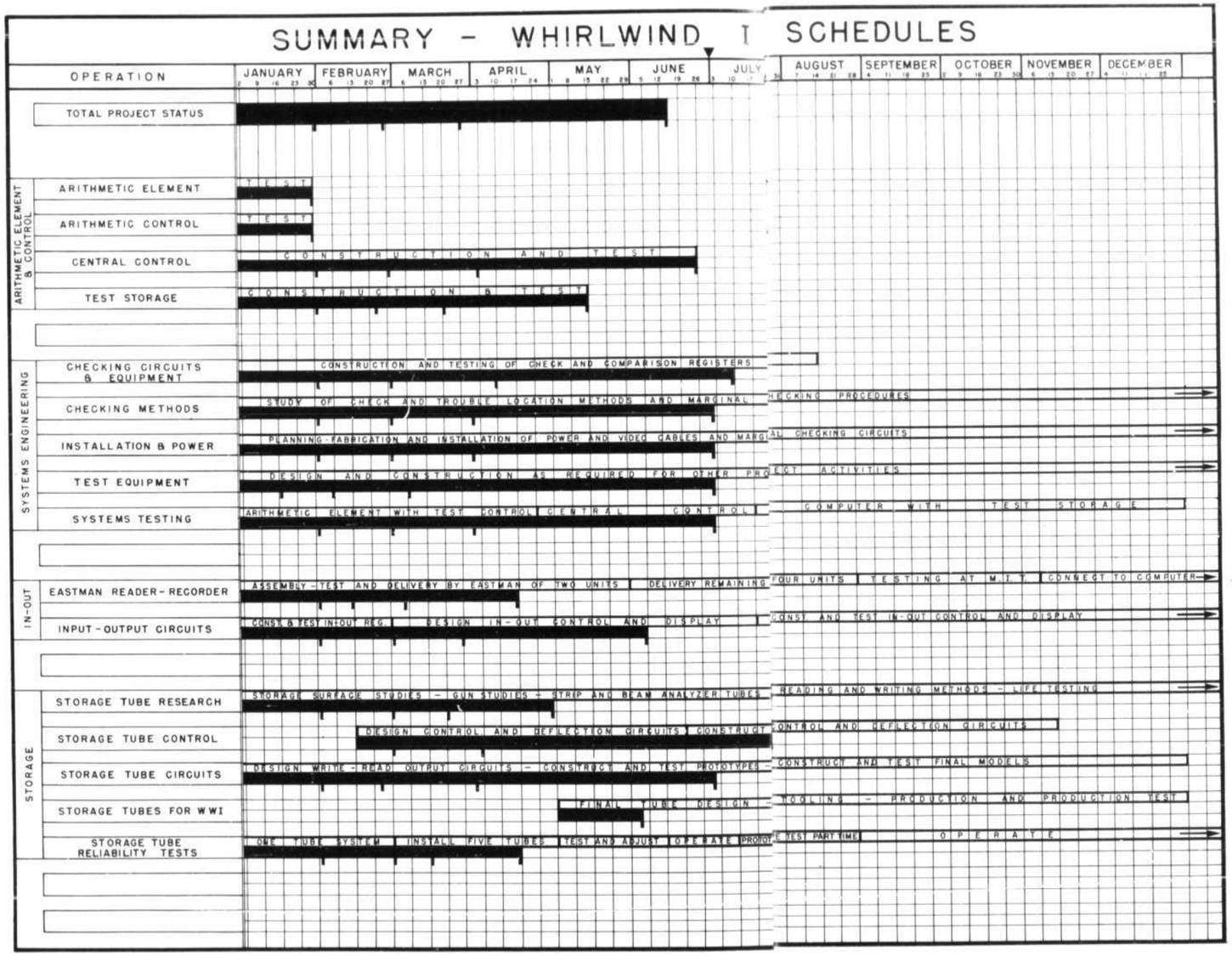
SUMMARY - WHIRLWIND I SCHEDULES



LEGEND

JANUARY

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and the estimated time allotted for its completion. Estimates made in January 1949.

Indicates extension of the work into next period.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

Date of the latest posting.

Summary line. Shows the overall status of the project.

SUMMARY - WHIRLWIND I SCHEDULES

	OPERATION	JULY 4 11 18 25	AUGUST 1 8 15 22 29	SEPTEMBER 5 12 19 26	OCTOBER 3 10 17 24 31	NOVEMBER 7 14 21 28	DECEMBER 5 12 19 26	JANUARY 2 9 16 23 30	FEBRUARY 6 13 20 27	MARCH 6 13 20 27	APRIL 3 10 17 24	MAY 1 8 15 22 29	JUNE 5 12 19 26 3 10
	TOTAL PROJECT STATUS							49 50					
SYSTEM TESTING	ARITHMETIC ELEMENT - OPERATION MATRIX - TEST STORAGE	CONTROL & TEST STORAGE TESTS											
SYSTEM TESTING	ARITHMETIC ELEMENT - CENTRAL CONTROL - TEST STORAGE		SOLUTION & DISPLAY OF SHORT PROBLEMS										
SYSTEM TESTING	ARITHMETIC ELEMENT - CENTRAL CONTROL - TEST STORAGE - IN-OUT						COMPUTER WITH TEST STORAGE - IN-OUT CONTROL & FILM UNITS						
SYSTEM TESTING	WHIRLWIND I WITH ELECTROSTATIC STORAGE		ES CONTROL	PRELIMINARY TEST IN STORAGE ROW					COMPLETE WWI SYSTEM TESTING →				
SYSTEM TESTING	CHECKING & TROUBLE LOCATION	MARGINAL CHECKING STUDY & INSTALLATION					CHECKING & TROUBLE LOCATION PROBLEMS →						
SYSTEM TESTING	WHIRLWIND I RELIABILITY STUDIES							WHIRLWIND I RELIABILITY STUDIES →					
IN-OUT	FIRST TWO UNITS OF THE EASTMAN READER - RECORDER	TEST & DELIVERY	TEST WITH COMPUTER IN-OUT CIRCUIT		INTEGRATE WITH COMPUTER								
IN-OUT	REMAINING FOUR UNITS OF EASTMAN READER - RECORDER	ASSEMBLY - TEST & DELIVERY							INTEGRATE WITH COMPUTER OR IN-OUT EQUIPMENT				
IN-OUT	INPUT - OUTPUT CIRCUITS	CONSTRUCT & TEST IN-OUT CONTROL & DISPLAY		CIRCUITS FOR MULTIPLE IN-OUT UNITS									
IN-OUT	PUNCHED TAPE IN-OUT EQUIPMENT	DESIGN - MODIFY & TEST TELETYPE EQUIPMENT		STUDY FINAL REQUIREMENTS			DESIGN - CONSTRUCT & TEST PERMANENT EQUIPMENT →						
STORAGE	STORAGE TUBE RESEARCH	GUN, SURFACE & LIFE STUDIES		STUDIES TO INCREASE CAPACITY & REDUCE ACCESS TIME →									
STORAGE	ELECTROSTATIC STORAGE CONTROL	COMPLETE CONSTRUCTION & TESTING											
STORAGE	STORAGE TUBE CIRCUITS	COMPLETE DESIGN - CONSTRUCTION & TEST OF CIRCUITS & POWER SUPPLIES											
STORAGE	STORAGE TUBES FOR WHIRLWIND I	PRE-PRODUCTION & TOOLING		PRODUCTION & PRODUCTION TEST OF 16 TUBES					REPLACEMENT PRODUCTION →				
STORAGE	STORAGE TUBE RELIABILITY TESTS	5 TUBES TEST & ADJUST	PERFORMANCE TESTING →										
	INSTALLATION & POWER	DESIGN - CONSTRUCT & INSTALL REMAINING MARGINAL CHECKING EQUIPMENT & BALANCE POWER							VIDEO & POWER CABLES				

LEGEND

JULY 4 11 18 25

Period of one month, comprising the total number of days in the month.

PROTOTYPE

Operation to be performed, and the estimated time allotted for its completion. Estimates made in January 1949.

Indicates extension of the work into next period.

Work done. The ratio of the length of the solid bar to the length of the open bar above it shows percentage of completion at the end of the month.

▼

Date of the latest posting.

Summary line. Shows the overall status of the project.

account of the status of storage tube development is given in Section 4.

The design of the input-output control described in Summary Report 18 is complete. One new panel has to be built; the rest of the control will be made by modifying existing panels. This design does not yet include means for selecting among the possible types of readers and recorders external to the computer or the number of units which might be used. Delivery of the Eastman film reader-recorder units, which are being furnished to us by Special Devices Center on a separate contract, is shown on the schedule as overdue. A revised delivery date for the first unit early in September will be consistent with our other plans, and will not delay our program. During the next quarter we plan to make the necessary modifications to teletype equipment to adapt it to feeding the film reader-recorders. If it should prove desirable for test purposes, the teletype equipment will be able to feed the computer directly.

In Section 6 we are including summaries of several MIT theses which are of interest in the use and applications of digital computers. It should be noted that this work was not all done during the last quarter, but the reports became available at this time. The mathematical work of the Project is now exclusively on checking and trouble-location problems. Application studies are being made under a different contract in the Laboratory.

2. SYSTEM ENGINEERING

2.1 INSTALLATION AND TESTING OF WWI

During the months of April, May, and June, the manufacture of all elements of central control and test storage was completed in our shops. These are shown in the accompanying photographs. In this period 13 different types of Whirlwind panels were built for control, 16 check-comparison register panels were completed, and 60 power distribution panels were built. With the completion of power wiring in the flip-flop storage and central control rows and the installation of the above panels, the physical array of equipment for the Whirlwind I arithmetic element, central control, and test storage is complete, although some of the panels are yet to be connected into the system. All of the above equipment has been running since the second week in June. All power control, fusing, and interlock systems are operating satisfactorily. Complete manual voltage variation for marginal checking of central control is now available, and will be complete for flip-flop storage and the arithmetic element by July 1.

Work has begun on the construction and installation of electrostatic storage equipment. Design of rack wiring for electrostatic storage control equipment is nearly completed, and wiring design for one sample digit of storage proper has been started.

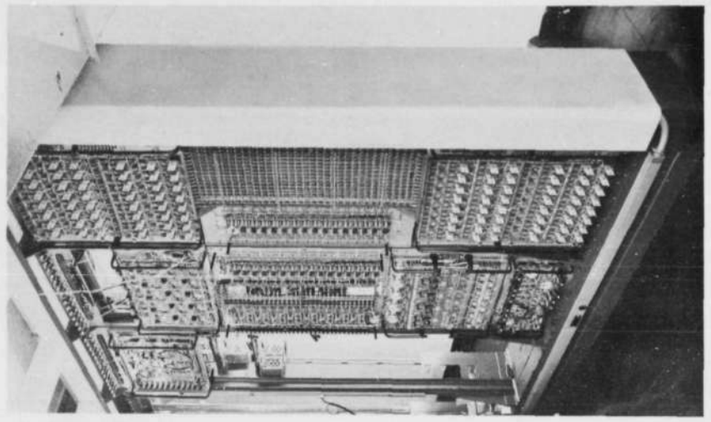
As they have become available, certain panels of central control have been added to the system. These panels, which have replaced their counterparts (made up of standard test equipment) in test control, are as follows: pulse generator, frequency divider, clock-pulse control, and time-pulse distributor.

All of these panels operated satisfactorily in the system with the exception of the time-pulse distributor. Although this unit functioned properly at high repetition rates, its output was not constant for each possible starting position after an inactive period. This was found to be caused by the method used for coupling the output gate tubes to the crystal-rectifier matrix. The coupling has been changed to one similar to that used in clock-pulse control. Although tests are not finally complete, indications are that the time-pulse distributor is now entirely satisfactory.

The five flip-flop storage registers and the check register have been installed. System tests on these registers are well under way. Some minor modifications have been made, but apparently no significant changes will be necessary to obtain the required operation.

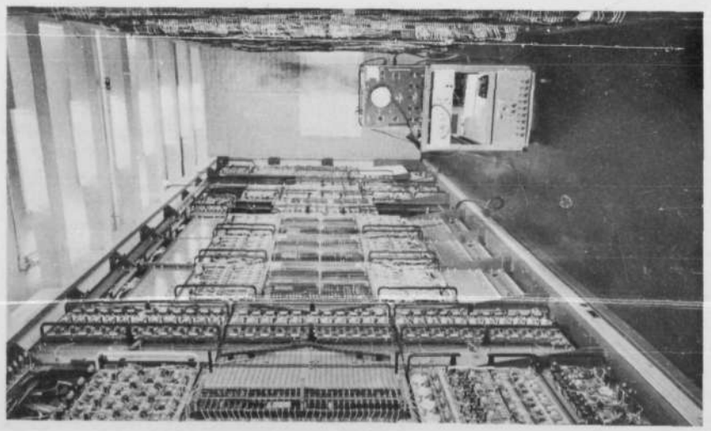
At several points in the system the available signal amplitude has been found more than sufficient, because of conservative designs. This has allowed the addition of degeneration to provide stabilization of the circuits against changes in vacuum tube characteristics. Degeneration has been added by two means, unbypassed cathode resistors and unbypassed screen-grid resistors. For example, variable resistors have been placed in the cathode circuits of the register drivers which supply restorer pulses to flip-flop registers, thus providing stabilization and variable amplitude adjustments; also, unbypassed fixed resistors have been placed in the cathode circuits of the buffer amplifers which pass add and subtract pulses from the A-register to the accumulator.

A considerable part of system test time has been devoted to measuring existing allowable limits of voltage variation in the marginal checking system. As now installed, the marginal checking system permits manual variation of the proposed variable d-c voltages. In the measurement of allowable limits, a problem is set up for periodic solution with automatic checking of solutions. The value at which correct solution fails is recorded as the maximum allowable limit. The purpose of these measurements is twofold: First, the measurements become permanent data to indicate possible future trends in component deterioration. Second, they constitute a check on over-all design. The allowable limits are in practically all cases what was predicted from individual panel data. For example, gate tube screens can be decreased 25% to 30%, in general, with correct operation maintained. It has been found that the variation of control-grid bias of



TEST STORAGE

Test storage switch (center) and toggle-switch storage equipment (right-hand rack). The latter contains 32 registers of toggle switches and associated output amplifiers.



CENTRAL CONTROL

From left to right the racks shown contain:
(1) Operation control switch, which controls
(2) the operation matrix drivers. These in turn drive
(3), (4), and (5) the operation matrix.
At the far end are mounted, in order, the time-pulse distributor, clock-pulse control, and parts of arithmetic control.

gate tubes provides essentially the same information as the variation of screen-grid voltage. Since screen-grid variation is the more convenient, control-grid voltage variation has been abandoned for the flip-flop registers to make the variation circuits available for other uses.

2.2 SYSTEM TESTING THE ARITHMETIC ELEMENT OF WWI

2.21 Introduction

The philosophy of system testing in WWI is to simulate final computer performance closely, so that problems in pulse timing as well as voltage amplitudes may be studied before the entire machine is assembled and ready for use. The arithmetic element represents only a portion of the final system function, and system tests of this section of the machine necessitate some sort of system framework.

One can see the nature of this framework if a simple comparison is drawn between the Whirlwind computer and the desk calculator. The operator of the desk calculator selects the arithmetic operation (multiply, add, divide, etc.) he wishes to have performed, inserts certain numbers from his notebook into the machine, initiates the operation, and records the answer. All of these steps, except the actual mechanical performance of the machine, are operator functions. In Whirlwind I, on the other hand, these "red-tape" functions are performed by the computer, and are thus directly related to the over-all operation of the machine. Therefore, to subject the arithmetic element (that part of the machine which does the actual arithmetic operations) to complete system testing demands a system framework which will simulate the basic red-tape functions related to the other computer elements, i.e., storage and central control.

Let us examine briefly a simplified operation cycle for the Whirlwind system so that we may see what these basic functions are. Of the operations listed below, all but No. 5 are of the red-tape variety; yet all are necessary for successful system simulation.

1. Select the operation, or order, to be performed - e.g., multiply, divide, add, etc.
2. Decide which number or numbers are to be operated on and insert these into specific storage registers.
3. Clear the operating registers of the arithmetic element of any numbers which may remain from a previous problem.
4. Read the newly selected numbers into the operating registers from storage.
5. Perform the operation selected in No. 1 above.
6. Read the answer to a check register for comparison with the proper result.

In the WWI system all the pulses which initiate and control an operation cycle will originate from a central pulse source and be dispersed through a time-pulse distributor to a control matrix. This matrix will change in its setting from order to order, and the pulses will be re-routed to carry out the specific order selected. Changes in orders will be accompanied by a change in storage-register positions so that the proper numbers and orders are selected during a computation. However, since the WWI control matrix and storage facilities are not completed, a much simpler system has been used in the last six months to test the arithmetic element. A test control has been set up (see photograph, page 9 of Summary Report 15) making use of standard test equipment. The function of the control matrix has been simulated by using a quantity of coders, but in order to change from one order to another it is necessary to stop the machine and throw appropriate toggle switches to channel the time pulses from the time-pulse distributor to the proper points in the rest of the system. In addition, a second group of coders provides two storage registers which are used to store the numbers to be used in any given operation. To change the numbers, the operator must manually change the toggle switches on the coders. Subject to these restrictions any operation can be performed on any number as in the final WWI system, with no further limitation on speed, timing, voltage, or problem-recurrence rate. Report R-161 describes the test control in detail.

2.22 How the System Framework Functions

A block diagram, Fig. 1, shows the framework used to carry out the system tests on the three

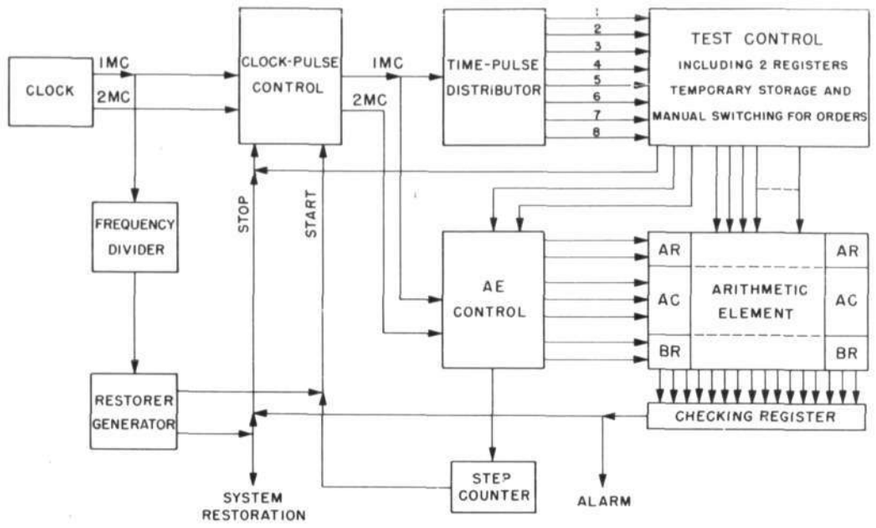


FIG. I. SYSTEM FOR TESTING ARITHMETIC ELEMENT.

registers (A-register, accumulator, B-register) of the arithmetic element. All pulses originate at the clock, or central pulse source, and are passed to CPC (clock-pulse control). The latter has the ability to start or stop the flow of pulses to the rest of the system when it is necessary. The 1-Mc pulses proceed to the TPD (time-pulse distributor) to be separated on each of eight separate lines. Each line receives one pulse every 8 microseconds when this panel works without interruption. These eight pulses originate all the operations in the system either through test control or through arithmetic control.

In the simpler operations,

ca clear and add
ad add
cs clear and subtract
su subtract
am add magnitude
cp compare,

the test control operates directly on the arithmetic element. For example, in the operation of ca, starting with the 4th time pulse from the TPD, test control routes the pulses to perform the following:

TP-4 a. Read contents of AC to bus for checking.
b. Clear A-register.
TP-5 a. Clear AC.
TP-6 a. Clear A-register.
TP-7 a. Read out contents of storage-register 2.
b. Read in to A-register
TP-8 a. Not used.
TP-1 a. Add contents of AR and AC.
TP-2 a. Perform a carry function.
TP-3 a. Perform arithmetic check.

In this sequence TP-1 and TP-2 perform the actual add operation, and the other pulses perform the so-called "red-tape" operations connected with this function. Because of the simplicity of the order, arithmetic control is not used.

The more complex operations,

mr multiply and round off
mh multiply and hold
dv divide
sl shift left
sr shift right
sf scale factor,

utilize test control to carry out the red-tape portion of the order and arithmetic control to carry out the operation. During this operation period, a pulse from test control via the clock-pulse control stops the 1-Mc pulses from entering the TPD and allows either the 1- or 2-Mc pulses to pass through the arithmetic-element control and carry on the operation directly. The step counter counts the pulses being used, and after the operation has been completed it produces an end-carry pulse which restarts the flow of 1-Mc pulses into the TPD.

A sample order mh (multiply and hold) will aid in following this activity:

TP-4 a. Preset step counter to count 15 before overflow.
b. Read out contents of AC for checking.
c. Read into check register.
d. Clear A-register.
TP-5 a. Read a number (multiplier) from storage-register 1 into A-register.
b. Clear AC.
c. Add AR to AC (delayed pulse).
d. Check correct answer in CR.
TP-6 a. Clear AR.
b. Check AC sign.
c. Clear BR.
TP-7 a. Read contents of AC to BR. (Multiplier now in BR.)
b. Read contents of storage-register 2 into AR. (Multiplicand now in AR.)
TP-8 a. Check sign of AR.
b. Clear AC.
TP-1 a. Send stop-clock order to clock-pulse control.
b. Send multiply pulse to AE control.

At this point in the program the multiply FF in arithmetic control opens and 2-Mc pulses emerge to carry out the detailed operation of multiplication. This consists of interrogating the right-most digit of the multiplier (BR), adding the multiplicand (AR), shifting the multiplier and the partial product, and repeating. The step counter counts the number of shift operations, and after 15 pulses have arrived sends a pulse to stop the 2-Mc pulses in arithmetic control and restart the original cycle at TP-2:

TP-2 a. Perform a final carry operation.
TP-3 a. Check answer in AC for proper sign.
TP-4 a. Read answer to check register for comparison with correct result.

A detailed discussion of the multiply order may be found in R-134, The Five-Digit Multiplier, and all orders are described in R-127, Whirlwind I Computer Block Diagrams.

2.23 How the System was Tested

The rather lengthy program just described represents the final performance requirements for a typical order on the arithmetic element and its control. The equipment needed to obtain these results contains some 1200 vacuum tubes and 3500 crystals and transformers, with hundreds of cables, wires, and connectors. Any component failure would prevent the system from functioning and represents a problem in location of the source of trouble. To minimize this possibility at the system level of testing, an extensive test program was carried out as outlined in Fig. 2 and described below.

2.231 Preliminary Tests

Tube Testing

Each tube was subjected to standard tests that simulated, on a d-c basis, the operating conditions and circuit performance of that section of the system in which it was to be used. Each was then subjected to a 100-hour preburning schedule at 80 percent rated dissipation, and retested to establish its stability.

Component Testing

All components were tested thoroughly

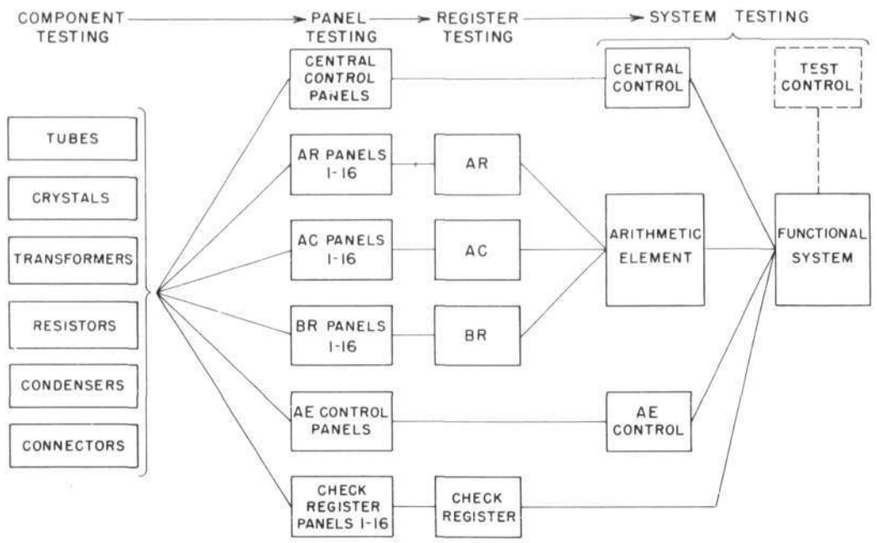


FIG. 2. OUTLINE OF TEST PROGRAM FOR SYSTEM TESTING THE ARITHMETIC ELEMENT OF WWI.

before being mounted. Crystals of various types were tested for forward and back resistance, to specifications somewhat tighter than the production specifications to which they were made. Transformers were connected into Whirlwind pulse circuits simulated by test equipment, and their behavior examined closely. Each resistor was checked for tolerance, especially those in flip-flop circuits which call for 1 percent, and coaxial connectors and power plugs were tested for proper size against a standard gauge.

Panel Testing

In the design of the Whirlwind I system, considerable thought was given to the way in which the arithmetic element was subdivided. Each digit of each register and each unit of arithmetic control was constructed on a separate panel. This resulted in a large number of subassemblies; but because of the similarity of their functions, most panels could be assembled in a high-production fashion, and quickly tested for individual performance. The method of testing was as follows:

1. Each panel first received the conventional ohmmeter and d-c voltage checks.
2. Next, the individual circuits of each panel (flip-flop, gate tube, buffer amplifier) were given specific tests in which Whirlwind I standard pulses (0.1- μsec half-sine-wave) at various amplitudes and frequencies were used. The limits on these tests were stringent and indicated whether or not the components had been damaged during assembly, whether they had been wired properly in the circuit and grounded adequately, and finally whether their tolerances lined up in such a way that the components could operate within specific Whirlwind limits.
3. The circuits of each panel were then subjected to a semi-system test which simulated closely the actual functions which the panel would perform in the final system. This test grouped the various circuits, determining the readiness of one to work into another, and at the same time checked cabling, terminations, and impedances. It also indicated definitely which panels had adequate margins of performance to be mounted directly in the system.

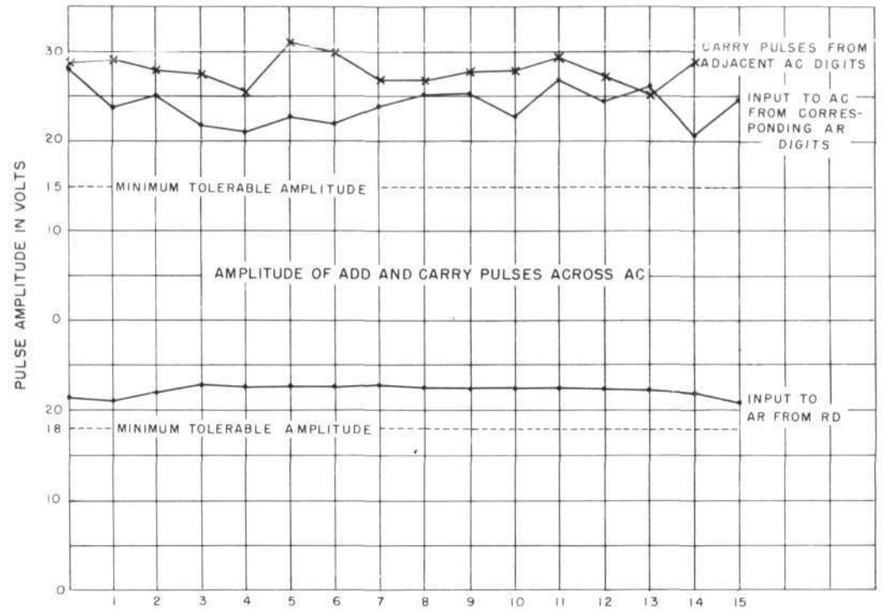


FIG. 3 AMPLITUDES OF TYPICAL PULSES IN THE ARITHMETIC ELEMENT

The individual panels which make up AE control and portions of central control shown in Fig. 1 were also subjected to this rigorous panel testing schedule. In many instances the standard test equipment provided the pulse sequences necessary for the tests; in other cases it was easier to use a completed panel as test equipment for its neighbor.

2.232 Preliminary System Testing

The next step in the testing program was to perform each operation of an order on each register in such a way as to collect data on the register while it was operating under system conditions. This amounted to sending the pulse repeatedly to each register which performs the function in question and taking the data from digits 0 to 15.

The bottom graph in Fig. 3 shows the results of a typical register test in which the amplitude of the read-from-AR-to-AC pulse is plotted against digit position. This test checks the ability of the register-driver panel (RD) to drive the 16 digits in parallel and the effectiveness of the determinations which were used in each of these control lines. The top graph in the same figure shows amplitude variations from panel to panel as these input pulses from the AR proceed to add into the accumulator and then form carry pulses in the carry register.

2.233 System Testing

System testing to date has consisted of running each order in the machine as a complete cycle and arranging the timing and recurrence rate of these orders so that quantitative data on voltage, timing, and available margins could be taken. Three types of system testing have been used effectively, each contributing different types of information.

Push-Button Testing

It is possible, by inserting single pulses into the system in place of the 1- or 2-megacycle clock pulses, to watch the step-by-step solution of a given order and assure that all cables, tubes, power wires, and indicator wires are properly in place and functioning. This test is rather qualitative in nature. It picks up glaring errors such as wrong programming or sequencing, but does nothing to locate the subtle faults due to the high pulse repetition rate. It is the starting point of all systems activity, however, and must be correct before further work can be done.

Cyclic Testing

The solution of a single order at normal WW speeds takes from 10 to 26 microseconds depending on the nature of the operation. It is impractical to view any activity within the system in such a short time without elaborate single-sweep scopes. If, however, this short solution is repeated at some audio rate of about 1000 microseconds, with the intervening period between solutions left as idle time, a dual advantage results: the repetitive nature of the solution permits oscilloscope viewing of any particular phase of the activity, and the long waiting period (974 to 990 microseconds) permits the neon indicator lights to glow, showing the state of all flip-flops in the computer at the time of solution. Thus any wrong solution shows up as an incorrect light pattern and any intermittent solution as a blinking light. Furthermore, the use of the oscilloscope makes a study of timing and voltage amplitude possible while the system is solving any problem. The ability to make this study has been the most valuable asset in this early system work. The margins in timing and amplitude represent in one respect a direct measure of the reliability one may expect from such a system, and knowing these margins it is possible to improve the weaknesses which arise before they cause serious trouble.

Figure 4 shows the results of such a study for the shift-right operation. In this problem, a number (1010101010101010) has been read into the accumulator and a similar number into the B-register. The step counter has been set to shift right two positions. This operation calls for two 2-megacycle pulses into the shift-right line, after which the step-counter end carry must return to the shift-right control and prevent the third pulse from passing through the gate in question. The diagram of Fig. 4 shows the amplitude and relative timing of the first and second pulses as they carry out this operation.

Similar studies have been made on all the operations, with particular attention to the 2-Mc operations in the multiply, shift, and scale-factor operations.

Continuous-Operation Testing

This type of testing simulates the WW final performance very closely. It is essentially the same as the cyclic method except that the waiting period has been eliminated, and 1 microsecond after a solution is obtained the cycle is started over.

Under these conditions the neon indicators change so rapidly that they cannot be of any use, so electronic pulse checking with a check register is needed. Here the checking register is set up to produce an alarm on the checking pulse if the flip-flops have received the wrong information. The alarm pulse stops further pulses from clock-pulse control and lights an error light.

The achievement of this mode of operation means that all circuits having a tendency to be frequency-sensitive must be removed from the system. To locate some of these circuits it was necessary to approach continuous operation by increasing the number of solutions from one (as in the cyclic condition above) to two to three — up to thirty or forty — and then allowing a longer wait period for recovery. This type of testing is more stringent than the final WW system operation will

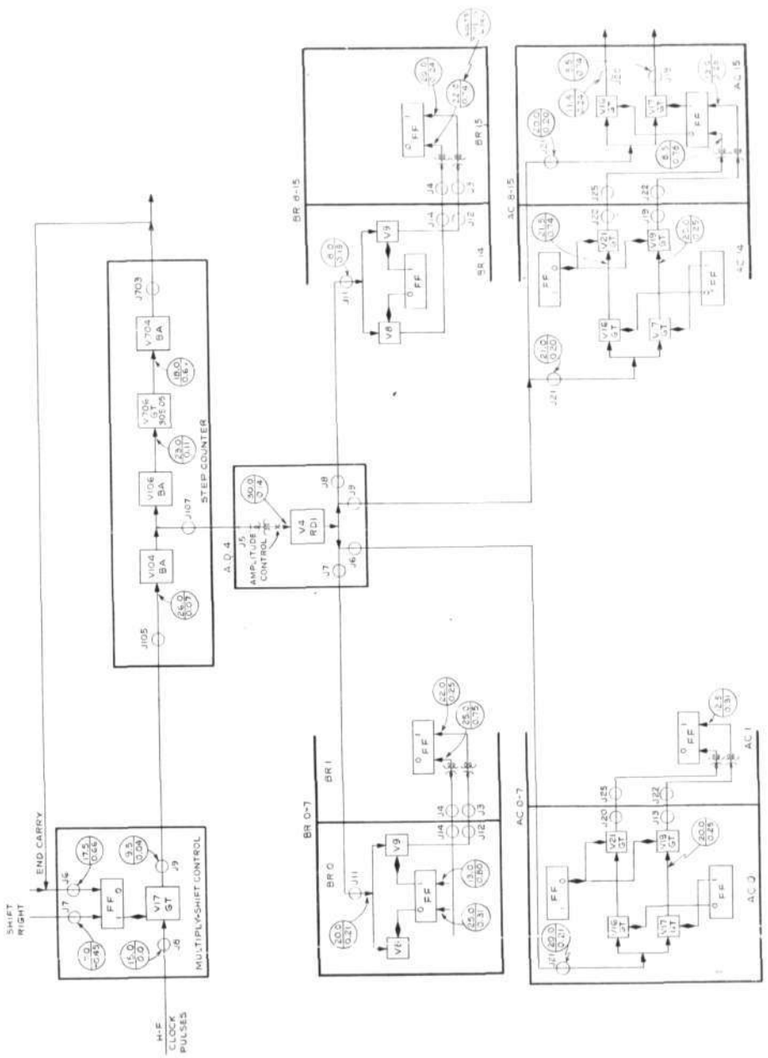


FIG. 4 PULSE AMPLITUDE AND TIMING DURING SHIFT-RIGHT OPERATION (FOR CP0, CP1)

call for, so in itself represents a margin of safety for the circuitry involved.

2.24 Trouble Location in System Operation

When trouble exists in a given operation it is not obvious from the wrong answer which pulse in the sequence is the cause of the error. The push-button technique described above can be used to locate some errors, but a much more powerful method is available by a slight modification of the cyclic testing scheme. The long waiting period may be moved from the end of the operation to a position between any two of the clock pulses used to obtain the solution, and the neon light indicators will then show the position of the flip-flops at the interim points in the solution of a problem. Thus, each operation, such as clearing the A-register, reading in numbers from storage, or the partial results in solving a given arithmetic order, may be viewed and compared with correct results while the machine is operating at normal speeds under completely normal conditions. If an error does exist it can be traced quickly to a particular pulse in the sequence; and then, in the majority of cases, the particular circuit in question can be readily isolated.

2.25 Marginal Checking

The continuous-operation type of testing is particularly useful if the operator wishes to apply marginal voltage checks to the WW system. The self-checking nature of the continuous type of operation gives an immediate failure alarm when any portion of the system fails to perform its function. In marginal checking, the design margin of selected circuits is lowered by changing voltages on pertinent tube electrodes, and thus the first failure in these circuits will sound an alarm and stop operations.

Preliminary results indicate that the marginal checking will be a powerful tool in locating weaknesses in the system, both in the early design and testing and later in reliability studies. Regarding the latter, preliminary studies of reliability are quite encouraging. No long runs of reliability have yet been made, as design tests are not quite finished and certain low margins are being improved; however, a few runs of 5 to 8 hours indicate that 10^8 solutions of a given problem with about 40 pulses per solution can be made without error.

2.3 CONSTANT-FREQUENCY RESTORATION AND THE CLOCK-PULSE CONTROL

2.31 A-C Coupling in WWI

The flip-flop is a basic electronic circuit in binary computers such as Whirlwind I. Being a balanced Eccles-Jordan circuit, the flip-flop remains in one of its two stable states for indefinite periods and is thus capable of holding a "bit" of information. Information is extracted from the flip-flop by having it control the gating (suppressor grid) potential of a gate tube to which a pulse is applied. The emergence or non-emergence of this pulse at the output of the gate tube is an indication of the static information stored by the flip-flop.

Since flip-flops may have to hold information for long periods, d-c coupling of a gate tube to the flip-flop appears necessary. As discussed in Summary Report 3, the undesirable problem of cascaded power supplies in d-c-coupled circuits has been avoided by the employment of a-c coupling and restoration. In this scheme the gate tube is coupled to the plate of the flip-flop by a capacitor, and pairs of trigger pulses (restorer pulses) are applied periodically to the flip-flop. Outside of the one-microsecond interval between the two pulses of a restorer pair, the flip-flop will be in its static state; yet the dynamic action of periodic triggering will restore the charge condition on the coupling capacitor.

The employment of non-linear resistors (crystal rectifiers) in the coupling circuit provides two widely different time constants. The long time constant allows preservation of the gating condition for the relatively lengthy period between consecutive pairs of restorer pulses, while the short time constant makes possible the rapid restoration of charge on the coupling capacitor during the short interval between the two pulses of a restorer pair. The effect of the crystal rectifiers is seen to be fundamentally a clamping action.

2.32 Original System Restoration

During restoration it is necessary to keep all affected circuits inactive; this amounts to shutting off the clock pulses that operate the computer. The original plan called for two different ways of restoration: during automatic operation restoration was to occur after each time pulse 5, while in pushbutton operation it was to be repeated at a 62.5-kc rate.

Depending on the arithmetic process being performed, the time interval between a time pulse 5 and the following one can range between 10 and 60 microseconds with test storage used at high speed. This time interval is short enough to insure reliable preservation of charge conditions on the coupling capacitors. However, the addition of electrostatic storage will lengthen this interval, perhaps appreciably at first. In addition, during manual operation the 62.5-kc restoration would interfere with the operation of electrostatic storage, which must always proceed at the same high speed. The integration of the input-output element with the system posed further problems in connection with restoration, and the restoration became too complex for the clock-pulse control to handle.

2.33 Constant-Frequency Restoration

With the so-called constant-frequency restoration system recently adopted for WWI (see M-846), only two types of restoration conditions arise. The features of this method are summarized below:

a. Regardless of the speed of operation (manual or automatic), restoration occurs at a constant rate of 62.5 kc except during electrostatic-storage (ES) operation.

b. Because ES operation must not be interrupted, no restoration is allowed to occur then. To insure proper frequency of restoration, WWI will be restored at the start of each ES operation.

c. The first restorer pulse occurs 2 microseconds after the pulse used to initiate restoration in order to allow the corresponding time pulse to complete its functions throughout the computer. This is necessary because the 62.5-kc clock pulses can occur on any time pulse, and some TP's float around for as long as 1.7 microseconds before fulfilling their mission. This delay then insures total inactivity of the computer during restoration.

2.34 The Clock-Pulse Control

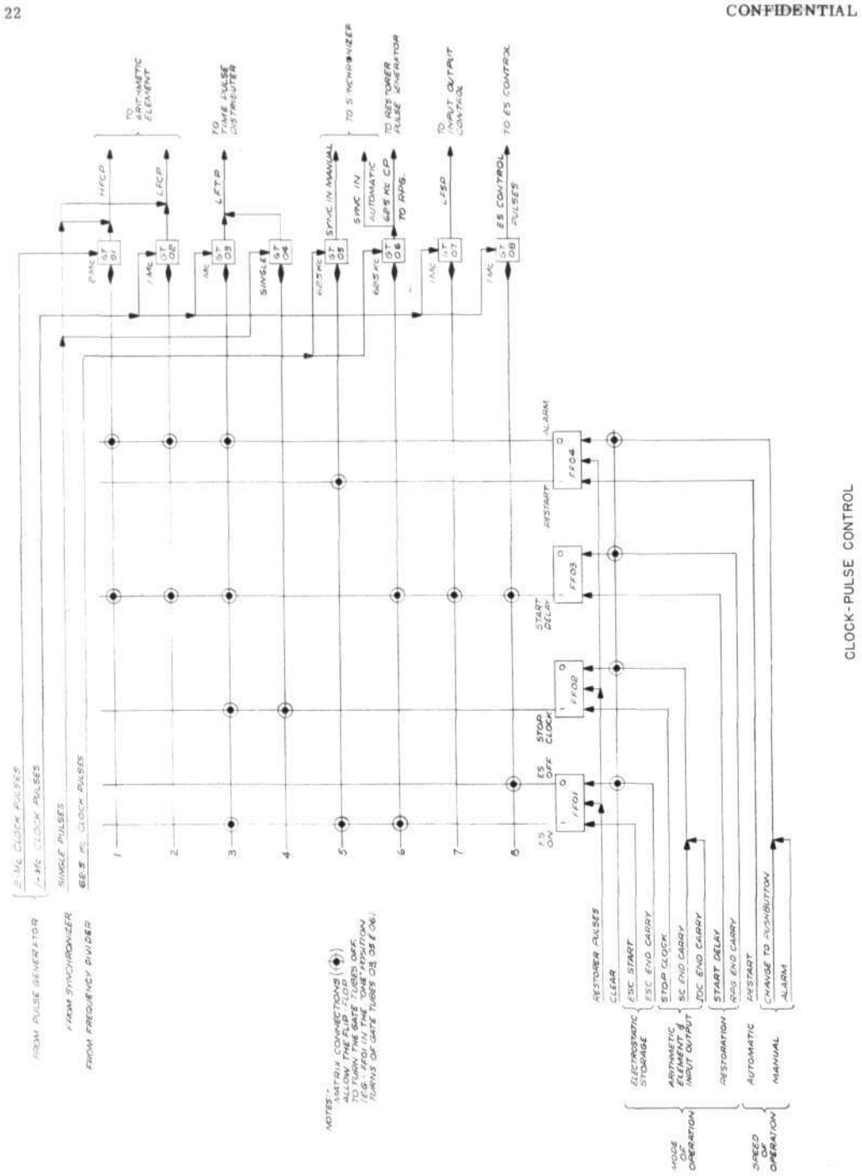
The role of the clock-pulse control (CPC), described fully in E-239 and shown in the accompanying block diagram, is to determine which component of the central control should receive clock pulses (of 2-Mc, 1-Mc, or 62.5-kc rate) and at what time. One of its functions is therefore to supply a pulse to the restorer-pulse generator whenever restoration is to be initiated. The four flip-flops of the CPC are used to remember the particular mode of computer operation at all times and to control a set of gate tubes to which appropriate clock pulses are applied. The modes of operation to be distinguished are:

1. Automatic and manual. The former is the normal high-speed operation of the computer, while in the latter, used mainly for testing purposes, a pushbutton action initiates each step of operation.
2. Restoration. During restoration all clock pulses are gated out.
3. Stop Clock. This condition amounts to the interruption of the regular timing cycle of eight 1-Mc time pulses in order to allow the performance of operations lasting variable lengths of time, such as multiplication, division, shifting, and input-output operations.
4. Electrostatic Storage Operation. In ES operation restoration is first ordered; then 1-Mc pulses are supplied to ES Control while the rest of the computer is kept inactive.

The termination of each of these modes of operation is signified by an appropriate end-carry pulse to the CPC. The constant-frequency system of restoration makes the CPC more efficient by freeing a flip-flop and making it available for remembering ES operation.

2.4 REVISED ORDERS IN THE WHIRLWIND COMPUTER

An order, which provides a basic instruction for the Whirlwind Computer, consists of two parts, an operation section and an address section. The operation section, written as a two-letter combination and converted in WWI to five binary digits, indicates what step is to be performed; the address (with a few exceptions) indicates the storage register in which the desired quantity is to be found or



CLOCK-PULSE CONTROL

stored, as the case may be. The list of operations, which has appeared with various degrees of completeness and detail in R-127, M-217-1, and Summary Report 15, has recently been revised and frozen. The official operations are now described in E-235: Description of WWI Codes; a formal R-series report is planned at a later date; and a list, with abbreviated descriptions, appears in this article. Every effort will be made to retain these operations without modification.

Since only 24 out of the 32 possible operations have been assigned, new ones may be added in the future. These new operations may simplify later use of the machine but will not change the validity of programs based on E-235.

The longest of the earlier lists, in M-217-1, described 25 operations; of these eight have been dropped, one renamed and modified, and five modified, while seven new operations have been added. Three of the four operations involving absolute values (nm, am, sm) have been eliminated. The four automatic subprogram operations (as, ax, ay, az) intended for double-length operations require more of the computer's facilities than they are worth; they have been dropped and their function largely supplanted by the modified sp operation described below. The temporary nature of the store-and-display operation (sd) has been recognized by switching it to a group of unofficial orders (indicated by the first letter q) which will be retained for testing purposes and eliminated later. The remove-order operation (ro) which originally gave indirect access to the contents of the A-register has been replaced by operation ta — transfer address — which gives a direct transfer from the A-register to storage. The sp operation has been modified so that it puts the contents of the program counter into the A-register to serve as a return address at the completion of a subprogram. This change does not affect the previous function of the sp operation. The cp operation has been changed to make it take action (i.e. act as an sp operation, including the modification) when the number in the accumulator is negative, rather than positive as before. The operations ca, cs, and cm have been modified to make them clear the B-register during each of these operations.

Six of the seven operations added are concerned with input-output. Of these six, five are described in Summary Report 18. The sixth, called ri — read initially — is intended primarily for use in starting the computer. The address section of a read-initially order is irrelevant. The operation itself will take words as they come from a film reader through the in-out register and store them in consecutive storage registers until register No. 2047 has been reached; then the reader will be stopped and the computer will start normal automatic operation, taking as its first order the first word that was read in from film. A few manual switch settings are required for this preliminary read-in process, including the selection of the register in which the first word is to be stored.

The seventh new operation has been adopted for convenience. Called ao — add one — it takes the number from the storage register indicated by the address section, adds a one to the right-most digit, performing carries if necessary, and returns the increased number to the same storage register, meanwhile retaining the increased number also in the accumulator. Thus the order ao x is exactly equivalent to the three orders ca x, ad y, ts x, where y is the address of a register which contains the quantity 1×2^{-15}. Because of the frequent need to increase the contents of a register by one, it is thought that use of the ao operation will reduce total computing time by an appreciable amount, perhaps 10% on the average and 30% or more in some cases. Several other specialized convenience operations capable of reducing computing time were seriously considered but not adopted at this time.

All these revisions were made with an approach different from that used in any of the previous modifications or additions. The original list in R-127 was made up of operations which seemed necessary or very useful and was revised and augmented from time to time with new operations which seemed useful and electronically feasible. The list of operations was always considered to be somewhat tentative; the computer had not been completed, so that modifications did not require wiring changes;

the programs that were written were largely exploratory, so that even if a modification of the code should invalidate previous programs, no real loss would be incurred. Now, however, the operation matrix is being wired up, and some definite list is needed. More important, programs now being written are intended for actual use on the computer. Modification of the matrix wiring is quite simple, but modification of long programs is difficult. Therefore the adoption of a list of operations which can be rigidly adhered to became almost imperative.

Only those operations whose future utility seems incontestable have been included, permitting the addition of other convenient operations after more experience has indicated their usefulness. It is the intention of those concerned that no revision which will invalidate any program based on this list shall be made in the present list of operations except under extreme necessity. As a consequence, all programs based on this list are to be clearly marked "in accord with E-235" to indicate that the program will always be valid for use on Whirlwind I.

LIST OF REVISED ORDERS

OPERATION				FUNCTION
Name	Code			
	Letter	Number		
		Decimal	Binary	
read initially	ri	0	00000	Take words from film until storage is full
remote unit stop	rs	1	00001	Stop reader-recorder number x
run forward	rf	2	00010	Start reader-recorder number x forward
run backward	rb	3	00011	Start reader-recorder number x backward
read	rd	4	00100	Put whatever is in the in-out register, into register x, after waiting for the next incoming word if necessary
record	rc	5	00101	Put whatever is in register x into the in-out register after waiting for the last word to be taken out
transfer to storage	ts	8	01000	Put whatever is in the accumulator into register x
transfer digits	td	9	01001	Put the right eleven digits from the accumulator into x
transfer address	ta	10	01010	Put the right eleven digits from the A-register into x
conditional program	cp	14	01110	If the accumulator contains a negative number, take next order from register x
subprogram	sp	15	01111	Take next order from register x
clear and add	ca	16	10000	Put whatever is in x into the accumulator
clear and subtract	cs	17	10001	Put the negative of what is in x into the accumulator
add	ad	18	10010	Add whatever is in x into the accumulator
subtract	su	19	10011	Add the negative of what is in x into the accumulator

OPERATION				FUNCTION
Name	Code			
	Letter	Number		
		Decimal	Binary	
clear and add magnitude	cm	20	10100	Put the absolute value of what is in x into the accumulator
special add	sa	21	10101	Add whatever is in x into the accumulator, and store any overflow to be picked up by next ca, cs, or cm.
add one	ao	22	10110	Add one to whatever is in x; store result in x and in the accumulator
multiply and roundoff	mr	24	11000	Take whatever is in x, multiply it by what is in the accumulator, round off to one register length (15 digits)
multiply and hold	mh	25	11001	Same as mr, except hold 30 digit product in accumulator and B-register
divide	dv	26	11010	Divide what is in the accumulator by whatever is in x, and leave the quotient in the B-register
shift left	sl	27	11011	Shift the contents of the accumulator and B-register left x spaces
shift right	sr	28	11100	Shift the contents of the accumulator and B-register right x spaces
scale factor	sf	29	11101	Shift the contents of the accumulator and B-register left until the first digit is a one and store the number of spaces shifted in register x.

3. CIRCUITS AND COMPONENTS

3.1 FIVE-DIGIT MULTIPLIER RELIABILITY

The life test on the five-digit multiplier (prototype arithmetic element) which is being conducted to investigate system reliability has been continued during the past three months. After the initial life run during the month of February (see Summary Report 17), several changes were made to improve operation and facilitate marginal checking and detection of errors. These included overhauling the motor-generator power supplies and rewiring of the power-supply filter and control panel, providing additional marginal-checking circuits to the test equipment being used as part of the central control in the multiplier, and inclusion of a second relay circuit for counting errors to be used in parallel with the existing one. Also during this shutdown all tubes were removed and tested and about 20 tubes which showed excessive deterioration were replaced. Following the shutdown, a period of two weeks was consumed in testing and improving the error-detection circuits. The life run was recommenced on April 1st.

The multiplication of 31 × 31 is carried out periodically at a rate of 15,000 times a second. At the end of each multiplication all of the flip-flops in the arithmetic element are sensed by pulsing gate tubes associated with each flip-flop so that if an incorrect solution exists an error pulse is produced which indexes the relay counters. An Esterline-Angus chart-type recorder connected to one of these counters is used to show when errors occur.

A summary of the results obtained during the three-month period is shown in the accompanying chart. This period represents about 2100 hours of operation. Of the 91 days covered by this test, 47 were errorless, the longest error-free run being 199 hours or about 8 days. An average of about 1 1/2 hours per day has been spent in marginal checking, trouble location, and servicing.

Most of the errors have been of a random nature so their cause is very difficult to determine. An intensive examination of all the circuits revealed several intermittent connections such as poor relay contacts, defective fuse holders, poor solder joints, and defective tube adapters. (About half of the tubes in the multiplier require adapters since loctal-base 7AD7's are being used in place of octal-base 6AG7's for which the circuits were originally designed.) There was a substantial decrease in the incidence of errors at the end of April after some of these intermittent connections were corrected (see chart).

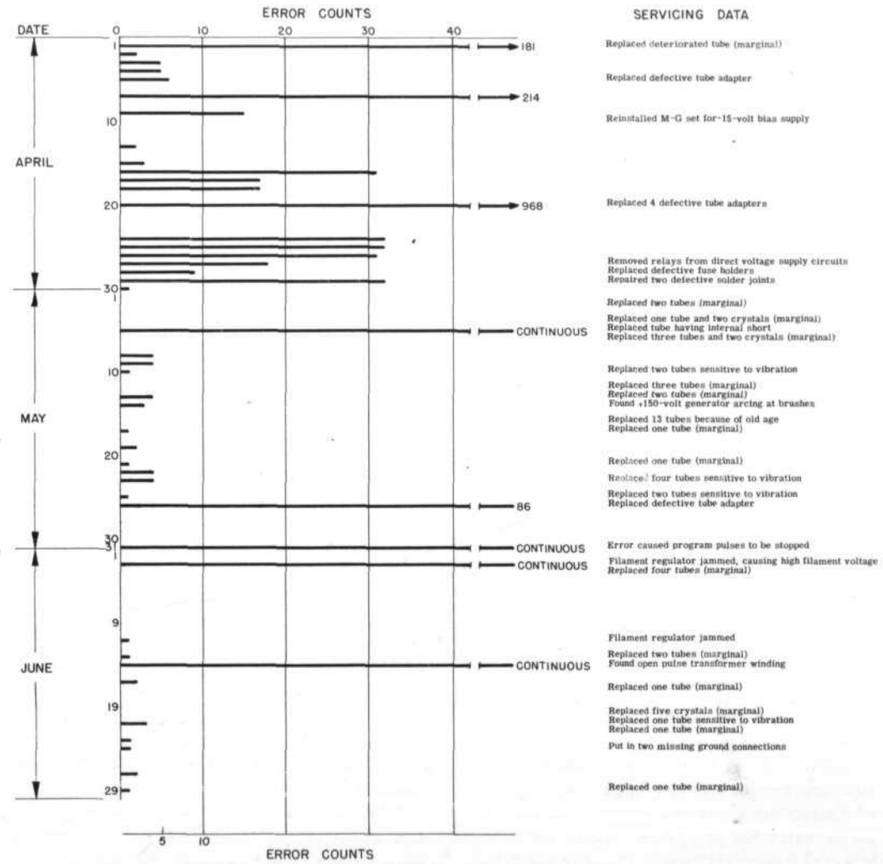
Tubes have been found to be another source of intermittent errors. Nine tubes have been removed because they caused errors when tapped lightly. These tubes were of different types and had been in use for widely different periods of time so no generalization can be made as to expectancy of this type of failure. An examination of the internal structure of some of these tubes has indicated mechanical defects such as a piece of lint, and a warped grid support. An attempt to correlate errors with vibration of the building, however, was unsuccessful.

Throughout the life test, a marginal checking procedure has been carried out on a routine basis. As a result of this checking, 23 tubes and 8 crystal diodes which had deteriorated were discovered and replaced. With a few exceptions, these replacements were made before errors occurred as a result of marginal operation. Many of the tubes removed had been in operation for more than 5000 hours.

For the last month random errors have been occurring at the rate of about one every two days. An investigation is under way to determine whether any circuits are overly sensitive to transient noise pulses. Such noise injected on the +150-volt supply line to the digit panels showed up two wiring mistakes which have existed for at least 9 months but which had not previously been detected. The introduction of pulses at other points in the system promises to be useful in determining whether some of the errors might be caused by transient noise.

Since its construction, the multiplier has been in operation for about 11,500 hours. Some 6AS6 tubes have been in use for more than 8000 hours and some 7AD7's for more than 7000 hours. Vacuum tubes are the components that have proved

to be subject to the greatest deterioration, but up to the present time there has been no conclusive indication that greater reliability will be obtained if all tubes are replaced after a certain period of life. Replacements in the multiplier have been based on marginal checking and periodic tube testing. For a larger system such as WWI it might be impractical to make static tests on the tubes, in which case their wholesale replacement after a certain length of time would be indicated.



FIVE-DIGIT MULTIPLIER PERFORMANCE

3.2 LIFE OF VACUUM TUBES IN WWI

3.21 Failures in WWI

The project policy of very carefully checking vacuum tubes before installation has resulted in a relatively low number of failures during the first 1000 hours of operation of the WWI arithmetic element. Out of about 1200 tubes, 8 tubes have become unsatisfactory for use, as shown in the accompanying table.

FAILURES OF VACUUM TUBES IN WWI

Tube Type	Total No.	No. of Failures	Hours of Service	Comments
7AD7	500	2	7	Gassy
			595	Bad cathode
7AK7	525	3	3	Shorted
			905	Shorted
			128	Changed characteristics
3E29	14	1	438	Open filament
6SN7	100	2	42	Shorted
			227	Shorted

Most of these failures were probably due to structural defects in the tubes; however, the 7AD7 with a bad cathode is representative of a type of failure which has plagued this Project before (see below; also Summary Reports 17 and 18 and Report R-139).

3.22 Vacuum Tube Life Tests

At the present time special tubes manufactured by Sylvania, RCA, and Raytheon are on life test. The tubes manufactured by Sylvania and RCA have cathode sleeves of various degrees of impurity, while those manufactured by Raytheon have cathode sleeves which have had no impurity added. No information is available as yet on the RCA tubes, which are type 6AG7, or on the Raytheon tubes, which are type 6AN5. Both these lots have approximately 1000 hours of aging at present. The Project is fortunate in having obtained these three special lots of tubes, which may contribute considerably to the understanding and cure of the problem of apparent cathode interface resistance.

Three groups of special 7AD7 tubes made by Sylvania have operated over 2500 hours. Data taken to 2500 hours show very little change in plate current on d-c test. Under pulse-test conditions, some tubes show the formation of apparent cathode interface resistance. Of ten tubes made with 599 "active" alloy cathode sleeves, eight show some formation. Of ten tubes made with high-purity 499 "passive" alloy cathode sleeves, two show some formation. Thirty special tubes made with Sommers "A" alloy cathode sleeves show essentially no formation of apparent cathode interface resistance.

The 7AD7 tubes in WWI are largely of F8B production lot. Three groups of tubes from this F8B lot are on life test with different heater potentials. A group operated with 8 volts on the heaters has shown considerable apparent cathode interface resistance and also some loss of emission at 2100 hours. Another group operated at the normal heater potential of 6.3 volts has shown little change in 2500 hours; however, pulse tests indicate some apparent cathode interface resistance. The third group, operated for 1500 hours with a heater potential of 5 volts, has shown no change as yet. It appears that formation of apparent cathode interface resistance is accelerated at high cathode temperatures and possibly retarded at low temperatures.

3.3 FAILURES OF COMPONENTS IN WWI

The following failures of electrical components (exclusive of tubes) have occurred since operation of the computer started last December. Tube failures are treated under 3.2.

Component	Total No.	Type	No. of Failures	Hours of Service	Comments
Choke	550	50 μh	1		Open because of mechanical damage; found by marginal checking.
Crystal rectifier	3000	D-357	1	783	High forward resistance.
		D-358	2	739	Between grid and cathode of a 7AD7 cathode follower tube; low back resistance.
				748	Clamping crystal in divide control panel; unstable back resistance; found by marginal checking.
Power plug	100		1		Loose pin.
Pulse transformer	1200	1:1	1	327	Open secondary.

4. ELECTROSTATIC STORAGE

The original specifications for the WWI storage tube called for storage of a 32 × 32 array of elements in each tube with an access time of 6 microsecs. A no less important specification called for high reliability. It has been apparent for some time that in order to maintain reliability and yet meet production dates for WWI, the performance specifications would have to be reduced to storage of a 16 × 16 array with an access time of 20 microsecs.

This reduction is not considered serious. The important problems to be met first are those of reliability, reproducibility, and life. The quantitative change to the higher performance will be carried out after the initial WWI production. One set of 16 tubes, with spares and replacements, storing 256 words with an access time of 20 microseconds will serve the purposes of WWI for many months. The present time schedules call for the production of such tubes to start in October 1949.

4.1 TUBE CONSTRUCTION

The storage tube construction group is at present engaged in building a production run of experimental tubes. Until this last quarter the design of the tube has been in a continual state of change, largely in detail; no two tubes had been built which were even theoretically identical. It has therefore been difficult to dissociate the effects of these known differences from the effects of uncontrolled differences. Such a procedure was reasonable considering the many small problems involved in the development.

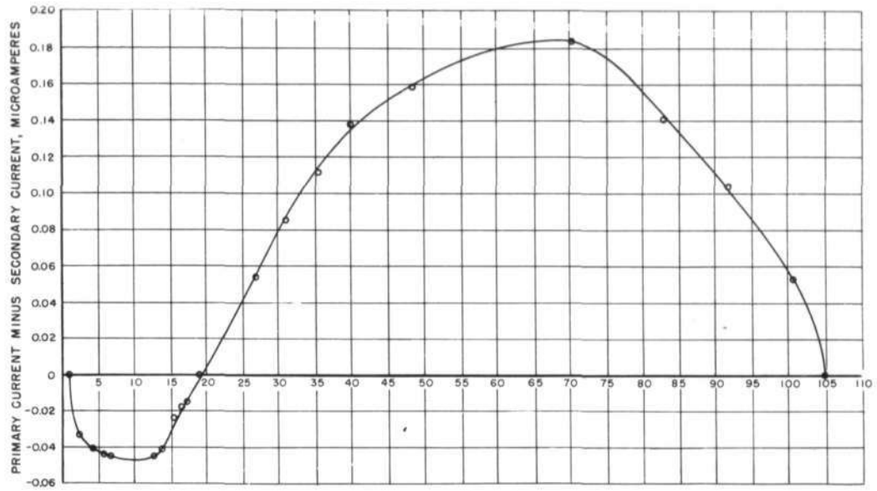
Early in this last quarter we were able to build a number of tubes with consistently good surfaces. One in particular (ST96) met our preliminary performance specifications and operated successfully in all our test setups. The time had arrived when the detailed constructional specifications for this tube should be written and all our techniques scrutinized in order to overcome previously uncontrolled differences, especially those due to contamination.

The storage tube contains many parts. The problem of consistent reproduction lies not only in the mechanical construction, assembly, and alignment of these parts but even more in the care with which they are cleaned and handled. The many man-hours of hand-assembly time present endless possibility for the introduction of dust, lint, and contamination. Equally endless care is required if the resulting tubes are to have high vacuum, long-lived cathodes with high emission, and lint-free storage surfaces with uniform secondary-emission characteristics and low surface leakage.

The efforts of the construction group for about half the quarter have gone into the preparation of specifications and improvement of techniques. Every detail of the construction has been reported in writing and the construction subsequently followed by independent observers in order to discover inadvertent deviations from standards. The construction and alignment of parts has been improved by jigs and fixtures. Washing procedures have been improved and standardized for the July production, and a vacuum firing system built to give us greater control over this important step. The specifications are now complete in rough form; polishing and minor changes should be complete in about a month.

The experimental production began shortly before the end of the quarter. Three tubes have been built. The first was satisfactory except for an area on the storage surface about 5/8 inch in diameter which was mechanically damaged. The second tube was a very reassuring duplicate of ST96. The third tube had a contaminated surface traced to improper cleaning. Although one good tube out of three may not seem a high percentage, we expected to lose the first few until the new procedure became smooth working. It was heartening to learn that ST96 could be duplicated; that its performance was not partially fortuitous.

The present plan is to continue the run during July, with a scheduled production of 6 to 8 tubes. Upon their completion we should know where we stand on reproducibility. The construction group will take the first two weeks in August as a vacation. Then about six weeks will be available for studying changes in specifications and techniques



HOLDING GUN STABILITY CURVE

before October 1, the date when production for WWI must start.

One present result of the above program is an improvement in the pressure of the storage tubes after seal-off by a factor of 10 to 100 due to better preparation of the metal parts. This improvement coupled with the use of getters (exonerated, when carefully used, of having any bad effect on the storage surface) should minimize difficulty with gassy tubes.

4.2 TESTING

4.21 Static TV Test

Since only a few tubes were built during this period, the TV unit has been available for special tests and the routine testing of tubes on life runs. The special tests have covered such matters as the causes of the upper stability limits of holding-gun voltage (see E-242) and the effects of increased holding-beam density. The life-test work is reported below.

4.22 Automatic Write-Read Test

Successful techniques have been worked out with the write-read unit for measuring charging rates under the holding beam. The method consists of charging a spot to a selected voltage, allowing the holding gun to operate for varying lengths of time, and then measuring the resulting potential of the spot by adjusting the signal-plate read gate for an output signal null. The derivative of the resulting curve gives the holding stability curve for that spot. This stability curve (see accompanying sample curve) shows the restoring current available for all spot voltages. The restoring current available to maintain negative spots is much less than that available to maintain positive spots. The general shape of this curve is easily deduced from secondary-emission measurements and theoretical consideration. The true shape of this curve, including second-order effects, is obtained by the method outlined above.

4.23 Reliability Tester

Successful runs of from 10 to 40 hours without error have been obtained with several tubes including ST96. In general, failures have been traced to test-equipment and power-supply troubles. Unfortunately, the entire equipment is not in itself sufficiently reliable to obtain really adequate life data. There are more than 500 vacuum tubes in the equipment, with no provision for either marginal or continuous checking to discover the exact cause of intermittent error.

Considerable emphasis has been placed on performance testing of storage tubes, approaching the reliability problem from the additional angle of determining limits and safety factors for short-time satisfactory operation. These tests have included spot spacing, spot interference, spot size under various conditions, special cycling patterns with unrestored spots, holding-gun effects, background effects, and charging rates.

The results show that the present design should be satisfactory for 16 × 16 arrays, although a somewhat smaller high-velocity beam diameter would produce a worthwhile improvement in safety. A 32 × 32 array will require substantial work on the design of the tube. We do not expect to have experimental models of such a tube before the computer is working with a set of 16 × 16 tubes.

The changeover from 1 to 5 tubes is still in progress and nearly complete. The decision was made not to tear down the whole unit and reassemble it for 5 tubes, but to make the change gradually, leaving the 1-tube unit working except for shutdowns of not more than a day. This method has worked well. The ability to check the changes as they are made has been valuable. It is expected that the additional tubes will not only provide more information on tube differences but will also help to distinguish between equipment and control failures.

The 5-tube system should be ready in July. The WWI electrostatic storage control should be installed in the computer room during August and will be available for prototype and reliability runs, leaving the reliability tester for performance tests.

4.24 Electrostatic Gun Tests

Several research tubes for gun studies have been built, and the velocity and current distribution of the present holding and high-velocity guns and some other high-velocity guns have been measured. This work is being carried on as a master's thesis. There have been a number of interesting results which will be reported at the end of the next quarter when the thesis is complete. At present a new beam-analyzer tube is being built containing a 5UP gun modified to give a smaller spot with more uniform current distribution.

As mentioned above, work is in progress on the design of high-velocity guns with smaller spot diameters, more uniform current densities, and higher current densities than the present unmodified 5UP gun. A study of holding guns giving much higher currents than the present 3 to 5 ma is also under way. Some studies have been made on the possibility of leaving the holding gun on all the time, which would make the design of the gun much easier. These tests plus planned life tests are made using the present holding gun with a magnetic concentrating coil.

4.25 Secondary Emission Tests

Another master's thesis which has been started has as its purpose to study the secondary-emission characteristics of surface materials at low primary voltages. A first tube has been built using a test surface of solid metallic beryllium. Later tests will use composite surfaces and rotatable surfaces for measuring the effect of striking angle. Data have been taken in the past on secondary emission under high-velocity and holding-gun voltages; the purpose of the present tests is to make the more difficult measurements at primary voltages below first crossover. These data in combination with the holding-stability data mentioned above should be of great value in designing tubes for higher densities and higher speeds.

4.26 Life Tests

No failures have yet occurred in the 8 tubes in the life rack. The secondary emission of the surface seems to rise at first and then flatten off at somewhat below its original value after several hundred hours. The high-velocity gun seems to have little effect on the surface. A pattern stored under the holding beam for a long time produces a prominent after-storage; this, however, does not affect the tube's usefulness and may be completely removed by having the entire surface positive under the holding beam for a few hours. At present, one tube has run 3300 hours, 3 others more than 1800 hours.

4.3 STORAGE TUBE CIRCUITS

The circuit design is on schedule and should be complete and installed by the first of the year. A prototype mount has been built complete with adjusting circuits and tested with one of the new tubes. The remaining prototypes for both one-of-a-kind or multiple gun drivers and gate generators, etc., are undergoing test. The deflection circuits and transmission line are under construction. The complete control should be installed in August. The plan is to use this control for testing the digit prototype instead of using the reliability tester in the basement.

A new input circuit to the r-f amplifier has increased its gain and improved its rejection of switching transients. The r-f pulser is under construction.

5. INPUT - OUTPUT

Information on the input-output system will be found in the Quarterly Review, Section 1.

6. MATHEMATICS & APPLICATIONS

6.1 CALCULATION OF CORRELATION FUNCTIONS

In recent years there has been built up (notably by Prof. Norbert Wiener) a very considerable theory of information leading to new techniques in prediction and filtering. In particular, it is possible to design practical electrical filters with optimum filtering characteristics for a signal whose general nature is fairly uniform and whose past history is known. Furthermore, there appears to be much promise in accurate long-range weather forecasting making use of past weather observation through the theory of prediction.

In both the electrical and the meteorological cases as well as in any other application of the theory it is necessary to evaluate what are called correlation functions for the given time series (where the series may be a television signal or a set of weather observations). Because of the statistical nature of the time series involved (the correlation functions for known analytic functions of time are generally easy to calculate but useless), the calculation of correlation functions is a numerical calculation of such magnitude that it is impractical for hand computation but well suited for high-speed calculating machines.

A correlation function is in a sense a function of a function. To any time series G(t) there corresponds a particular autocorrelation function $C_{GG}(\tau)$ - i.e. a function of a delay time - and to any two time series G(t) and H(t) there corresponds a cross-correlation function $C_{GH}(\tau)$. By definition the cross-correlation of G(t) with H(t) at the time τ is the time average of the product of G(t) with H(t - τ) - i.e. the average of G times H with H delayed by a time τ. More rigorously,

$$C_{GH}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} G(t)\, H(t-\tau)\, dt.$$

The autocorrelation function is simply

$$C_{GG}(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} G(t)\, G(t-\tau)\, dt.$$

An equivalent form results from replacing the infinite integral by an infinite sum, which is permissible if the time series are stochastic functions. Then the crosscorrelation function becomes

$$C_{GH}(\tau) = \lim_{N\to\infty} \frac{1}{N} \sum_{i=1}^{N} G(t_i)\, H(t_i - \tau).$$

In order to calculate the value of $C_{GH}(\tau)$ for any one value of τ, one must find the average of an infinite number of products, a patent impossibility. It can be shown, however, that a good approximation can be obtained by finding the average of perhaps 10,000 products. To define $C_{GH}(\tau)$ fairly well for values of τ near zero (generally $C_{GH}(\tau)$ is very small for τ very large unless G and H are periodic with a common period), it is necessary to repeat the above calculation for several hundred different values of τ. Consequently, to evaluate $C_{GH}(\tau)$ one must form from 1,000 to 100,000 products for each of 100 to 1000 values of τ, requiring from 100,000 to 100,000,000 multiplications and additions.

It is interesting to examine how a calculation such as this one would actually be programmed for the Whirlwind computer, paying particular attention to the handling of the film readers and recorders which will be used for input and output. Before proceeding to these details of programing, however, we must clearly understand the mechanics of the problem.

Suppose that two time functions are given - perhaps G(t) is the barometric pressure at Boston and H(t) is the barometric pressure at corresponding times in New York - represented by observations taken at equally spaced intervals of time. Thus, G(t) and H(t) might be given as the barometer

readings in millibars taken at noon every seventh day from January 1, 1907, to December 31, 1946. Thus a table of values could be prepared (subtracting a normal pressure of 1000 from each reading to emphasize the fluctuation):

Date	Boston	New York
1 Jan., 1907	G (1) = 20	H (1) = 19
8 Jan., 1907	G (2) = 17	H (2) = 30
15 Jan., 1907	G (3) = 14	H (3) = 22
22 Jan., 1907	G (4) = 23	H (4) = 16
.	.	.
.	.	.
.	.	.
17 Dec., 1946	G (2085) = 36	H (2085) = 25
24 Dec., 1946	G (2086) = 27	H (2086) = 28
31 Dec., 1946	G (2087) = 33	H (2087) = 26

Now, to find $C_{GH}(\tau)$ for $\tau = 0$, it is necessary only to form $\frac{1}{2087} \sum_{t=1}^{2087} G(t)\, H(t)$. That is, one adds up 20·19 + 17·30 + 14·22 + 23·16 + . . . + 36·25 + 27·28 + 33·26 and divides the sum by 2087 to obtain some number, perhaps 631. Then to find

$$C_{GH}(1) = \frac{1}{2086} \sum_{t=2}^{2086} G(t)\, H(t-1),$$

one adds up 17·19 + 14·30 + 23·22 + . . . + 27·25 + 33·28 and divides by 2086 to obtain perhaps 598. Notice that only 2086 values could be used, for G(1) cannot be used since there is no value H(0) to pair with it. Similarly, only 1987 products can be used in computing $C_{GH}(100)$. It is also necessary to compute C_{GH} for negative values of τ. Notice, however, that

$$C_{GH}(3) = \frac{1}{2084} \sum_{t=4}^{2087} G(t)\, H(t-3)$$

$$= \frac{1}{2084} \sum_{t=1}^{2087} H(t)\, G(t+3) = C_{HG}(-3)$$

Therefore, by calculating C_{GH} for positive values of τ and then reversing the roles of G and H and calculating C_{HG} for positive values of τ, it is possible to obtain the cross-correlation for both positive and negative values of τ without using any more data than for positive values alone.

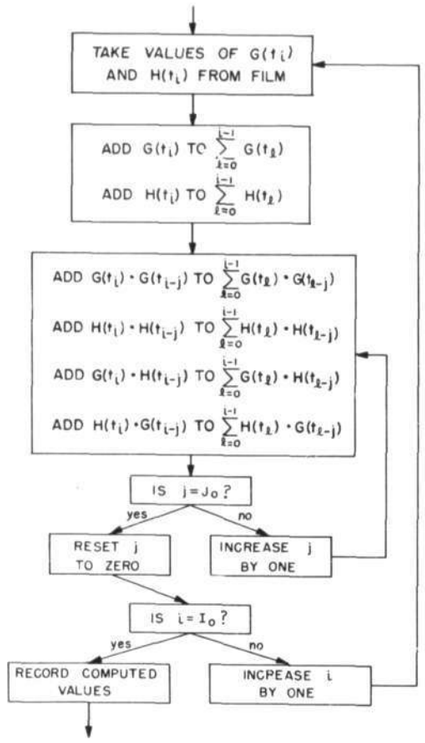
A mechanized procedure can be built up as a flow diagram for actual programming. It will be more convenient to start forming each sum at some particular value of t (in the example, $C_{GH}(0)$ used $\sum_{t=1}^{2087}$, $C_{GH}(1)$ used $\sum_{t=2}^{2087}$, and $C_{GH}(100)$ used $\sum_{t=101}^{2087}$), so that if the function is to be calculated for values of τ up to Jo, it is convenient to start numbering the data at t = -Jo + 1 so that all the sums can then be formed as $\sum_{t=1}^{Io}$ where Io + Jo is the total number of points (in the example, Jo would be 100 and Io would be 1987 and the sum would always be started with what was formerly called G(101)).

Suppose that the cross-correlation is to be calculated for $\tau = 0, \pm 1, \pm 2, \ldots, \pm$ Jo and the autocorrelations of both G and H are to be calculated for $\tau = 0, 1, 2, \ldots,$ Jo and suppose that Jo + Io binary values of G and of H are stored, each on a separate reel of film (it is assumed that the numbers have all been scaled so that the largest is just less than one in magnitude). It will not be possible to put all the data into the high-speed storage of the computer at once, because there may be many thousand words of data.

Suppose that at first the Jo values of G and of H, i.e.

G(-Jo + 1)	H(-Jo + 1)
G(-Jo + 2)	H(-Jo + 2)
G(-Jo + 3)	H(-Jo + 3)
.	.
.	.
.	.
G(0)	H(0)

are in storage. Then the values of G(1) and H(1) are taken from film as shown in the first block of the accompanying flow diagram. G(1) and H(1) are stored, becoming the first terms in the summations indicated in the second block of the flow diagram.



FLOW DIAGRAM, CORRELATION PROBLEM

By adding each value of G and of H into the running sums, the computer finally obtains the sum of the G's and H's from t = 1 to t = Io, from which the average value of G and of H can be found. This is really a convenient by-product, not an essential part of the computation.

The main block in the flow diagram shows the calculation of one term of each of the four sums which will eventually form the four values $C_{GG}(j)$, $C_{HH}(j)$, $C_{GH}(j)$, and $C_{HG}(j) = C_{GH}(-j)$ respectively. Now the same calculation can be repeated for the next value of j, and so on until all values j = 0, 1, 2, . . ., Jo have been used. Then the value of G(2) and H(2) must be taken from film, but G(-Jo + 1) and H(-Jo + 1) are no longer of any use and may be discarded. The whole cycle is repeated, G(3) and H(3) are taken from film and G(-Jo + 2) and H(-Jo + 2) are discarded, and so on until G(Io) and H(Io) have been used, at which time the calculation is complete and the results are recorded on film.

Actually the accumulation of the products requires the use of two storage registers to store the sums in order to prevent the round-off error from becoming large.

In practice also, the data will be taken from film not one word at a time as indicated in the flow diagram, but in blocks of fifty or more words (to minimize the amount of time used in accelerating and decelerating the film). Using blocks of words from film does not change the basic principle of the program. Instead of taking a new word and discarding an old word each time the major cycle is repeated, the program takes fifty new words and discards fifty old words every fifty major cycles (of course an extra fifty registers must be used as a sort of buffer storage since the new words must be taken in at the beginning of the fifty cycles and the old words cannot all be discarded until the end of the fifty cycles).

The detailed programming, including the double-length additions and the handling of data in blocks, is dealt with in greater detail in E-246; a possible final form of this program for WWI is reproduced herewith for purposes of illustration. The Whirlwind computer will be able to perform the required calculations, including all "bookkeeping" operations, at a rate of from 1000 to 3000 multiplications per second, depending on the final operating rate of the storage element. The minimum 100,000 multiplications could be performed in less than one minute, while 100,000,000 multiplications might require about one day. The calculation is already being performed by the MIT Center of Analysis, using

FINAL FORM OF PROGRAM, CORRELATION PROBLEM

	0050	0075	0100	0125	0150	0175	0200	0225
1	CA 0229	CA 1241	SL 0015	AD 0225	RS 0001	CA 1845	RT 0049	-
2	TS 0191	TS 1241	TS 0217	TD 0070	TD 0066	RF 0002	TS 1845	RT 0236
3	SP 0167	CA 0937	RC 0217	TD 0071	TD 0078	CS 0226	CA 0587	RT 0636
4	AD 0216	MR 0587	AD 0097	AD 0220	SP 0060	TS 0214	SA 1847	SP 0054
5	CP 0167	SA 1544	TD 0099	TD 0068	AD 0214	RD 0217	TS 1847	RT 0011
6	CS 0230	TS 1544	AD 0097	TD 0069	CP 0191	AD 0218	CA 1846	AD 0198
7	TS 0216	CA 1543	AD 0215	AD 0225	CS 0226	SU 0217	TS 1846	RT 0005
8	CA 0232	TS 1543	CP 0097	TD 0076	TS 0214	DV 0219	CA 0060	D
9	TS 0191	AD 0215	RS 0003	TD 0077	AD 0072	AD 0185	AD 0221	D
10	CA 0237	CP 0120	CS 0226	AD 0220	SU 0222	RD 0437	TS 0060	D
11	MR 0587	CS 0227	TS 0215	TD 0074	CP 0167	AD 0214	CA 0205	D
12	SA 0638	TS 0215	AD 0216	TD 0075	CA 0227	CP 0156	SP 0120	-
13	TS 0638	CA 0213	CP 0095	AD 0225	TD 0198	RS 0002	D	-
14	CA 0637	SU 0233	SP 0115	TD 0082	TD 0173	CS 0226	+.001495	-
15	TS 0637	CP 0155	CS 0232	TD 0083	AD 0225	TS 0214	+.001526	-
16	CA 0437	CA 0214	TS 0215	AD 0220	TD 0185	AD 0198	+.000092	-
17	MR 0587	SU 0234	CA 0223	TD 0080	RF 0001	TD 0061	-	-
18	SA 0940	CP 0155	TS 0114	TD 0081	RD 0217	TD 0079	D	-
19	TS 0940	RF 0003	SP 0094	AD 0060	AD 0213	AD 0225	.000000	-
20	CA 0939	RC 0235	AD 0062	SU 0222	SU 0217	TD 0203	RT 0001	-
21	TS 0939	AD 0235	TD 0064	CP 0149	DV 0219	TD 0067	RT 0050	-
22	CA 0237	CA 0638	TD 0065	AD 0227	AD 0173	TD 0073	CA 0436	-
23	MR 0587	SR 0015	AD 0220	TD 0060	RD 0237	CA 0587	RS 0000	-
24	SA 1242	AD 0637	TD 0062	CA 0060	AD 0214	SA 1846	RT 0500	-
25	TS 1242	DV 0236	TD 0063	TD 0072	CP 0173	TS 1846	RT 0200	-

IBM calculators, at a rate of about 5 multiplications per second.

A specially designed single-purpose analog calculator has been built by the RLE group at MIT, and a digital machine (also single-purpose) is being built, both capable of performing the multiplication at a rate of 500 per second. As one would expect, the very straightforward calculation is well suited for solution on special-purpose machines, and the efficiency in terms of cost is somewhat higher than that obtained from the more versatile large-scale, general-purpose computer. In such cases the main question is whether or not enough calculations of a given type are needed to justify building a special machine. It seems that demand for correlation functions is sufficient to warrant construction of special-purpose machines.

6.2 INVESTIGATION OF THE GAUSS-SEIDEL ITERATIVE METHOD

With the advent of the digital computer, it may be expected that increasing accent will be placed on iterative methods in numerical analysis. The most important problem arising in this connection is that of finding under what conditions the iterative process converges to the correct solution. Some interesting results have been obtained in a study of the Gauss-Seidel method for solving systems of simultaneous linear algebraic equations by successive approximation. The work was undertaken towards a Master's thesis in the MIT department of Mathematics; it is fully described in Report R-165.

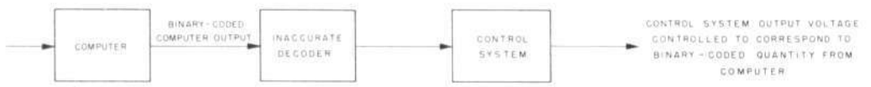
It has long been known that the Gauss-Seidel process will converge for the case where the system matrix is symmetric and definite. Furthermore, it can easily be shown that if the process converges stably for a given system, using a certain initial guess, it will converge for that system with an arbitrary initial guess (such as assuming all unknowns to be identically zero). By stable convergence is meant convergence that will not be transformed into divergence if the ordinary arithmetical operations are replaced by an arithmetic involving round-off.

Although many physical boundary-value problems, such as those occurring in electric network theory, mechanical framework theory, statistics, and field theory, lead to symmetric, definite matrices, it may very well be necessary at times to solve a system whose matrix is either non-symmetric, or symmetric but not definite. One way of avoiding the difficulty is to premultiply the system of equations by the transpose of its matrix, an operation which always results in a symmetric, definite matrix. This requires about half the number of operations needed for matrix multiplication. A partial investigation was carried out to discover whether this rather expensive way out was actually necessary. It was demonstrated that when the system matrix is real and symmetric, and has either only positive or only negative terms on its main diagonal, premultiplication is necessary in order to provide definiteness. For other types of matrices the question still remains open.

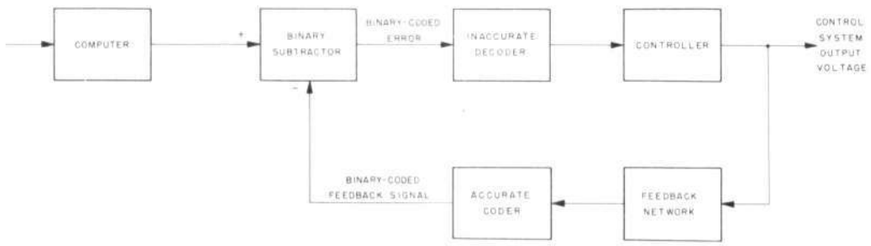
6.3 CONTROL SYSTEMS TO OPERATE WITH THE WW COMPUTER

One significant characteristic of the output data from a digital computer is that is is sampled rather than continuous. When control systems operate from computer data they must operate from control information supplied at discrete intervals of time, rather than from information supplied continuously. The problems arising when the error data of a closed-loop control system are supplied from the computer were the subject of a recent MIT doctorate thesis written between May 1948 and March 1949. The thesis is briefly described in this article, and published in full as Report R-170.

Such a control system might be used, for example, to maintain a physical quantity such as a terminal voltage, a shaft position, a force on a lever, or a recording pen position at a value to correspond to the computer output. Normally the physical quantity would be controlled by some type of servo system which would operate from the computer signal. The fact that the computer signal is a binary-coded quantity means that a binary-to-analog decoder would be needed. At present the difficulties in building an analog-to-binary coder with acceptable accuracy seem less than those in building the decoder. The stringent accuracy requirements on the decoder might be relieved by having it decode the error signal in a servo system rather than the actual input quantity. The desirable modification is shown in the accompanying block diagram.



(a)



(b)

A CONTROL SYSTEM (a) WHICH PUTS STRINGENT ACCURACY REQUIREMENTS ON THE DECODER AND ONE (b) WHICH RELIEVES THESE REQUIREMENTS

This problem and numerous similar ones will be encountered in the application of the digital computer to practical problems. The analysis and design of servo systems with sampled-error data seems to include almost all the problems of sampled-input-data control systems (those without feedback around the computer element), and in addition an interesting stability problem arising from the feedback.

This investigation emphasizes the servo problem, but the techniques developed apply readily to any sampled-data system. The primary object of this study was to evolve an analysis of sampled-error-data servomechanisms which would be useful in system design. A sampled-data system has a sampling device at some point in the transmission. A sampling device has an output which is related only to samples of its input taken at instants, equally spaced in time. If $\theta_i(t)$ be the input signal to the device, then the output is related in a linear fashion to $\theta_i(nt_r)$ where n is any integer, and the constant t_r is the length of time between samples.

When the sampling device is put in the feed-forward section of a servomechanism, special stability problems arise which are not present in the conventional servomechanism with continuously supplied error data. When the computer is used in a control system, the computer contains the sampling device. This is evident because the computer output is related to only discrete samples of the computer input data.

A procedure using linear difference equations to analyze sampled-data systems was worked out some time ago (Ch. 5, Theory of Servomechanisms, James, Nichols, and Phillips; New York, 1947.) in connection with war work. While this procedure is perfectly correct, it is cumbersome to use because it does not give system response characteristics directly in terms of element characteristics. Because of the difficulty in applying it, it is useful only to determine whether or not a given system is stable.

The essential contribution of the present investigation to the analysis and design of a sampled-data system arises from the recognition that the sampling device, though not linear in the usual sense, is additive; that is, responses to separate inputs are superposable. Its response characteristics are accordingly described by a describing function which describes the response at the output of the sampling device when the input is excited by a single exponential of complex frequency s. The describing function is analogous to the usual type of transfer function used to describe conventional linear systems. The essential difference between the sampling device and a conventional linear device is that while a single exponential excitation applied to the usual linear device results in a single exponential output, this is not true of a sampling device. When a single exponential is applied to the sampling device, the resulting output is a whole family of exponentials whose complex frequencies are separated by the radian-per-second equivalent of the sampling frequency, $\frac{1}{t_r}$. The describing function of the linear device, usually called a transfer function, relates the single exponential output component to the single exponential input component. The describing function of the sampling device, not a transfer function, relates the family of exponentials at the output of the sampling device to the single exponential input.

The properties of the sampling device are characterized most simply in terms of an equivalent circuit which has the same describing function as the sampling device. The equivalent circuit has two cascaded components, an impulse modulator and a linear filter. The impulse modulator supplies the additional frequencies to the output, and the linear filter is described by a conventional transfer function. The result of this description is that the only unconventional element in a sampled-data system is the impulse modulator, and its characteristics are very simple to describe in terms of Laplace transforms. If the Laplace transform of the input to the impulse modulator is $\theta_i(s)$, then the Laplace transform of the output from the impulse modulator is $\sum_{n=-\infty}^{\infty} \theta_i(s + jn\omega_r)$, where ω_r is the radian-per-second equivalent of the sampling frequency and n has all integer values and zero. The

fact that the remainder of the system has negligible response to the higher-frequency components means that the only effective elements of the impulse modulator output are those which have small n-values.

Using the equivalent circuit of the sampling device, the remainder of the investigation develops methods for analyzing sampled-error-data control systems. The analysis developed gives the output continuously in time in terms of the continuous input. The relation between the output and input transforms is given directly in terms of element transfer functions and simple sums of them. This fact makes it very easy to correlate changes in the system elements with changes in the system response characteristics; consequently effective design is possible. Techniques are developed to implement this design analysis which are very similar to the techniques already used for conventional systems. The results of this thesis agree identically with results already presented by others, but go considerably further. At all points in the discussion where comparisons with former procedures are possible, these comparisons are made.

The last part of the investigation deals with a discussion of the objectives in the use of feedback in a control system and resulting implications in the design of sampled-error-data feedback systems. The main use of feedback in a control system is to make a high-power, calibratable device from a high-power, uncalibratable feed-forward section which is controlled by a low-power, calibratable measuring device in the feedback link. The design techniques for sampled-data systems are illustrated in a simple example at the end of the thesis.

The results of this investigation can be used in determining: how often the sampling device must sample for satisfactory operation in a given system (i.e. at what intervals the computer must operate); how to design a system for best results with fixed sampling rate; whether or not it is advisable to enclose the sampling device in a feedback loop to relieve accuracy requirements on the control equipment.

6.4 SOLUTION OF POWER NETWORK PROBLEMS ON A DIGITAL COMPUTER

The operating characteristics of large power networks are ordinarily studied by analogue methods on a-c network analyzers. The possibility of making similar studies by numerical methods on a digital computer is the subject of a recent MIT master's thesis which has been published as Project Whirlwind Report R-169.

The problem considered is steady-state network operation; fault studies and transient stability studies have not been included, although future work may prove computers particularly appropriate for this phase of network performance. Similar techniques are applicable to the analysis of hydraulic or pneumatic networks.

The mathematical solutions of problems of power networks operating under steady-state conditions differ from those of pure impedance networks because in the steady state, values of real and reactive power flow are usually specified at the loads irrespective of the voltages at these points. The unknowns to be found for the steady-state solution are the voltages at the loads or buses, the power flow and reactive flow in the network lines, and the required power generation, wherever no values are specified for these quantities. Sometimes other unknowns such as transformer tap setting, possible maximum loads, and system losses may be required.

In contrast to the direct mathematical solutions possible for simple impedance networks, the mathematical solution of the power network problem in closed form is practically impossible, so that methods of successive approximation must be employed. The solution described in this study requires no complex algebra; it takes advantage of the fact that voltage drops throughout a power network are dependent mainly on the flow of reactive power, whereas phase shift depends for the most part on the flow of real power. The two sets of equations stating the two dependencies are written, and a process of successive approximations for the real and reactive parts of the network solution is developed.

A program for performing the steps of successive approximation has been worked out for the Whirlwind I computer. The cycles of orders of the program are made as general as possible to reduce "fitting" of the solution to each specific network. The program is applicable to the general type of power network. Unfortunately the network problem inherently requires a large amount of computer storage, since not only must the characteristics of the network elements, power lines, and buses (loads or generators) be stored, but also the configuration of the entire network must be coded for the computer. Computer instructions are ordinarily kept in the storage element of the computer, but since 820 orders are required in this order program, the input film is used for orders, leaving the main part of the internal storage available for numerical network values. The method of solution then permits a network containing 80 power lines to be solved within the storage limitations of WWI. For larger networks the program would have to be changed to permit external storage of numerical values. The large storage requirement is probably the main drawback to computer solution of power networks.

The time estimated for solution of the problem is less than two minutes for the maximum 80-line network. The estimate is based on the assumption of five steps of successive approximations, that is, five complete traverses of the complete network. The convergence of the solution to correct answers after five approximations seems assured.

A certain amount of work is required to assemble the network data into a form appropriate for computer solution. Some of this work might be done by the computer itself. Furthermore, under the requirements of the solution scheme, the initial data must be given in a standard form. That is, the method assumes that the amount of power generated or the load taken at each bus is known, and that the voltages and line flows of the network are desired. In a more general network problem the data are not usually given in this form but in a mixed form, so that some voltages, for example, are known and some unknown, and similarly for the generation at the various buses. Therefore, for the method of solution given, a cut-and-try method of determining network performance must be used. The network study in this case then resolves itself into the parametric type of solution — e.g., the reactive power generated at the various buses of the network could be varied until the correct network voltages were obtained. The new initial values to be tested at each step would have to be given to the computer.

It seems likely that any standardized form of numerical network solution will suffer from such a limitation, but again the computer itself, given appropriate instructions, could perform the cut-and-try operations. At each step of the solution the computer would vary the parameters in the correct direction to send the solution to a final desired network operating condition.

Certain network values such as the power-system losses are difficult to compute with analogue networks on a-c boards. The numerical solution of such values is much more tractable, and the computer solution looks particularly attractive from this point of view. In fact as far as system losses are concerned, the values are automatically computed within the solution cycle and would be immediately available.

Further work may clarify those aspects of power problems to which the computer is best suited, but even at the present time the application of large-scale digital computers to the general power-network problem seems feasible. The computers can provide fast and accurate numerical answers expressing the exact operating condition of the power network.

7. APPENDIX

7.1 VISITORS

During the past quarter the Laboratory has had among its visitors the following:

Dr. Mina Rees, Dr. Charles V. L. Smith, Dr. Emanuel R. Piore, Dr. Harry Nyquist, Dr. Karl Spangenberg, and Lt. Grace Hopper, all representing the Office of Naval Research.

Dr. Louis N. Ridenour, University of Illinois.

Cmdr. D. W. Mallin, Lt. Cmdr. B. G. H. Rowley, Mr. J. F. Coales, and Mr. W. E. Elliott, all of the British Joint Services Mission, interested in applications of digital computation to naval operations.

Mr. A. Eisenstein of the University of Missouri; and Mr. R. L. McCormack, Mr. N. L. Anderson, Mr. I. E. Levy, and Mr. James Cardell, of Raytheon, to discuss receiving tube life.

Mr. Alan Block of Arma Corporation.

Mr. W. H. Reid, International Business Machines Corporation.

Mr. Paul Stademan, Special Devices Center, ONR.

Dr. H. T. Engstrom, Dr. C. Tompkins, Mr. A. A. Cohen, and Mr. J. M. Coombs, all of Engineering Research Associates.

Dr. G. W. Brown of the Rand Corporation.

Mr. J. H. Halgren, Radio Corporation of America, who was interested in tube problems.

Capt. E. L. Johnson, Capt. E. T. Hayward, Cmdr. R. M. Whittemore, Cmdr. J. R. Roszel, Ensign T. E. Manore, Mr. C. E. Bishop, Mr. G. M. Traveis, and Mr. J. H. Lindsay, all of the Bureau of Supplies and Accounts.

Mr. Charles F. West, Mr. J. E. DeTurk, and Mr. J. H. MacNeill, of Project Hurricane at Raytheon.

Dr. J. W. Marchetti and Dr. Lowell M. Hollingsworth of the Cambridge Field Station, Air Materiel Command.

Mr. L. K. Marshall, Research and Development Board.

Dr. John R. Bowman, Mellon Institute, to discuss vacuum tube problems and chemical storage.

Mr. George J. Gleghorne, Mr. George B. Greene, Mr. Eldred Nelson, and Mr. Eugene M. Grabbe, of Hughes Aircraft Company.

Dr. Ralph E. Meagher, University of Illinois.

Dr. R. W. Shephard, New York University.

Mr. D. U. Burdick, Bureau of Ships.

Mr. L. F. Hope, Research Division, General Motors.

Mr. Harold M. Kelley, du Pont, concerned with possible application of digital computers to mass-spectrograph analysis of organic compounds.

Mr. Gilbert H. Mitchell, Lt. Cmdr. G. O. Atkinson, and Mr. Arnold Shostak, Office of Naval Research.

Mr. J. G. Miles, Engineering Research Associates.

Mr. E. L. Harder, Western Electric Corporation.

Mr. H. L. Bennett and Mr. E. A. Kiessling, Watson Laboratories, Air Materiel Command.

Mr. Harry Goode, Mr. Aaron Coleman, Dr. Walter MacWilliams, Mr. Perry Crawford, Mr. J. L. Little, Lt. Cmdr. D. M. Rubel, Dr. Robert Campbell, Mr. Herbert Sherman, Prof. Edwin Boyan, Mr. Paul Sherertz, Dr. W. Norris Tuttle, Mr. Richard Leghorn, Cmdr. Arthur Gralla, and Mr. E. Burke Hammond, all representing the RDB Ad Hoc Committee on Scientific and Synthetic Analysis.

A group of students taking a special course in computers given by Prof. Caldwell of MIT.

Among visitors interested especially in storage tubes were the following:

Mr. J. H. Muncy of the Naval Research Laboratory.

Mr. John Dumainan of the Cambridge Field Station.

Dr. V. K. Zworykin, RCA Laboratories.

Mr. T. F. Rogers and Mr. L. A. Ames, of the Cambridge Field Station.

7.2 REPORTS AND PUBLICATIONS

Project Whirlwind technical reports and memorandums are routinely distributed to only a restricted number of people who are known to have a need for detailed information on the Project. Other authorized personnel who are interested in particular phases of the work may obtain copies of individual reports by making specific requests for them. Requests for classified material should in general be addressed to the Mathematics Branch, Office of Naval Research, Navy Department, Washington 25, D.C. Requests for unclassified material, or requests for classified material where approval has been previously arranged, should be addressed to John C Proctor, Servomechanisms Laboratory, 211 Massachusetts Avenue, Cambridge 39, Massachusetts.

The following reports and memorandums were among those issued during the second quarter of 1949:

No.	Title	Classification	No. of Pages	Date	Author
SR-16	Summary Report No. 16	Conf.	23	1-49	
SR-17	Summary Report No. 17	Conf.	16	2-49	
SR-18	Summary Report No. 18	Conf.	18	3-49	
R-146	Test Equipment Series - Coder	-	11	5-25-49	R.R. Rathbone
R-147	The Pulse Standardizer	-	10	4-11-49	R.R. Rathbone
R-155	Application of Digital Computers to Simulation of the Anti-Submarine Problem (L-1)	Conf.	29	3-30-49	R.A. Nelson
R-158	Information System of Interconnected Digital Computers for Anti-Submarine Naval Group	Conf.	16	4-12-49	J.W. Forrester R.R. Everett
R-159	High-Speed Pulse Recording on Magnetic Tape (S.M. Thesis; Abstract in E-215)	-	123	4- 6-49	E.S. Rich
R-161	Whirlwind I Test Control (Abstract in E-224)	-	15	4-14-49	G.G. Hoberg
R-162	Trouble Location in a Large-Scale Electronic Digital Computer (S.M. Thesis; Abstract in E-217)	-	70	4-12-49	G.C. Sumner
R-163	A Trouble-Location Scheme for a Digital Electronic Computer (S.M. Thesis; Abstract in E-218)	-	120	4-21-49	G.G. Hoberg E. Blumenthal
R-165	The Convergence of the Gauss-Seidel Iterative Method (S.M. Thesis)	-	11	4-15-49	E. Reich
R-166	Digital Computers as Information-Processing Systems	-	15	6- 1-49	J.W. Forrester
R-167	A Low-Speed Analogue for Analysis of Flip-Flops (S.M. Thesis; Abstract in E-248)	-	80	6- 8-49	J.M. Hunt
R-168	A Dual-Triode Capacitively-Coupled Flip-Flop (S.M. Thesis; Abstract in E-251)	-	89	6-15-49	M.H. Hayes
E-221	Standard Tests for Storage Tubes	-	4	3-30-49	A.H. Ballard C. Corderman
E-222	Low Emission 6AS6 Tubes	-	1	4- 4-49	H.B. Frost
E-223	Storage Tube ST81: Construction, Processing and Initial Testing	-	3	4- 5-49	M. Florencourt
E-225	Study of Input Output Checking	-	14	4-11-49	J.M. Salzer
E-226	Storage Tube ST80: Construction, Processing and Initial Testing	-	1	4-15-49	M. Florencourt
E-227	Storage Tube ST82: Construction, Processing and Initial Testing	-	2	4-15-49	M. Florencourt

No.	Title	Classification	No. of Pages	Date	Author
E-228	Storage Tube ST83: Construction, Processing and Initial Testing	-	2	4-20-49	M. Florencourt
E-229	Arithmetic Modification of Operations	-	8	4-25-49	G. Cooper
E-230	Research Tube RT50-1: Construction and Processing	-	1	4-25-49	M. Florencourt
E-231	Purpose and Operation of Research Tube RT51	-	4	4-28-49	H.E. Rowe
E-232	Results of Tests on RT47, RT47-1 and RT50, Beam-Analyzer Tubes	-	9	5- 2-49	J.H. McCusker
E-233-1	Status of Vacuum Tube Studies	-	6	5- 9-49	H.B. Frost
E-234	Programming Matrix Multiplication with Insufficient Electrostatic Storage	-	13	5- 4-49	P. Rabinowitz E. Reich
E-235	Description of Whirlwind I Codes	-	16	5- 6-49	J.M. Salzer C.W. Adams R.P. Mayer
E-236	Storage Tube ST87: Construction, Processing and Initial Testing	-	2	5- 3-49	M. Florencourt
E-237	Storage Tube ST88: Construction, Processing and Initial Testing	-	2	5- 3-49	M. Florencourt
E-238	Storage Tube ST94: Construction, Processing and Initial Testing	-	3	5- 5-49	M. Florencourt
E-239	Function of the Revised Clock Pulse Control	-	6	5-12-49	J.M. Salzer
E-240	Storage Tube ST95: Construction, Processing and Initial Testing	-	3	5-16-49	M. Florencourt
E-241	Notes on Resistance Measurements of Storage Plates with an Electrometer Circuit	-	5	5-17-49	W.J. Nolan
E-242	Migration and Stabilization of Charges on Storage Surfaces	-	7	5-17-49	H. Klemperer
E-243	Double Reading and Recording Using Eastman Film Units	-	3	5-18-49	J.A. O'Brien
E-244	Storage Tube ST93: Construction, Processing and Initial Testing	-	3	5-19-49	M. Florencourt
E-245	Optimum Programming of Square-Matrix Multiplication with Insufficient Electrostatic Storage	-	7	5-27-49	E. Reich
E-246	Calculation of Correlation Functions by WWI	-	8	6- 1-49	C.W. Adams
E-247	ESD Output Amplifier and Transmission Line	-	5	5-27-49	J.M. Hunt
E-249	Deposit of Film in the Glass Necks of Storage Tubes	-	3	6-10-49	W.E. Pickett
E-250	Temporary Operations for Whirlwind I	-	3	6-17-49	C.W. Adams
E-252	Proposed Test-Control Circuit for Whirlwind I with Test Storage	-	3	6-20-49	G.C. Sumner
M-824	Charts for Temperature Computations	-	1	3-24-49	R. Shaw
M-825	Bi-Weekly Report, Part I, 4-1-49	Restr.	16	4- 1-49	
M-826	Bi-Weekly Report, Part II, 4-1-49	Restr.	16	4- 1-49	
M-827	Summary of B-Register/In-Out Register Test Results	-	1	4- 4-49	G.C. Sumner
M-828	In-Out Orders	-	4	4- 5-49	J.M. Salzer
M-832	Bi-Weekly Report, Part I, 4-15-49	Restr.	17	4-15-49	
M-833	Bi-Weekly Report, Part II, 4-15-49	Restr.	16	4-15-49	

No.	Title	Classification	No. of Pages	Date	Author
M-837	Input-Output Meeting with Representatives of Engineering Research Associates	-	3	4-22-49	R.A. Nelson
M-840	A Preliminary Discussion of the Possibility of Using Transistors in High-Speed Computers	-	8	4-26-49	R.L. Sisson
M-841	Bi-Weekly Report, Part I, 4-29-49	Restr.	15	4-29-49	
M-842	Bi-Weekly Report, Part II, 4-29-49	Restr.	15	4-29-49	
M-843	Glass-Sealing Procedures for Storage Tubes - No. 2	-	5	5- 4-49	W.E. Pickett
M-846	Constant-Frequency Restoration	-	2	5-11-49	J.M. Salzer
M-850	Bi-Weekly Report, Part I, 5-13-49	Restr.	26	5-13-49	
M-851	Bi-Weekly Report, Part II, 5-13-49	Restr.	10	5-13-49	
M-854	Operation of Power-Supply Control System	-	4	5-24-49	C.W. Watt
M-855	Summary of Flip-Flop Storage Output Test Results	-	1	5-23-49	G.C. Sumner
M-856	Bi-Weekly Report, 5-27-49	Restr.	33	5-27-49	
M-860	Bi-Weekly Report, 6-10-49	Restr.	25	6-10-49	
M-861	Summary of Flip-Flop Storage Test Results	-	1	6-13-49	G.C. Sumner
M-862	Data on Secondary Emission from Beryllium and Beryllium Oxide	-	2	6-13-49	H. Klemperer
M-863	"Switch Check": Automatic Testing of the Program Counter and Storage Switch	-	5	6-16-49	C.W. Adams
M-864	A Pursuit Problem	-	2	6-21-49	P. Franklin
M-869	Bi-Weekly Report, 6-24-49	Restr.	25	6-24-49	
C-102-1	Decimal to Binary Conversion	-	2	4- 9-49	C.W. Adams
C-103	A Code for the Ballistic Problem	-	13	4- 1-49	T.W. Hildebrandt
C-105	Numerical Determination of Eigen-Values of Arbitrary Order for a Special Class of Differential Equations	-	7	4-18-49	M. Daniloff